ToASt User's Guide
Draft

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Abstract

This document contains the informations about the design of the ToASt silicon strip readout ASIC.

1 Introduction

The ToASt (Torino Amplifier for silicon Strip detectors) is an ASIC designed for the readout of Silicon Strip Detectors. It is designed in the UMC CMOS 0.11 μm technology.

2 ToASt description

The ToASt ASIC is a 64 channel chip which provides the space, time and deposited energy informations of the particle crossing the detector. The space information is provided via the channel number, while the timing and energy informations come from two time stamps obtained by storing the value of a global counter at the rising and falling edge of a comparator. The rising edge time stamp provides the timing information while the energy information is obtained from the difference between the trailing and the leading edge time stamps (Time-over-Threshold, or ToT method). The ToASt characteristics are summarized on table 1.

The ToASt schematic is depicted in figure 1. The 64 channels are divided into 8 regions. Each region contains the readout and configuration logic for 8 channels and a 16-cells FIFO. The 8 regions are readout by two global readout unit. Each unit has a 64 cells FIFO and a 160 Mb/s serial link. A global configuration unit manages the configuration informations of all regions. The configuration interface is based on a serial link working at 1/2 of the master clock frequency. It controls 16 Global Configuration Registers (GCRn) and 64×3 Channel Configuration Registers (CCRs).

3 Analog Front-End

The Analog Front-End (AFE), depicted in figure 2, is based on four main blocks : a charge-sensitive input amplifier followed by a shaper, a current buffer, a ToT generator and two comparators.

The AFE can be programmed to accept either n-type or p-type detector signals by setting the bit 10 of GCR0 (table 8). The default value is p-type. The simulated ToT gain is 40 ns/fC for p-type detectors and 30 ns/fC for n-type with standard settings. These values corresponds to 6.4 counts/fC and 4.8 counts/fC, respectively.

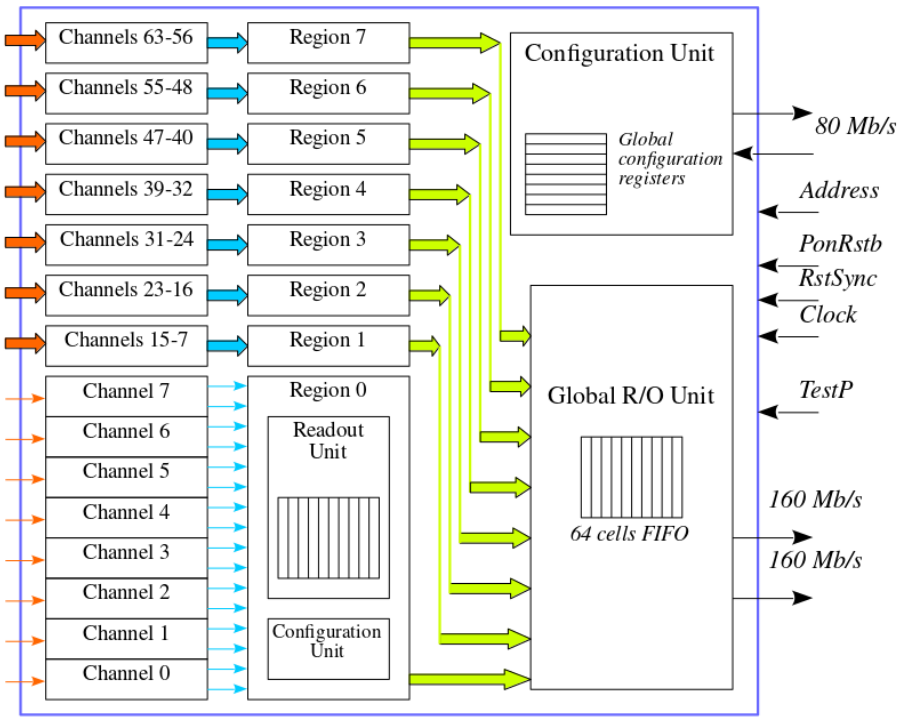

Figure 1: ToASt simplified schematic

In current tests, it seems that a value between 55 and 65 ns/fC is better in terms of channel equalization. The measurements have been performed for the p-type configuration.

Two comparators are implemented in order to improve the trade-off between a good time resolution for the leading edge (which requires a low threshold, where the slope is steep even for low charges) and noise rejection. With two comparators set to different threshold it is possible to store the time stamp on the lower threshold (time threshold) and validate it with a higher threshold (energy threshold). The measurement scheme is depicted in figure 3. This feature can be disabled, thus working with a single threshold (the energy one).

3.1 Test pulse control

A test charge can be injected at the input of each channel. The injection time is controlled by the rising and falling edges of the *TestP* input signal. The two edges sent complementary charge pulses, therefore only one of the two edges should be considered (specifically, the rising edge for the p-type detector configuration and the falling edge for the n-type).

By default the global test pulse enable is disabled (0) and the local test pulse enable is enabled (0). The latter is an error, due to an inversion in the channel logic. It will be corrected in the next version as default disabled (0).

The test charge injection must be enabled both at the global level (GCR14[7] set to 1) and at the channel level (CCR0[5] set to 0).

The test charge value is controlled by the GCR14. GCR14[5:0] controls the voltage amplitude of a test pulse which is a (inverted) copy of the *TestP* input. The test pulse is sent through a 350 fF series capacitor in order to generate two complementary charge pulses. The DAC range can be set in the range [0÷16] fC or [0÷65.8] fC, depending on the value of the range bit GCR14[6]. The voltage DAC works in inverted logic, i.e. the maximum voltage is obtained with hex 00. Table 2 summarize the test pulse tuning.

Table 1: ToASt characteristics

Input capacitance	$2 \div 17$ pF
Max rate per strip	50 kHz
Input charge range	$1 \div 40$ fC
Max noise	1500 e^-
Peaking time	50-100 ns *(prog)*
Channels per chip	64
Channel pitch	66 μm
Reference clock	160 MHz
Charge resolution	8 bits
Time resolution	6.25 ns (pk-pk)
	1.8 ns (r.m.s.)
Output drivers	2×160 MS/s
Max output rate	2×4.9 Mevents/s
Power consumption	180 mW @ 1.2 V
Die size	3.24×4.41 mm^2
Pads position	On two sides only

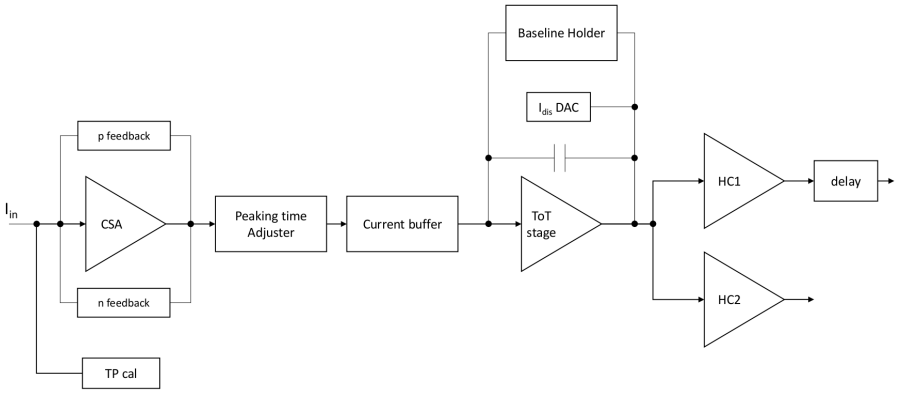

Figure 2: Analog channel

3.2 Thresholds and ToT current control

The threshold voltages and ToT current can be tuned both at the chip level, with a coarser resolution, and at the channel level, with a finer resolution.

The time and energy threshold coarse tuning is performed via two 5 bit DACs controlled by the GCR12 register. The tuning range is 494 mV with a 15 mV LSB. The fine tuning is controlled by two 6-bit DAC controlled by the CCR1 register. The tuning range is 84 mV with a 1.3 mV LSB. The DAC logic is inverted for both coarse and fine tuning, i.e. 0 corresponds to the maximum threshold value and 63 to the minimum one.

The ToT current can be tuned at the coarse level by a 5 bit DAC controlled by GCR13. The current range is from 2.1 nA up to 488 nA with a 15.2 nA LSB. The fine tuning of the ToT current (at the channel level) is controlled by a 5 bit DAC. The channel DAC LSB (and therefore its range) is tuned by a global 5 bit DAC (controlled by GCR13). The minimum range is 27 nA with a 0.84 nA LSB while the maximum one is 906 nA with a 28.3 nA LSB. Also for this control the DAC logic is inverted for both coarse and fine tuning, i.e. 0 corresponds to the maximum threshold value and 63 to the minimum one.

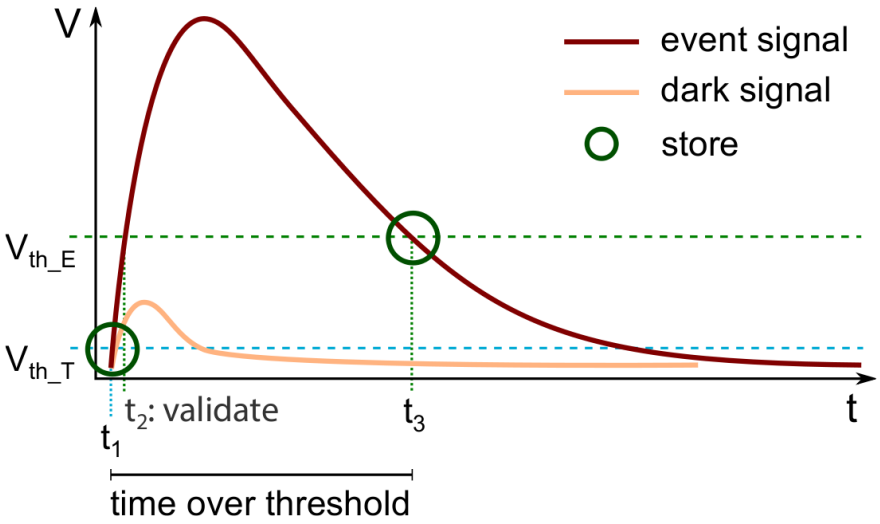

Figure 3: ToT measurement

Table 2: Test pulse tuning

GCR14[6]	**GCR14[5:0]**	$\mathbf{V}_{PULSE}$ *[mV]*	$\mathbf{Q}_{INJ}$ *[fC]*
0	111111	0	0
0	110001	11.3	4
0	000000	47	16.5
1	111111	0	0
1	110001	44.8	15.7
1	000000	188	65.8

3.3 Peaking time control

The peaking time adjuster is controlled between 50 and 100 ns by the GCR6[11:10] bits. Value 00 corresponds to the shortest peaking time and 11 to the longest.

4 Channel Control Unit

The Channel Control Unit (CCU) is the digital circuit controlling the channel functions. It receives the comparator output from the energy branch (EB) and time branch (TB) of the AFE and the 12 bits time stamp from the global controller via the region controller.

It contains 4 Hamming-protected 12 bits registers : a leading *(falling)* edge register to store the time stamp value at the rising *(falling)* edge of the comparator signal and two control registers to store local configuration informations.

The time stamp corresponding to the rising and falling edge of the input signal (the input signal selection is described later in this section) are stored in the leading and falling edge registers, respectively. The first value provides the event Time of Arrival (ToA) while the difference between the two is a measure of the energy deposited via the Time over Theshold (ToT) method. When an event is ready to be readout a *data_ready* signal is asserted. If the *freeze* input signal is asserted, the event is kept but no *data_ready* is asserted. The freeze mechanism is used to correctly divide data into frames. It should be noted that the *freeze* does

not prevent the readout of an event if its leading edge has arrived before the its assertion. A *busy* signal is asserted when the channels has received a leading edge and is waiting for the falling one.

During normal operations the leading edge time is stored on the rising edge of the TB comparator, while the falling edge time is stored on the falling edge of the EB comparator if a EB rising edge has been detected before the TB falling edge. Otherwise the even is discarded. When the single_th signal is set to 1, both registers are loaded on the edges of the EB signal, while the TB signal is ignored.

In the *le_only* mode, only the leading edge time stamp is stored. This mode of operation can be used when the ToT information is not required but the chip must sustain a high rate. In this case the ToT discharge current should be set to its maximum in order to minimize the dead time in the AFE.

The configuration registers are mapped as described in table 3. The calibration DACs range are relative to the values set by the corresponding global calibration DACs. The range bit of the two DACs halves the LSB value (0→3.12 mV, 1→1.56 mV). The CCU receives also the global configuration signals described in table 4

Table 3: Channel configuration registers bit assignment

Reg	**Bits**	**Function**	**Default**
0	11:8	*Reserved for future use*	0000
0	7	Channel mask	0
0	6	Delay enable	0
0	5	Calibration enable	0
0	4:0	ToT discharge current calibration DAC	00000
1	11	Energy threshold DAC range	0
1	10:6	Energy threshold DAC	00000
1	5	Time threshold DAC range	0
1	4:0	Time threshold DAC	00000

Table 4: Common channel configuration signals

Name	**Function**
single_th	use EB signal only
le_only	leading edge only mode
polarity	detector polarity

5 Region Control Unit

A Region is defined as a group of 8 channels. The Region Control Unit (RCU) continuously reads the 8 channels with a round-robin algorithm and stores the channel address, leading and trailing edge time stamps in a 27 bits, 16 cells Hamming-protected FIFO.

5.1 Freeze management

The freeze signal is asserted when at the time stamp counter roll-over and de-asserted when no *busy* and *data_ready* signals are active. Therefore all events with leading edge time before the time stamp counter roll-over will be read-out before events coming after the roll-over, independently from the duration of the ToT.

6 Global Readout Unit

6.1 Output data format

The output data format is described in table 5. The data are organized in 32 bits word, containing the the region and channel addresses (2×3 bits) and the leading and trailing edge time stamps (2×12 bits). Data corresponding to the same time stamp counter cycle are packed in frames, delimited by a frame header and a frame trailer. The frame header contains the chip address (as defined by the 7 address pads) and the frame number (from the frame counter). The frame trailer contains the number of data words present in the frame and a 16 bits CRC. When no data are available, a synchronization packet is transmitted.

Table 5: Data formats

Packet type	Header *2 bits*	Data *30 bits*
Data	11	Region[2:0] Channel[2:0] Le[11:0] Te[11:0]
Header	10	10 ChipId[6:0] Reserved[12:0] FrameN[7:0]
Trailer	01	01 DataCnt[11:0] CRC[15:0]
Sync	00	00 1100 1100 1100 1100 1100 1100 1111

7 Global Control Unit

The Global Control Unit (GCU) controls the 8 regions corresponding to the 64 ToASt channels.

7.1 Reset management

The chip reset input is synchronous and controls two internal reset signals : the global reset and the time stamp counter reset. The internal resets are controlled by the external input signal duration according to the following rules :

- 1 clock cycle reset pulse : ignored
- 2 clock cycles reset pulse : a 2 clock cycles time stamp reset is generated
- 3 clock cycle reset pulse : ignored
- 4 or 5 clock cycles reset pulse : both global and time stamp reset are generated. The pulse length is 2 clock cycles
- n>5 clock cycles reset pulse : both global and time stamp reset are generated. The pulse length is (n-3) clock cycles.

The time stamp counter resets also the readout logic; therefore when the output drivers enable configuration is changed, this reset signal has to be sent in order to effectively change the configuration.

7.2 Configuration control

The configuration control logic is the interface to the ToASt configuration registers. It accepts a 16 bits command via a serial link working at 1/2 of the master clock frequency and sends out 16 bits data over an output serial link working at the same reduced frequency. The operation codes are described in table 6, where $a_6a_5a_4a_3a_2a_1a_0$ is the 7-bits chip address while a_B is the broadcast address (i.e. the command is executed by all chips).

Table 6: Configuration operation codes.

Function	**Data** 4 bits	**Op code** 12 bits
Chip Select	1101	$01a_Ba_6a_5a_4a_3a_2a_1a_000$
Chip Deselect	0000	00xx xxxx xxxx
Register select (channel)	0100	$0000r_2r_1r_00c_2c_1c_0a_0$
Register select (region)	0100	$0000r_2r_1r_01a_3a_2a_1a_0$
Register select (global)	0100	$00010a_6a_5a_4a_3a_2a_1a_0$
Register write	0101	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
GCR read word	1000	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Channel register read word	1010	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$

In table 6, the addresses are interpreted as follows :

- GCR write : $d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$ is the 12 bit data to be written in the register
- Region and channel select : $r_2r_1r_0$ is the region address
- Channel select : $c_2c_1c_0$ is the channel address
- Channel select : a_0 selects DAC_If register (0) or DAC_th registers (1)
- Channel write : if DAC_If is selected, $d_4d_3d_2d_1d_0$ is written in the DAC_If channel register. if DAC_th is selected, $d_9d_8d_7d_6d_5$ is written in the DAC_thE register and $d_4d_3d_2d_1d_0$ is written in the DAC_thT register.

The received command is re-sent out from the serial output.
Important note : after a read command the configuration unit is not ready to accept another command until the read output word has been sent out. Idle codes have to be inserted to avoid the reset of the link.

Note : in the current version no region registers are implemented.

The ToASt operations are controlled by 12 bits Global Configuration Registers (GCRs). The bit assignment of GCR0 and GCR1 are shown in tables 8 and 9.

8 Calibration procedure

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The gain calibration procedure consists of the following steps :

- Data acquisition from a test pulse calibration DAC scan from 0 to 63 (i.e. from 0 to 16 fC) with (at least) 16 points and a ToT calibration DAC scan from 0 to 31 with 32 points.
- Calculation, for each channel and each ToT calibration DAC code, of the slope of the ToT vs test pulse calibration DAC code line (i.e. the channel gain)
- Define a reasonable target gain (in current tests, 60 ns/fC has been used as reference value. Also 55 and 65 ns/fC give good results)
- For each channel, search of the ToT calibration DAC value which provides the gain closest to the reference one.
- Store the ToT calibration DAC codes obtained with the previous step in a configuration file and upload in the ToASt CCR0 registers.

8.1 Offset calibration

The offset calibration procedure consists of the following steps :

- Load the gain calibration file obtained with the previous procedure
- Data acquisition from a test pulse calibration DAC scan from 0 to 63 (i.e. from 0 to 16 fC) with (at least) 16 points and a time and energy threshold calibration DAC scan from 0 to 31 with 32 points. The two thresholds should be moved toghether. If the threshold dispersion is not very high, the range 32-63 can be used for more precise tuning
- Calculation, for each channel and each threshold calibration DAC code, of the intercept of the ToT vs test pulse calibration DAC code line (i.e. the channel offset)
- Define a reasonable target offset (in current tests, -30 ns has been used as reference value. Also -25 and -35 ns give good results)
- For each channel, search the threshold calibration DAC code DAC value which provides the offset closest to the reference one.
- Store the threshold calibration DACs obtained with the previous step in two configuration files and upload in the ToASt CCR1 registers.
- A constant offset can be added to the energy threshold registers in order to exploit the double threshold mechanism.

9 Known problems and workarounds

- Channel calibration enable :
  - **Problem :** The channel calibration enable is active low. Its default value is 0, therefore at the reset all channels are enabled to receive the test pulse.
  - **Solution :** invert the signal in the local calibration logic for the next version
  - **Workaround :** program the channel control register with the correct values at startup

10 ToASt pinout

The ToASt pinout is listed in table 7

Table 7: ToASt pinout

Pin name	**Pin type**	**Direction**	**Description**
in[63:0]	Analog	In	Analog input
PonRstb	CMOS	In	Asynchronous reset
SyncRst±	SLVS	In	Synchronous reset
ClockIn±	SLVS	In	Input clock
ChipAddr[6:0]	CMOS	In	Chip address
TestPulse	CMOS	In	Digital test pulse
CfgRx±	SLVS	In	Configuration receiver
CfgTx±	SLVS	Out	Configuration transmitter
TxOut0±	SLVS	Out	Data serial output 0
TxOut1±	SLVS	Out	Data serial output 1
SEU_error	CMOS	Out	SEU error detected
Vbg	Analog	In	Reference voltage (600 mV)
VDDA	power	IO	Analog supply voltage
VSSA	ground	IO	Analog ground
VDDD	power	IO	Digital supply voltage
VSSD	ground	IO	Digital ground
VDDE	power	IO	IO supply voltage
VSSE	ground	IO	IO ground

11 Global Configuration Registers bit assignment

This section describes the GCR bit assignment. Tables 10, 11 and 12 show the bit assignment for the control of the global DACs for the analog section. In these tables :

- CSA : Charge Sensitive Amplifier
- PTA : Peaking Time Adjuster
- CB : Current Buffer
- BLR : BaseLine Restorer
- HC : Hysteresis Comparator

Table 8: GCR0 bit assignment

Bit	**Function**	**Default**
11	*not used*	0
10	detector polarity	1
9	leading edge-only mode	0
8	single threshold mode	0
7	*not used*	0
6	Frame counter reset	0
5	Tx 1 enable	0
4	Tx 0 enable	1
3:2	*not used*	00
1	Time stamp counter Gray mode	1
0	Time stamp counter enable	1

Table 9: GCR1 bit assignment

Bit	**Function**	**Default**
11	*not used*	0
10	CfgTx inversion	0
9	Tx_1 inversion	0
8	Tx_0 inversion	0
7:4	CfgTx output current control	1000
3:0	Tx 0 and 1 output current control	1000

Table 10: Analog control GCR bit assignment

Register	**Bit**	**Function**	**p-type** *(default)*	**n-type**
GCR2	11:10	*Not used*	00	
GCR2	9:5	CSA load Ibias	10010	
GCR2	4:0	CSA gain boost Ibias	00101	
GCR3	11:10	*Not used*	00	
GCR3	9:5	CSA gain boost Vbias	01111	01011
GCR3	4:0	CSA source followers Ibias	10000	
GCR4	11:10	*Not used*	00	
GCR4	9:5	Preamp feedback pMOS Ibias	10100	11111
GCR4	4:0	Preamp feedback nMOS Ibias	11111	10100
GCR5	11:10	*Not used*	00	
GCR5	9:5	Preamp Ishift	11111	00101
GCR5	4:0	PTA Ibuf	11111	10101
GCR6	11:10	PTA control	00	
GCR6	9:5	PTA pMOS Ibias	01110	11111
GCR6	4:0	PTA nMOS Ibias	11111	01110

Table 11: Analog control GCR bit assignment

Register	**Bit**	**Function**	**p-type**	**n-type**
GCR7	11:10	*Not used*	00	
GCR7	9:5	CB Ibias 1	11000	
GCR7	4:0	CB Ibias 2	01101	
GCR8	11:10	*Not used*	00	
GCR8	9:5	CB Vbias	10110	
GCR8	4:0	ToT Ibias	10100	
GCR9	11:10	*Not used*	00	
GCR9	9:5	BLR Ibias	10010	
GCR9	4:0	BLR Vcas	00110	
GCR10	11:10	*Not used*	00	
GCR10	9:5	HC Ibias 1	11000	
GCR10	4:0	HC Ibias 2	11000	

Table 12: Analog control GCR bit assignment

Register	Bit	Function	p-type	n-type
GCR11	11	*Not used*	0	
GCR11	10:6	HC Ibias 3	11010	
GCR11	5:0	Baseline Vbias	100000	
			101000	
GCR12	11:10	*Not used*	00	
GCR12	9:5	time threshold bias	01001	
GCR12	4:0	energy threshold bias	01001	
GCR13	11:10	*Not used*	00	
GCR13	9:5	ToT Ifb DAC Ilsb	01101	
GCR13	4:0	ToT Ifb DAC Imin	10101	
GCR14	11:8	*Not used*	0000	
GCR14	7	Calibration enable	0	
GCR14	6	TP scale	1	
GCR14	5:0	Ib calibration	110001	

Table 13: Region disable register

Register	Bit	Function	Default
GCR15	11:8	*Not used*	0000
GCR15	7	Region 7 disable	0
GCR15	6	Region 6 disable	0
GCR15	5	Region 5 disable	0
GCR15	4	Region 4 disable	0
GCR15	3	Region 3 disable	0
GCR15	2	Region 2 disable	0
GCR15	1	Region 1 disable	0
GCR15	0	Region 0 disable	0