ToASt design - *DRAFT*

Gianni Mazza

INFN sez. di Torino

mazza@to.infn.it

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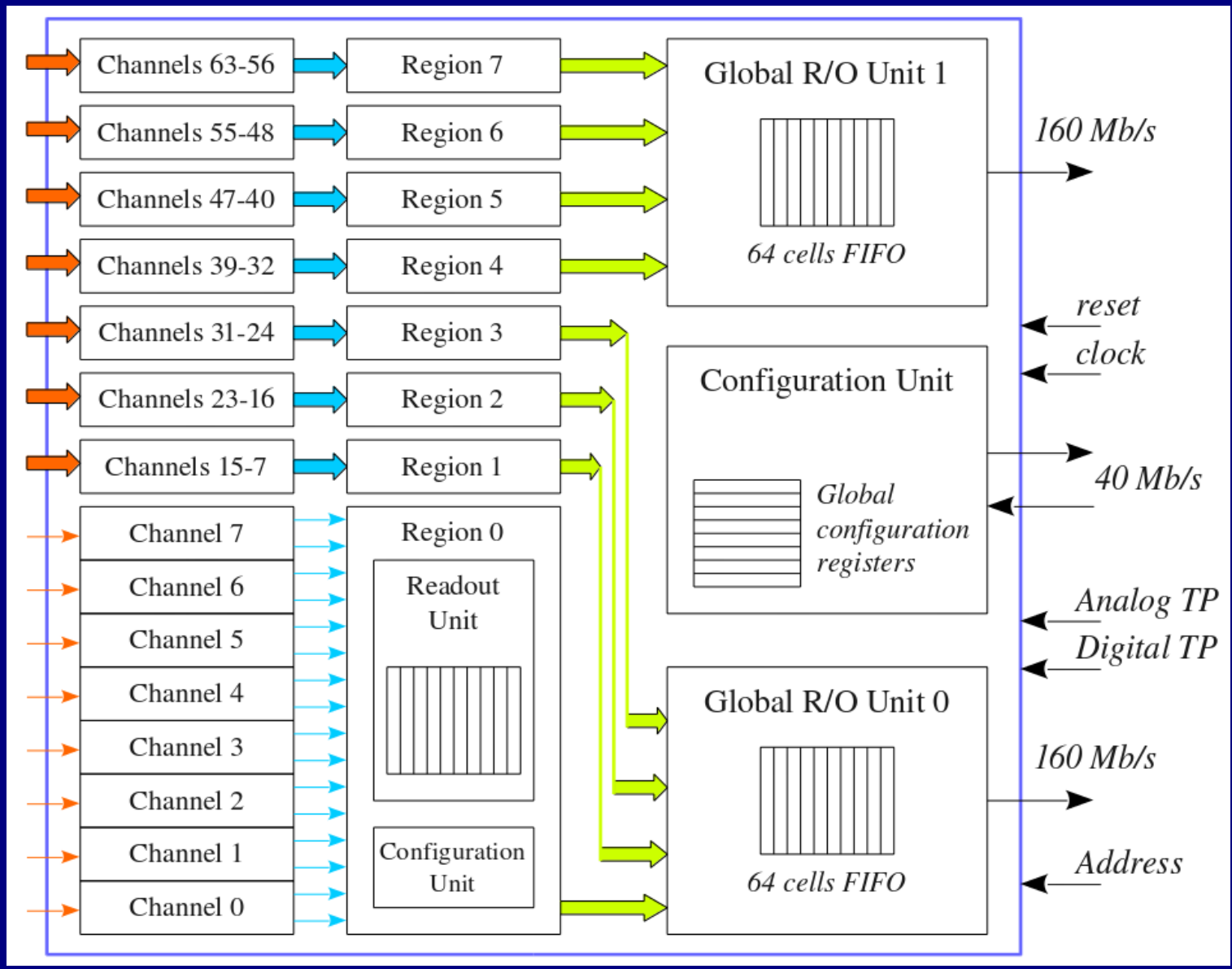
Specifications

Input capacitance	2÷17 pF
Max rate per strip	50 kHz
Input charge range	1÷40 fC
Max noise	1500 e^-
Channels per chip	64
Reference clock	160 MHz
Charge resolution	8 bits
Time resolution	6.25 ns (pk-pk)
	1.8 ns (r.m.s.)
Max power consumption	256 mW (4 mW/ch)
Max chip dimensions	4.5 $\times$ 3.5 mm^2
	4.2 (?)$\times$ 3.5 mm^2
Pads position	On two sides only

ToASt architecture



Pinout proposed changes

PASTA			ToASt	
SyncReset	Rx		SyncReset	Rx
ClockIn	Rx		ClockIn	Rx
ClockOut	Tx		(1)	
ChipSelect	Rx		ChipAddr	(2)
TestPulse	Rx		Digital_TP	Rx
			Analog_TP *(tbd)*	Rx
SerialIn	Rx		SerialIn	Rx
SerialClk	Rx		(3)	
SerialOut	Tx		SerialOut	Tx
TxOut_0	Tx		TxOut_0	Tx
TxOut_1	Tx		TxOut_1	Tx

(1) is it really needed ?

(2) fixed address, hardwired on PCB

(3) configuration link works at $F_{CLK}/4$

Channel configuration

Register	Bits	Function
0	11:8	*Reserved for future use*
0	7	Channel mask
0	6	Delay enable
0	5	Calibration enable
0	4:0	ToT discharge current calibration DAC
1	11:10	*Reserved for future use*
1	9:5	Energy threshold calibration DAC
1	4:0	Time threshold calibration DAC

Global configuration

Register	Name	Function
?	single_th	use EB signal only
?	le_only	leading edge only mode
?	polarity	detector polarity
More to be added...		