Hybrid pixel detector with epitaxial sensors and readout in 130nm CMOS technology for PANDA

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in the PANDA Collaboration

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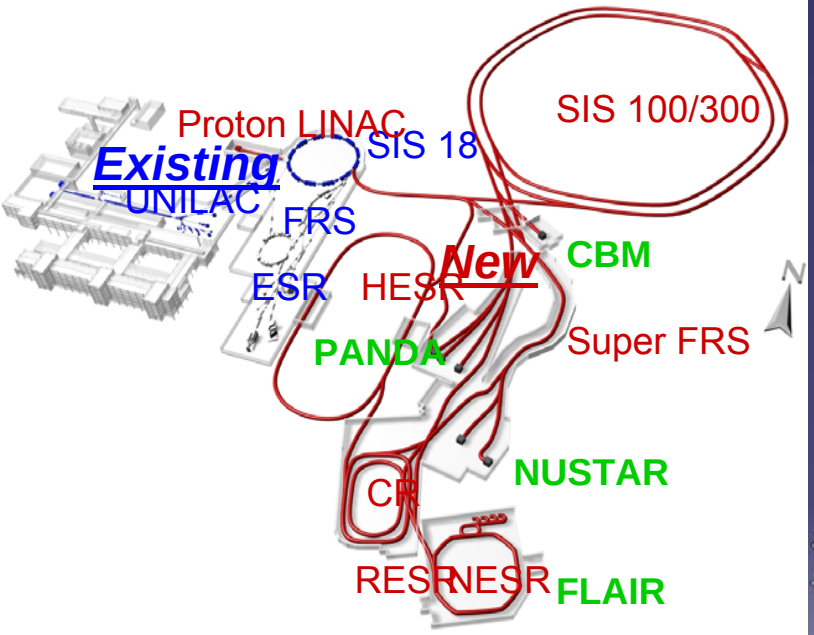
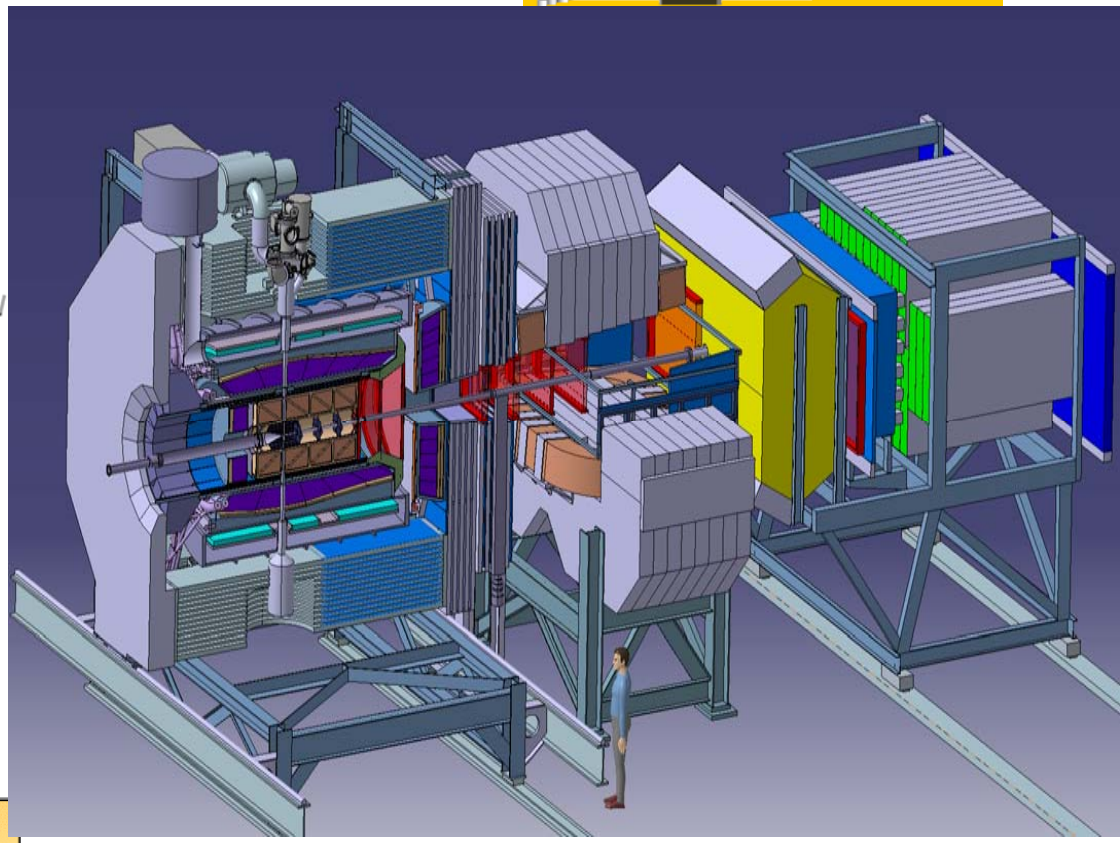
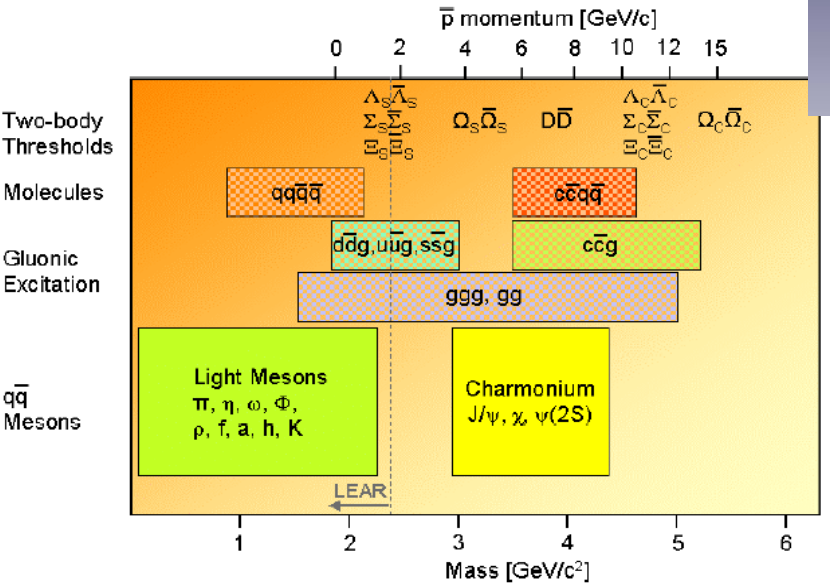
Overview

- Introduction – the MVD in PANDA
- Custom pixel detector
    - epitaxial silicon devices - results
    - pixel readout prototype - results
- Conclusion

Facility for Antiproton and Ion Research

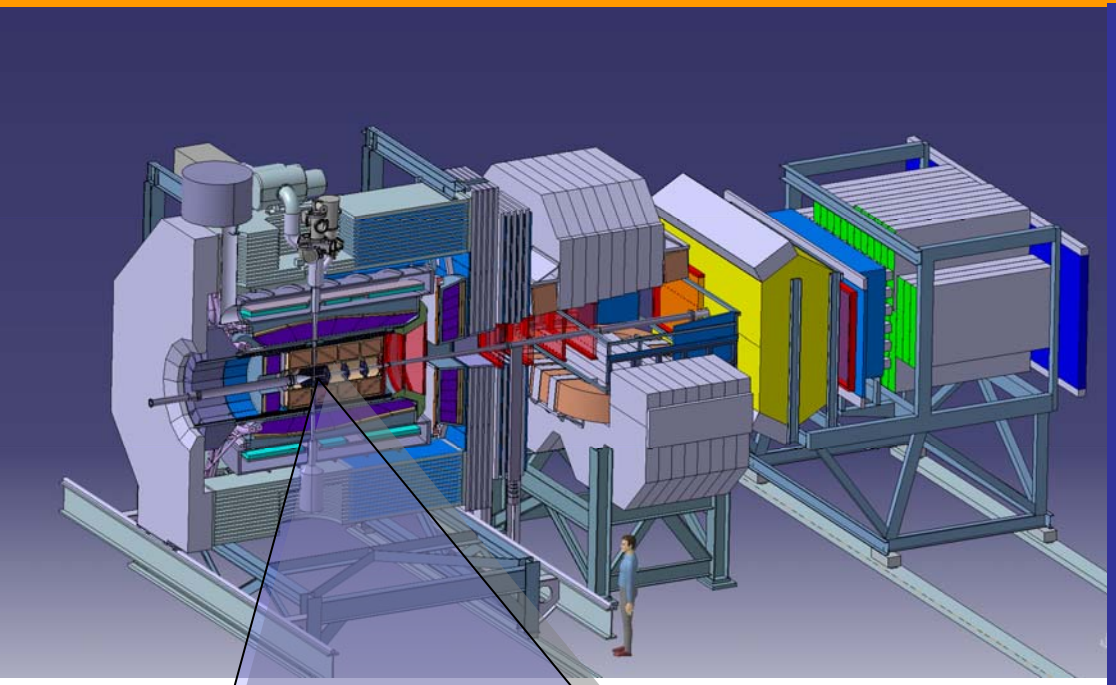


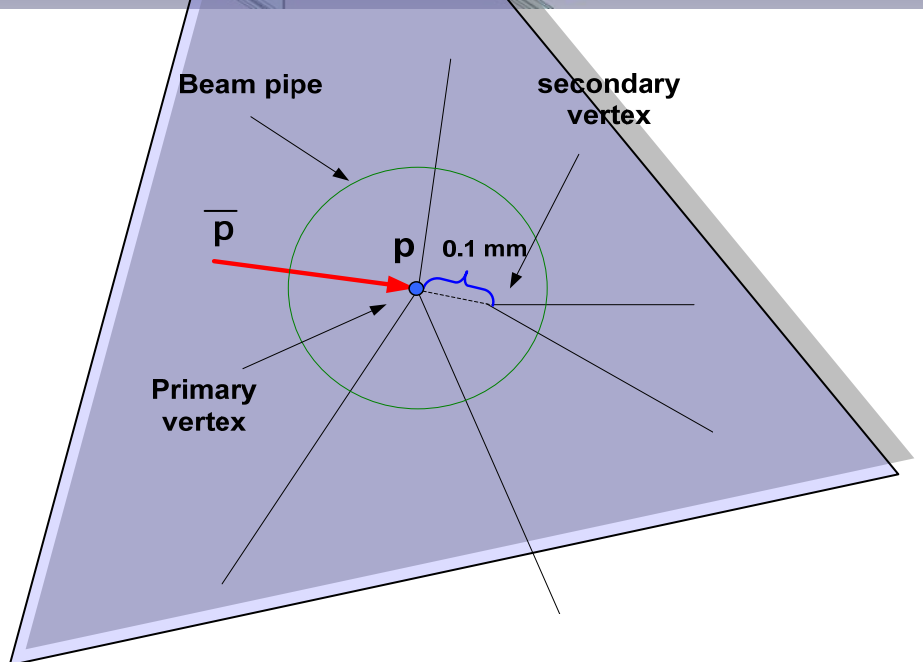




- Nearly 4π solid angle
- High rate capabilities ($2 \cdot 10^7$ annihilations /s)
- Continuous readout and Efficient event selection
- Moment resolution (1%)
- Vertex info for D, K^0_s, L (c_τ = 317 μm for D^{+-})
  - good tracking
- Good PID (γ, e, m, π, k, p) with Cherenkov, tof, dE/dx

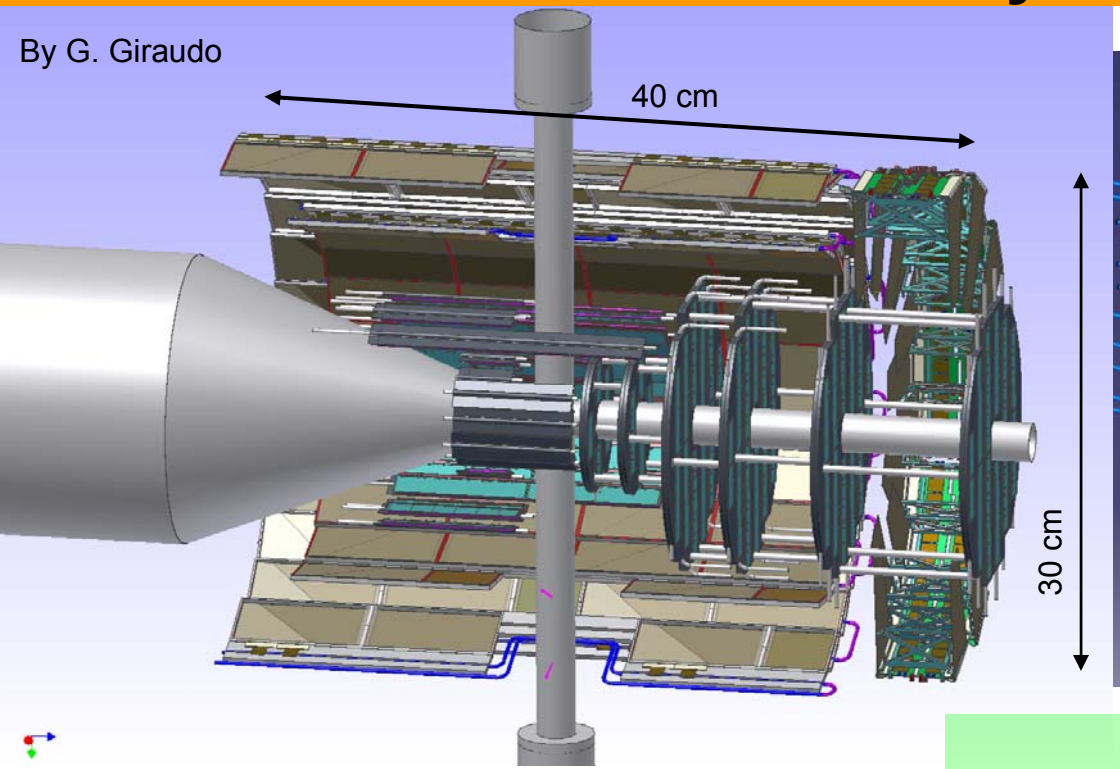
Micro-Vertex-Detector requirements

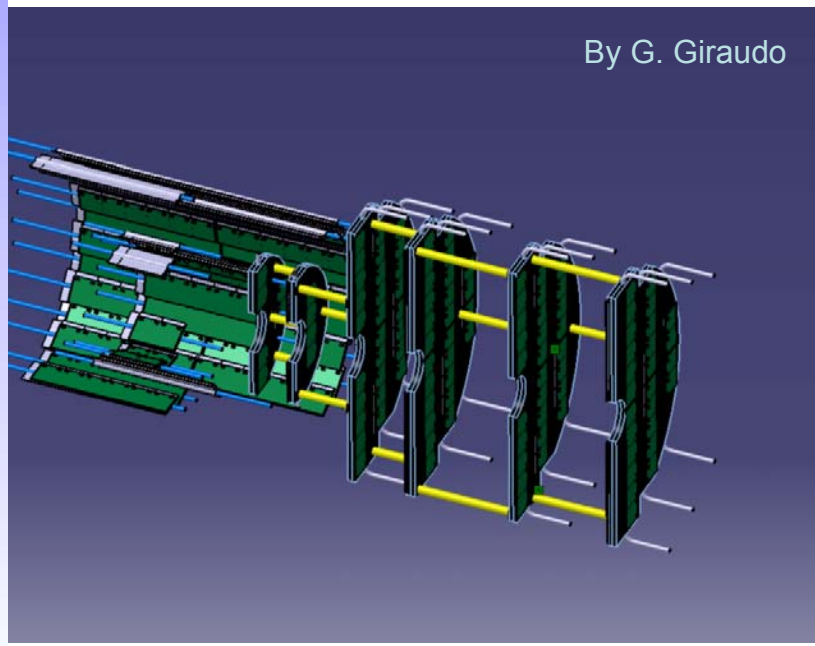




- Good spatial resolution in r-phi
  - Momentum measurement of pions from D* decays
- Good spatial resolution specially in z
  - Vertexing, D-tagging
- Good time resolution
  - rms 6 ns (at 50 MHz clock) with $2 \cdot 10^7$ ann/s
- Triggerless readout
- Energy loss measurement
  - dE/dx for PID
- Low material budget
  - low momentum of particles (from some hundreds of MeV/c) (<1% X_0 for each layer)
- Radiation hardness (~$4 \cdot 10^{13}$ n $_{1MeV\ eq}$ /cm^2) (half year data taking, 15 GeV/c antip-p)
  - Different radiation load

MVD layout





Micro Vertex Detector

4 barrels

Inner layers: hybrid pixels

Outer layers: double sided strips

and 6 forward disks

4 disks: hybrid pixels

2 disks: pixel and strips mixed

(see also the Poster Session I:
'A high rate low radiation length Micro-Vertex-Detection for the PANDA experiment', T. Stockmanns)

Custom Pixel Detector:

- 100 μm x 100 μm pixel sizes;
- ~ 1000 FE readout chip (114x110 pixels);
- continuous data transmission without trigger
- maximum event rate per cm^2:

~ 12.3 MHz for pbar-Au at 15 GeV/c

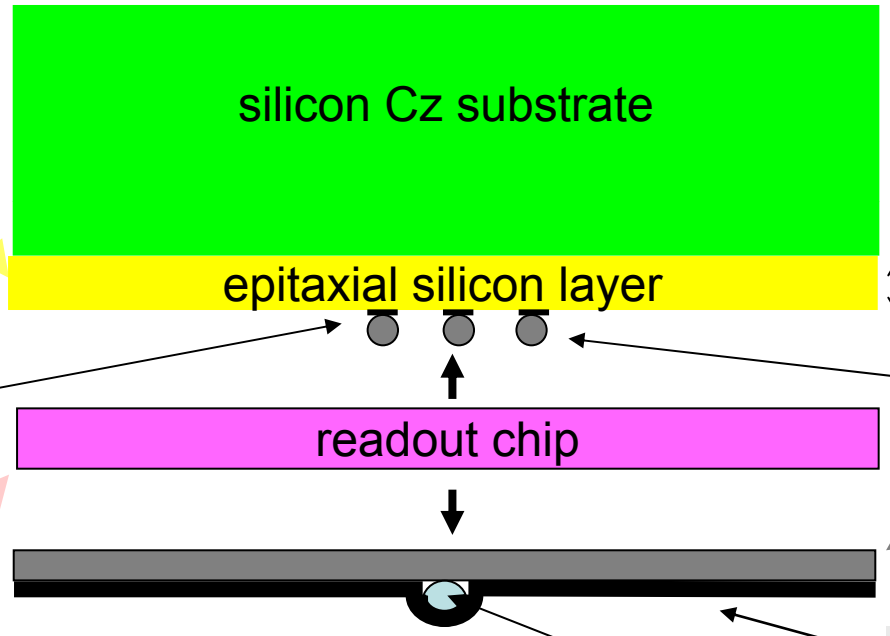
- max. chip data rate : ~ 0.8 Gb/s (40 bit/pixel)
- energy loss measurement: time over threshold;

dynamic range: →100 fC

Standard hybrid technology

THIN PIXEL SENSORS
(< 150 μm) realized with EPITAXIAL SILICON material (suggested by Boscardin-FBK)
(At LHC: thickness of 200 μm; at RD50 diodes with epitaxial material)

The thinning starts from this side, reducing the substrate to tens of μm.



ρ = 0.01÷ 0.02 Ω·cm
d = some hundreds of μm

ρ = 3 ÷ 4 KΩ·cm
d = 25 ÷150 μm

Several processes for defining geometry and for obtaining pixel sensors are made on this side

Bump bonding

Carbon foam support to improve power dissipation

Carbon fiber mechanical support

Cooling system

ASIC developed by the 130 nm CMOS technology with triggerless readout.
Up to now the readout is in 250 nm CMOS technology (see LHC experiment with trigger)

Epitaxial silicon devices

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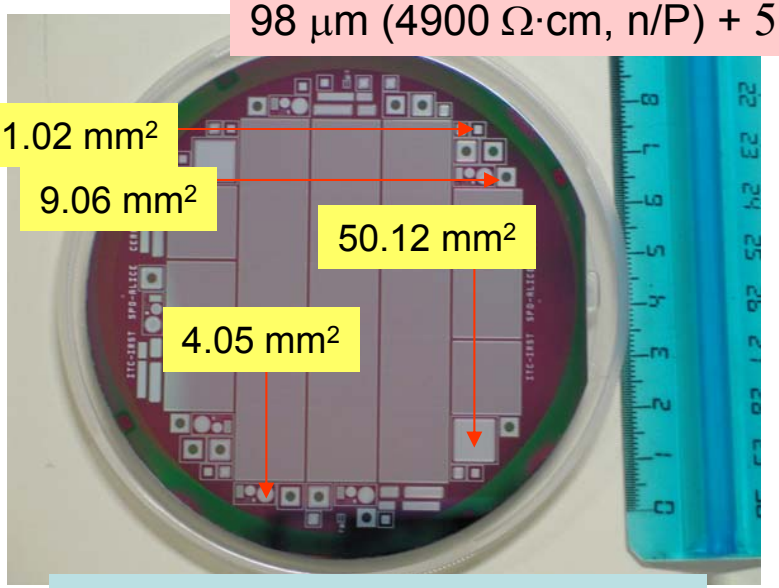
Diodes and single chip sensor from epi-wafers

49 μm (4060 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 100 μm
74 μm (4570 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 120 μm
98 μm (4900 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 150 μm



with the ALICE layout at FBK

Single chip assembly

- ✓ pixel obtained with the ALICE masks (50 μm x 425 μm)
- ✓ test performed using ALICE pixel readout chip and test system in collaboration with P. Riedler - CERN

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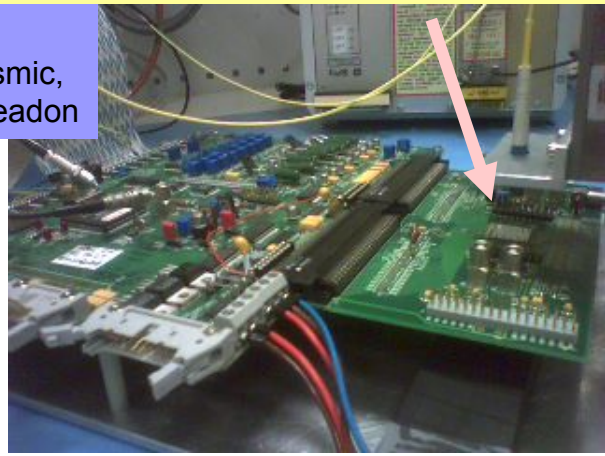
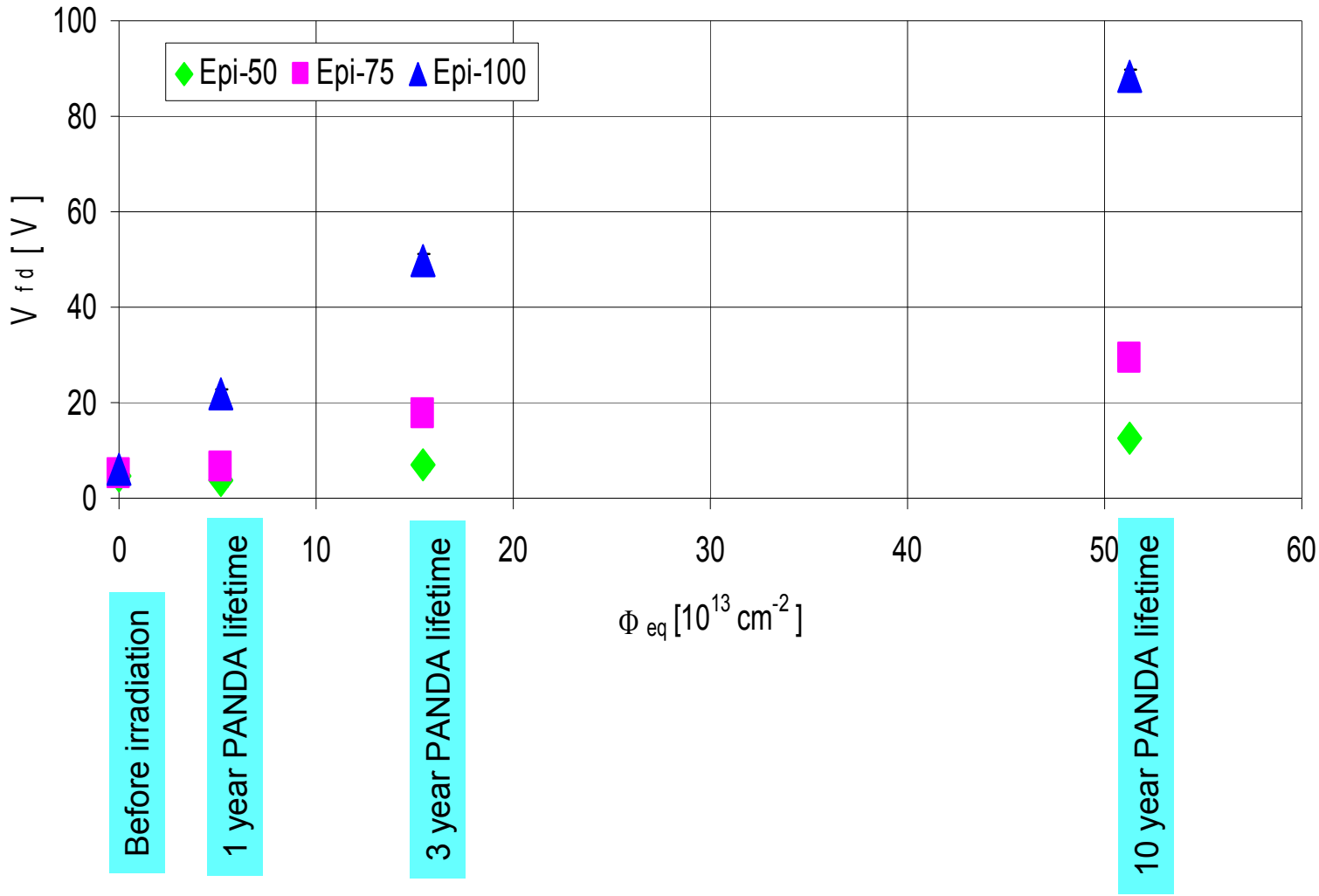


Diodes

Test of radiation damage with neutrons from Pavia nuclear reactor. Equivalent fluence values on the diodes : 5.13×10^{13}, 1.54×10^{14}, 5.13×10^{14} n(1MeV$_{eq}$)/cm^2 corresponding to ~ 1, 3 and 10 years of PANDA lifetime

300 μm FZ diodes have been used as reference

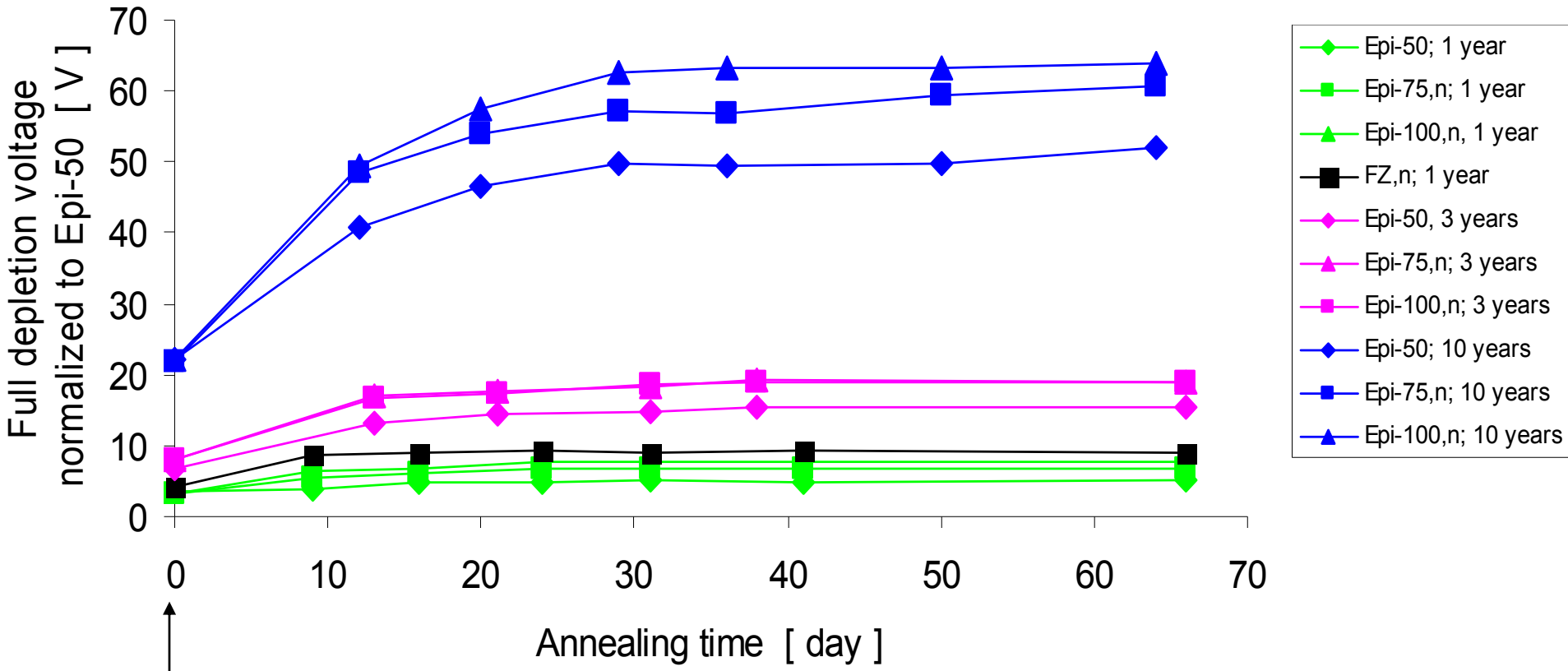
Results from radiation damage test with neutrons



FZ diode full depletion voltage:
14 V 150V >500V >500V

Results from Annealing Phase @ 60°C:

full depletion voltage normalized to 50 μm thickness



After irradiation, before annealing

$V_{fd} = eN_{eff}d^2 / 2\varepsilon_S$

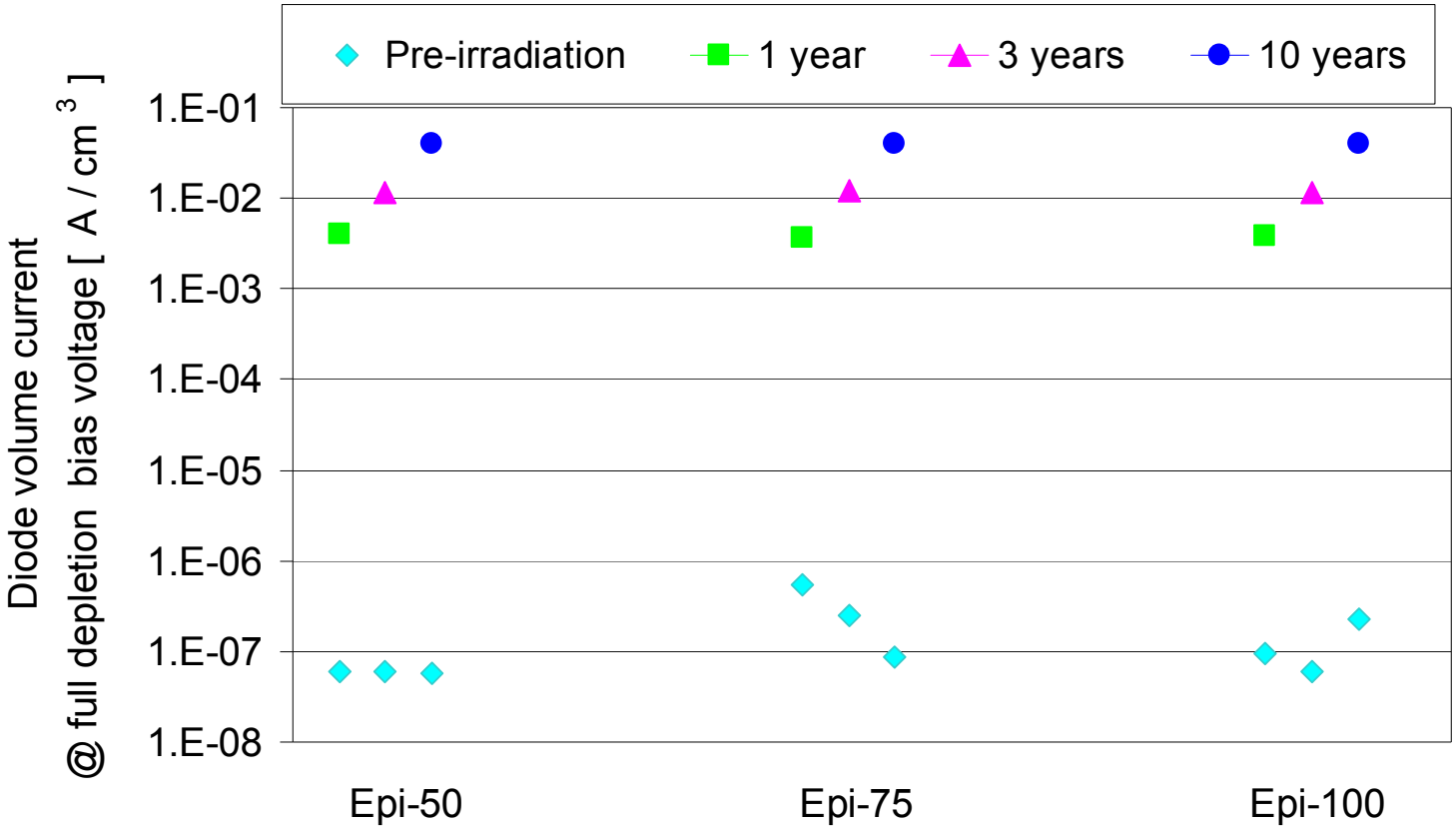
Neff: effective doping concentration

d: diode thickness

ε_S : silicon dielectric constant

Results from radiation damage test:
the radiation damage constant

Equivalent fluence values on the diodes : 5.13×10^{13}, 1.54×10^{14}, 5.13×10^{14} n(1MeV$_{eq}$)/cm^2 corresponding to 1, 3 and 10 years of PANDA lifetime



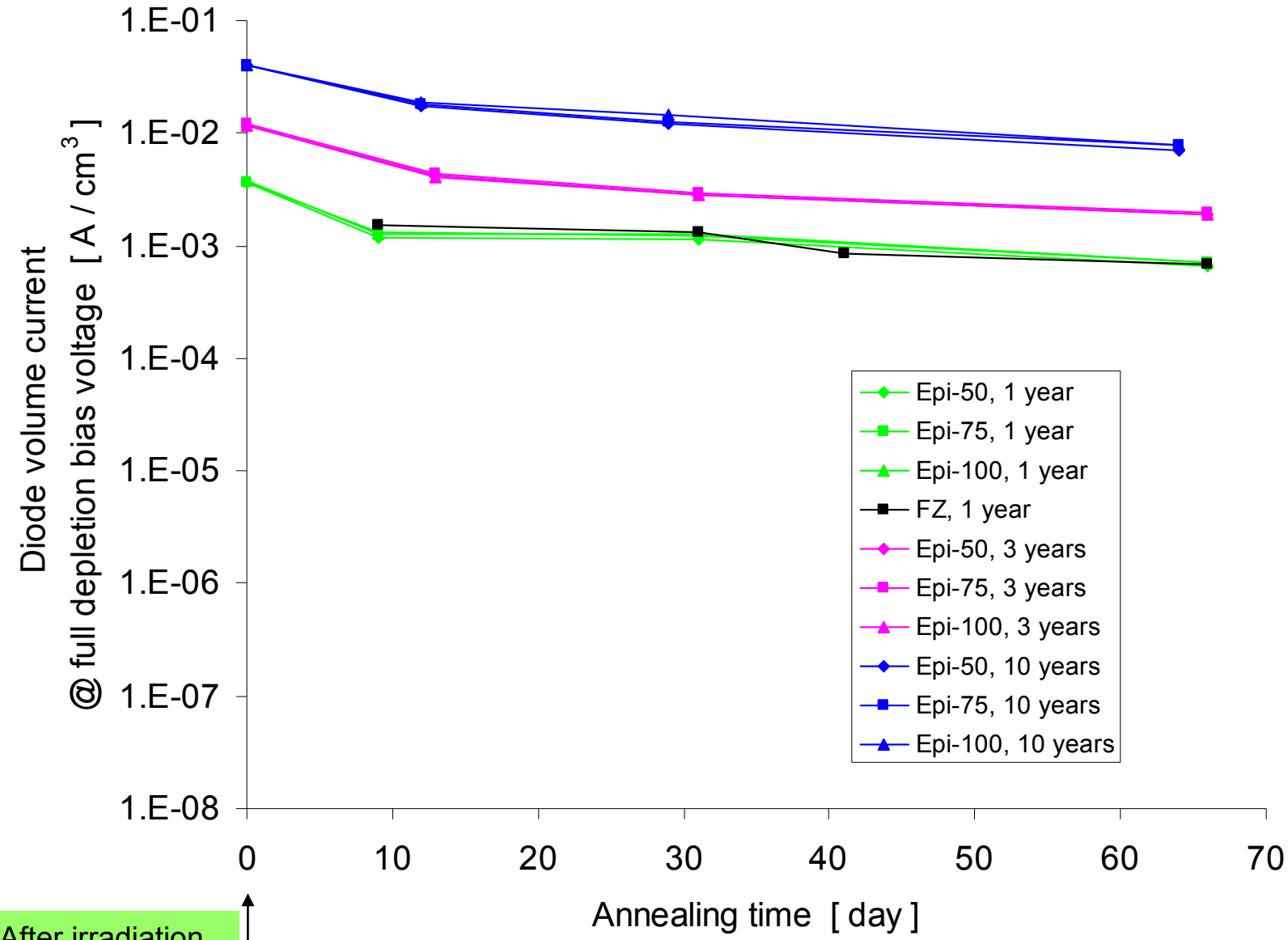
The radiation damage constant is

$\alpha = \Delta J/\Phi = 7.6(\pm 0.3) \times 10^{-17}$ A/cm for all diodes.

Lekage current < 50 nA/pixel (100 μmx100μm size, 100 μm thick)

Results from annealing phase @ 60°C:

diode volume current @ full depletion voltage



After irradiation, before annealing

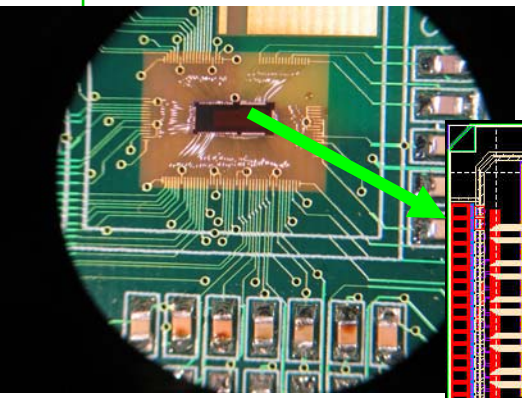
ASIC prototype

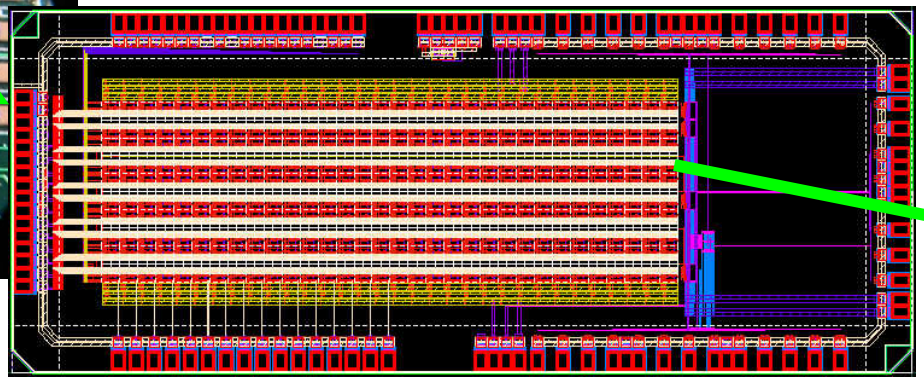
D. Calvo

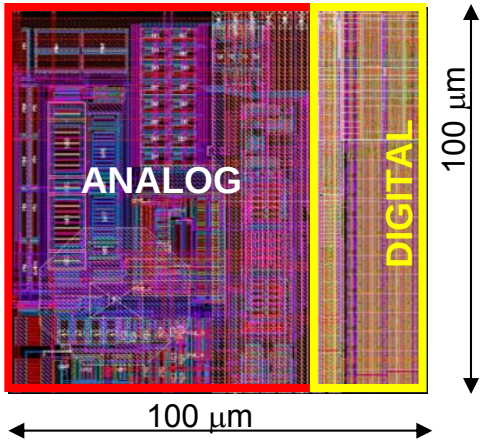
Second pixel readout prototype

ToPix_2, CMOS 130 nm technology

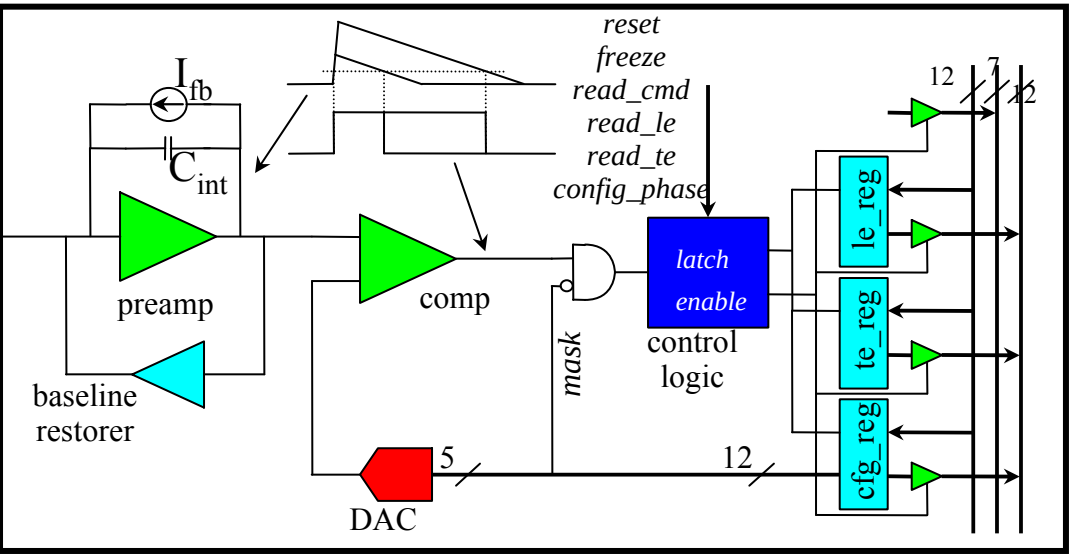
- 5x2 mm^2 area with 4 folded columns with a total of 320 readout cells of 100x100μm^2 size
- analogue + digital circuits (analog power consumption below 12μW @1.2V)
- Time over Threshold technique implemented to obtain a energy loss measurement
- SEU-hardened memory cells (Dice layout)
- absence of enclosed structures to study the radiation tolerance of the 130nm CMOS technology
- inputs for connecting external sensors
- selectable input polarity
- comparator threshold controlled by DAC (5 bits)
- 12 + 12 bits leading and trailing edge and 12 bits configuration registers
- 12 bits bus for time stamp and 12+7 bits output bus for data + address

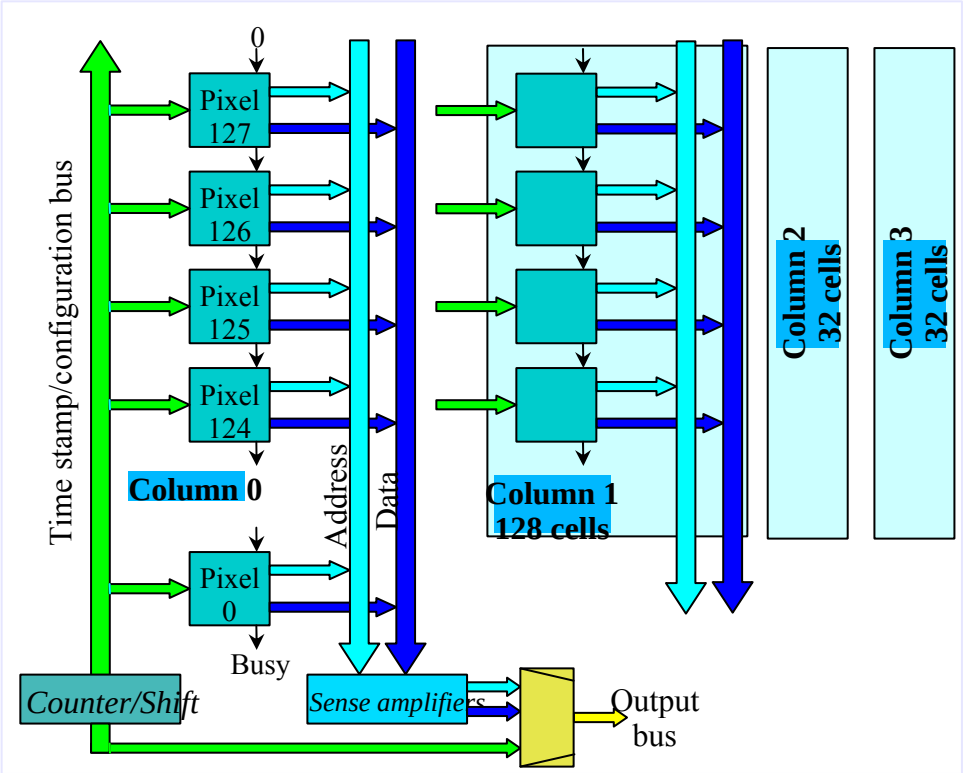




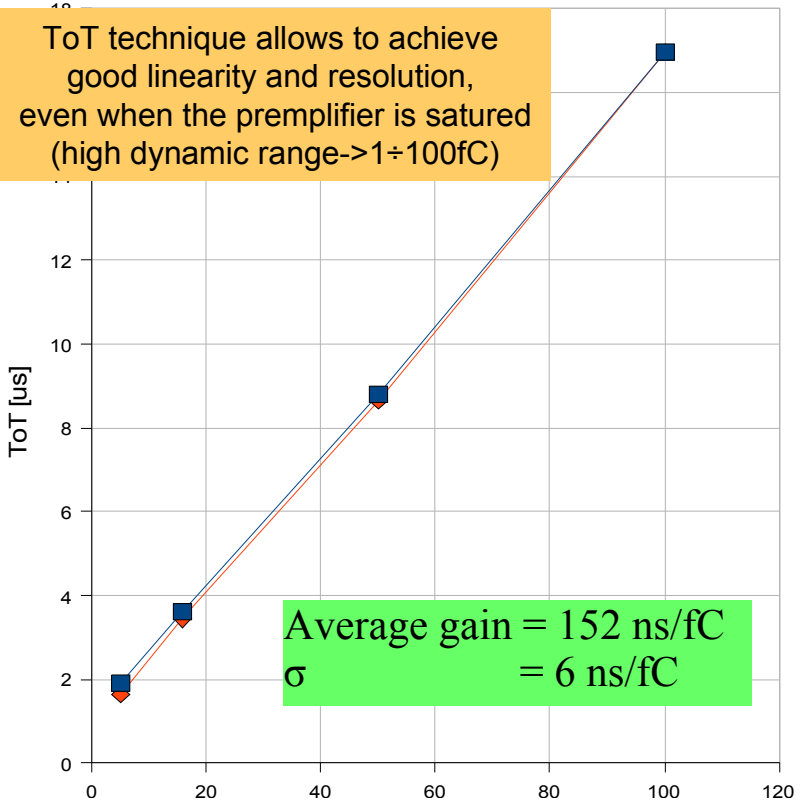


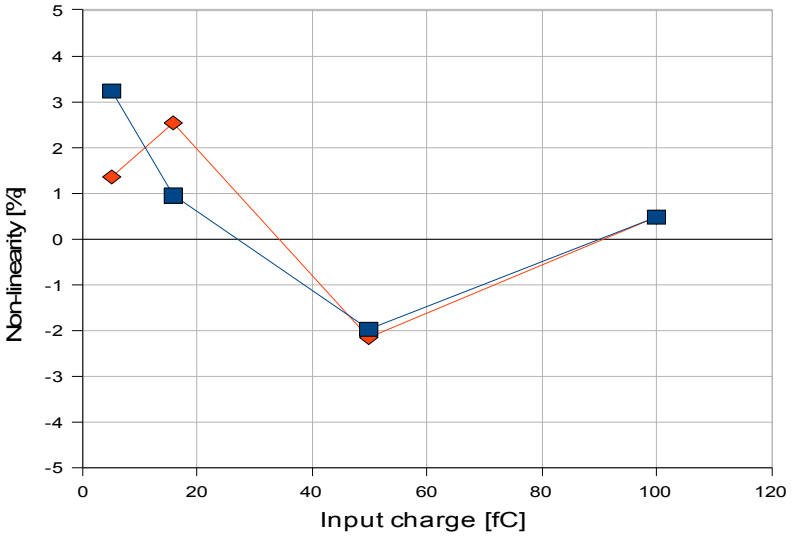
The architecture of ToPix_2



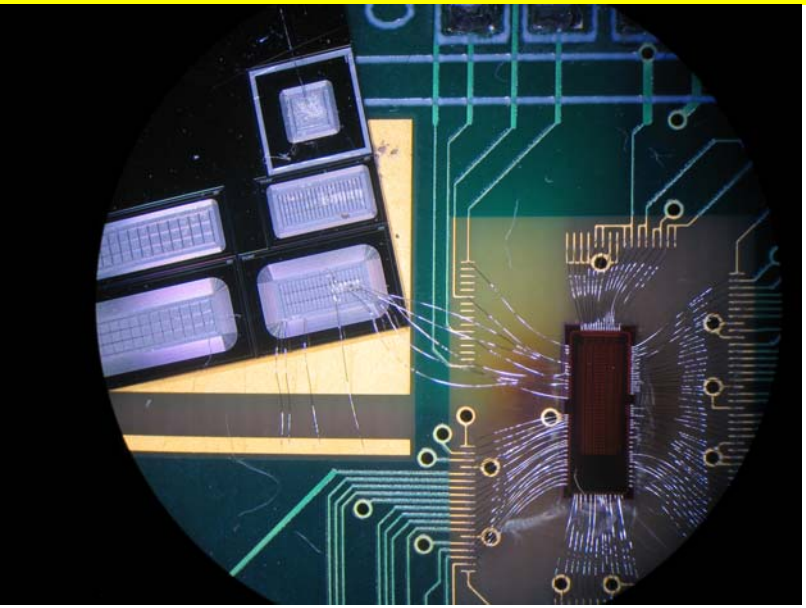


ToT technique allows to achieve good linearity and resolution, even when the premplifier is satured (high dynamic range->1÷100fC)

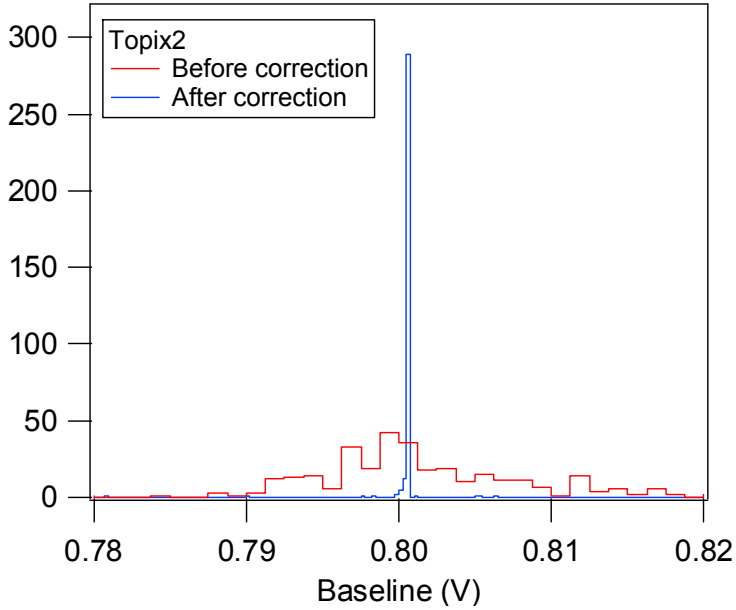




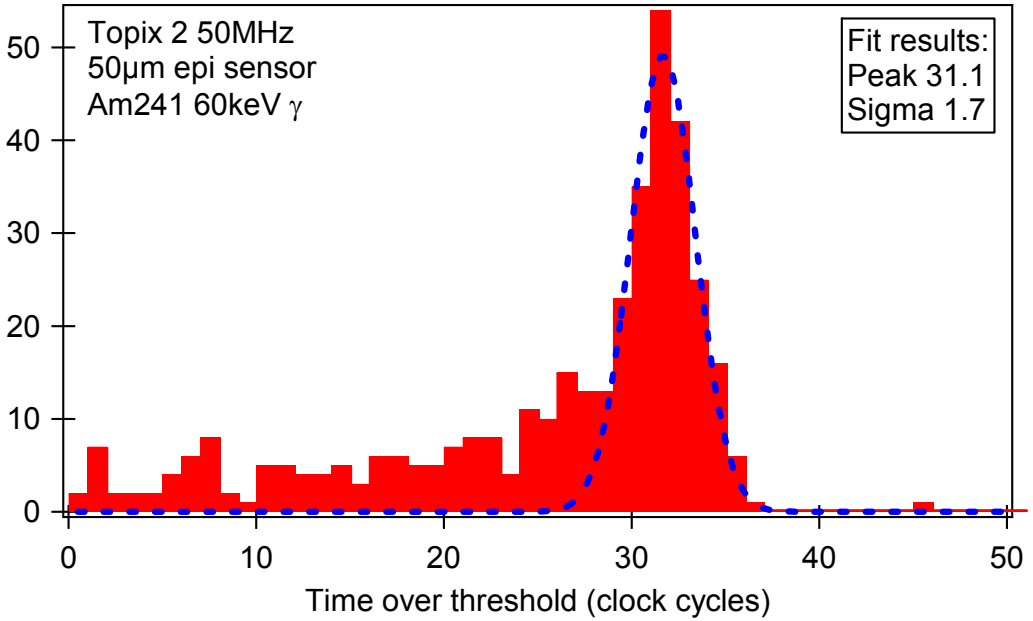
ToPix_2 and sensor



- ToPix_2 – epitaxial diode (125μm x 325μm, 50 μm thick) connection using wire bonding technique
- test with gamma rays (60 KeV) from ^{241}Am radioactive source



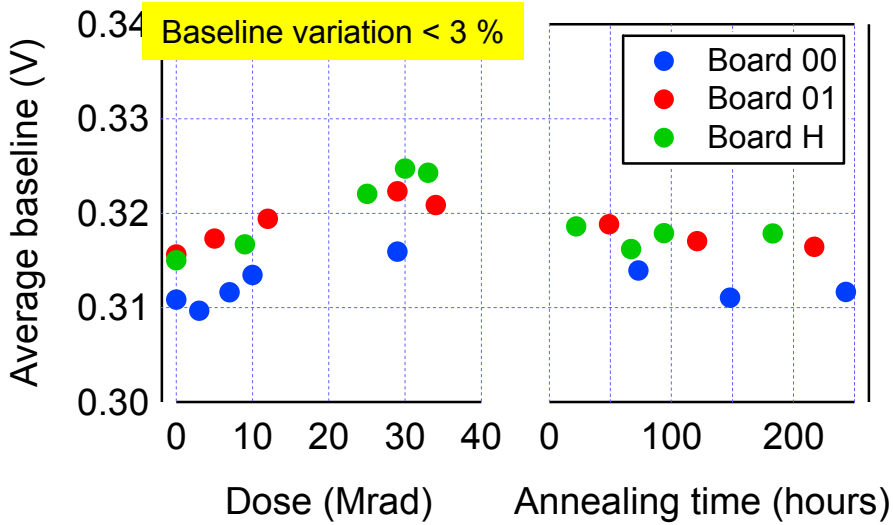
Individual pixel DAC baseline correction

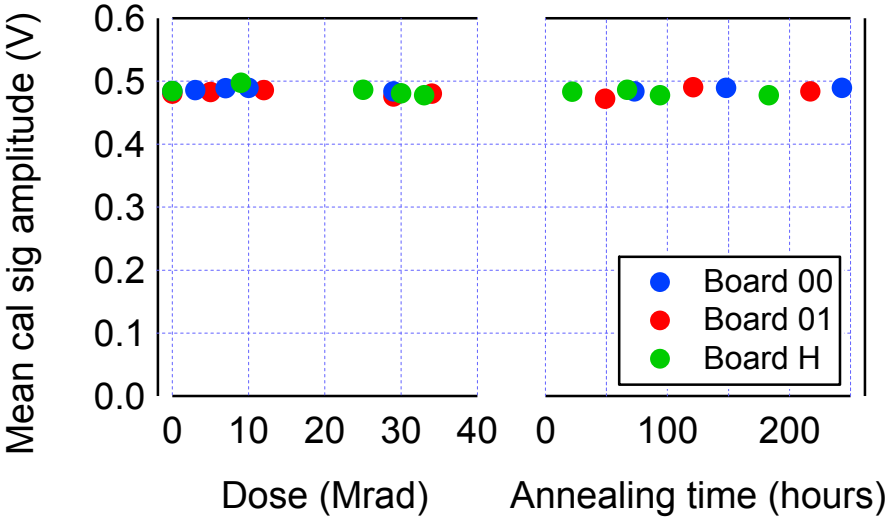


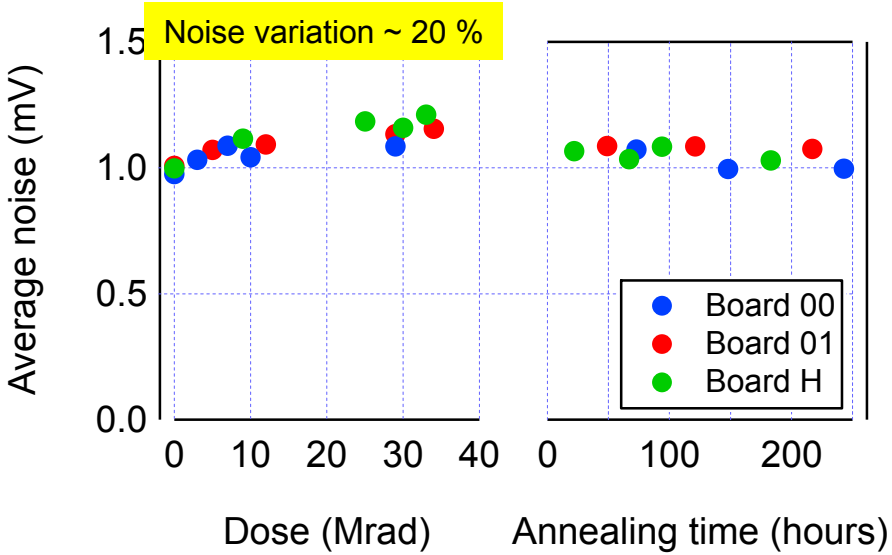
TOT calibration

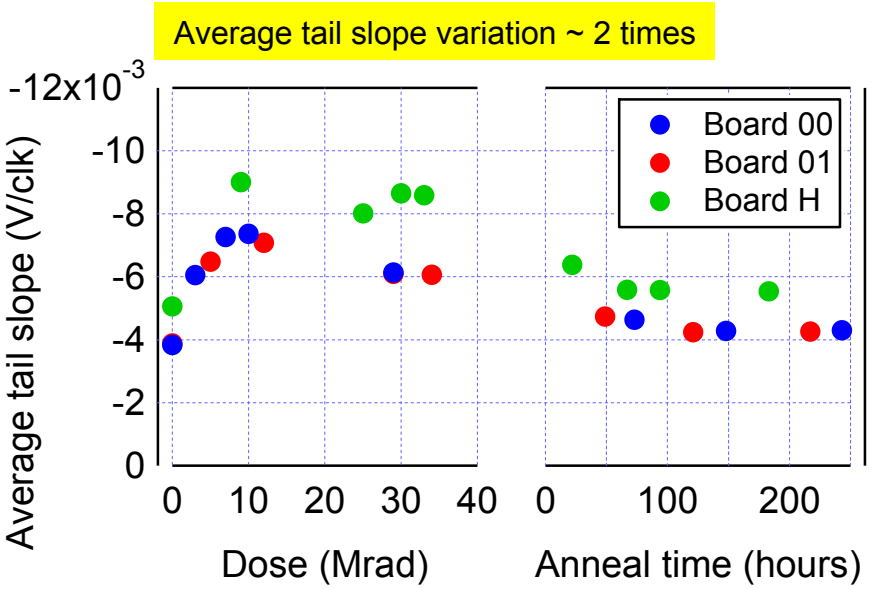
TID test on ToPix_2

Total Ionizing Dose test with the X ray source at CERN (Thanks to F. Faccio) followed by an annealing phase at 100°C



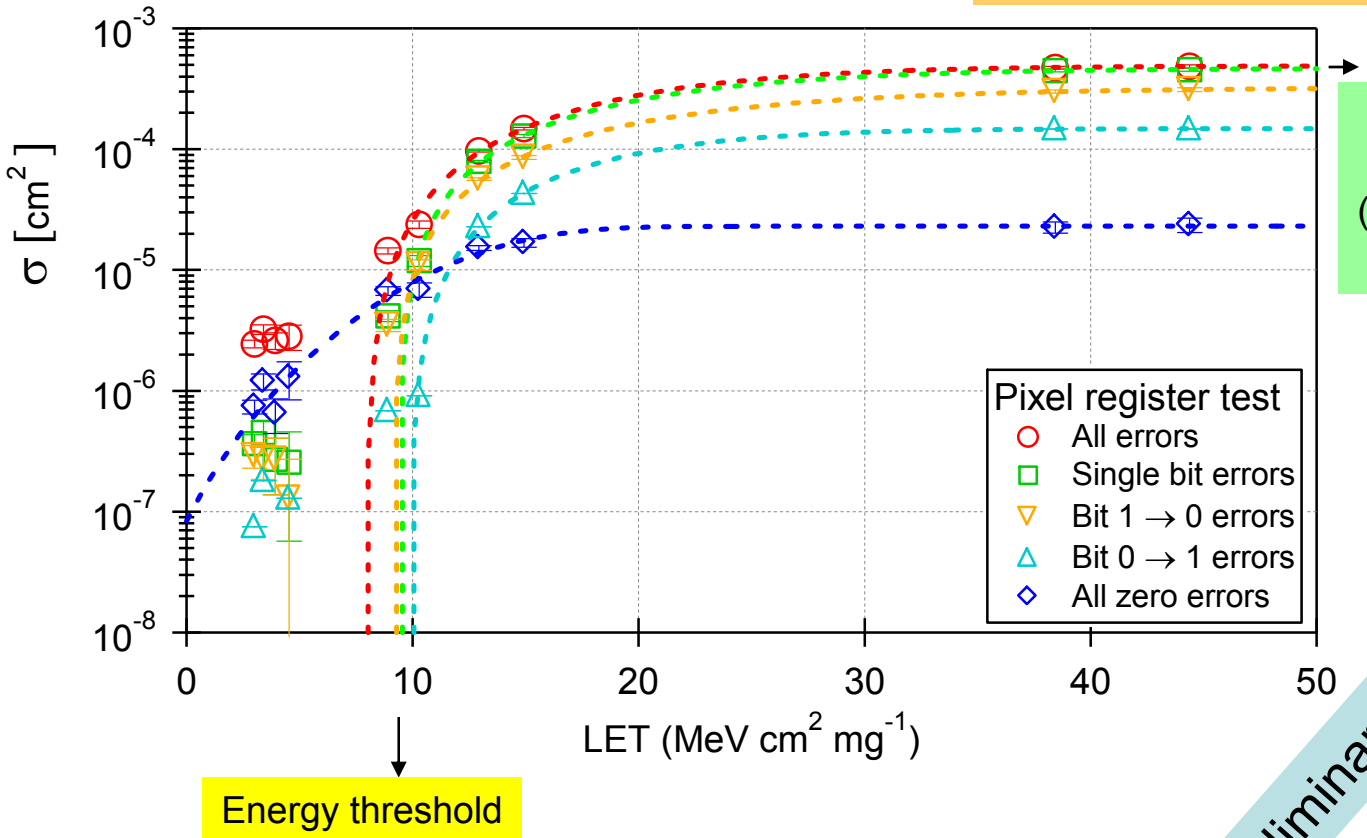






SEU test on ToPix_2

Test performed at INFN-LNL,
SIRAD facility (thanks to A. Candelori)



Saturated cross section per bit
~ $1.3 \cdot 10^{-7}$ cm²
(12 bit, 320 instances x 30 μm²)

Energy threshold

Preliminary results

Conclusions

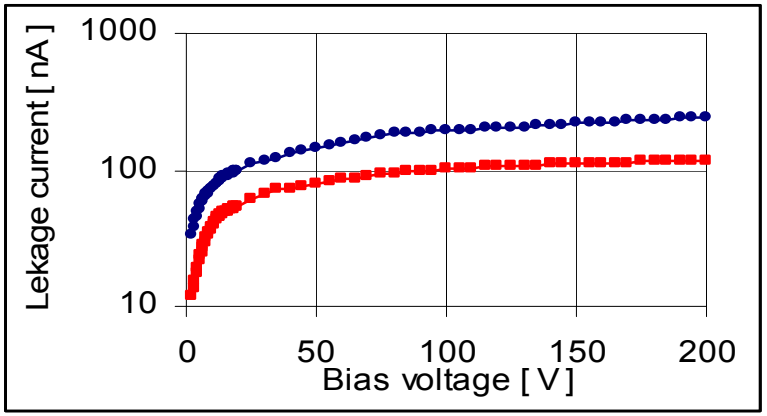
- the use of epitaxial silicon material could be very promising , also in term of radiation damage

- the tuning of the epitaxial layer resistivity, taking into account the short and long terms of annealing, has to be investigated for the full depletion voltage optimization

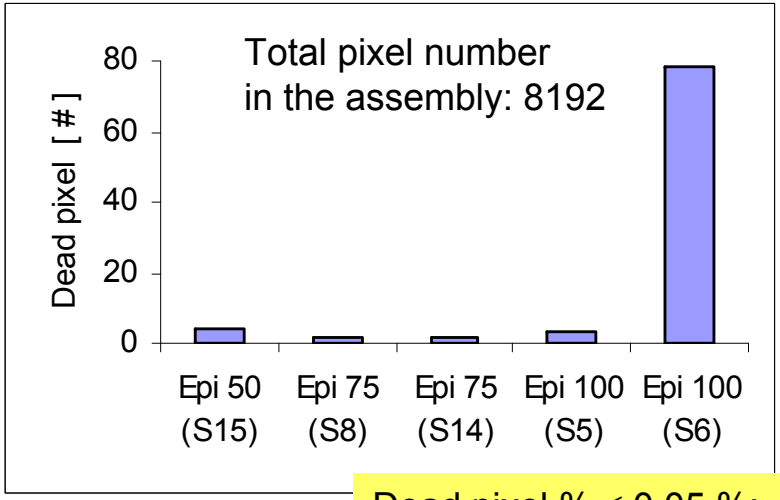
- the 130 nm CMOS technology is suitable to develop the pixel readout for:
  - limited power consumption
  - smaller pixel with many functionalities, but
    - enclosed gate layout is needed for the critical transistors of the discharge circuit
    - seu hardened cells are needed for digital part

Results from thin Si-epitaxial pixel assemblies

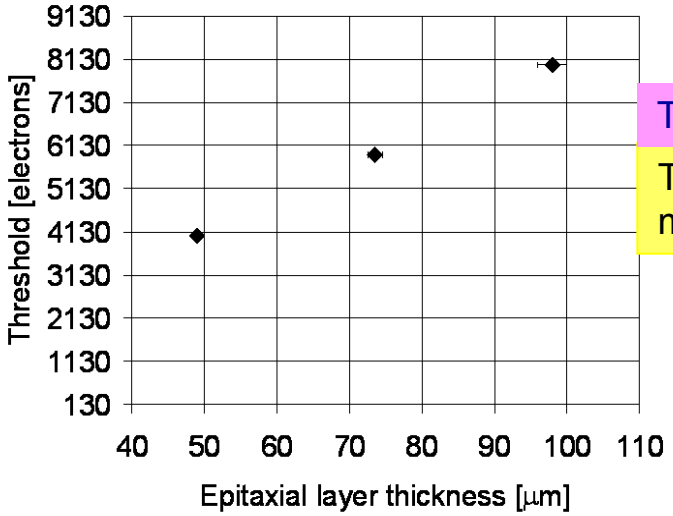
Epi 75 and Epi 50



Test performed with a ^{90}Sr source to verify the bump bonding process



Dead pixel % ≤ 0.05 %; ≤ 1% (worst case)



Test performed with a ^{90}Sr source

Threshold values in electrons corresponding to the Landau most probable value for the different epitaxial layer thicknesses

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