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Front-End Electronics for Pixel Detector of the PANDA MVD

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PANDA @ FAIR

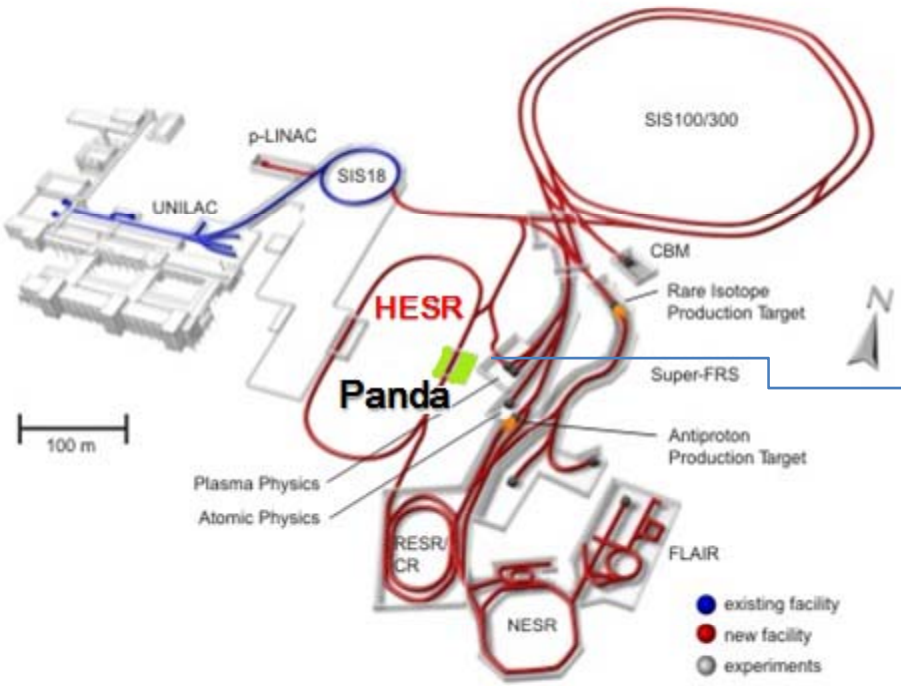
Facility for Antiproton and Ion Research

antiProton ANnihilation at DArmstadt

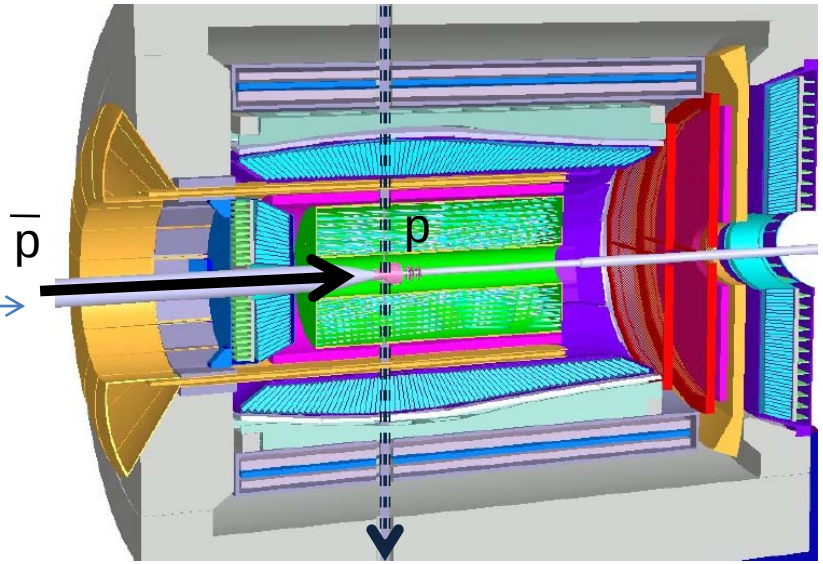
Strong Interaction Studies with Antiprotons

- charmonium spectroscopy
- glueballs and hybrids
- hadrons in nuclear matter
- open charm production
- γ-ray spectroscopy of hypernuclei

Antiproton Beam



Hydrogen Pellet Target



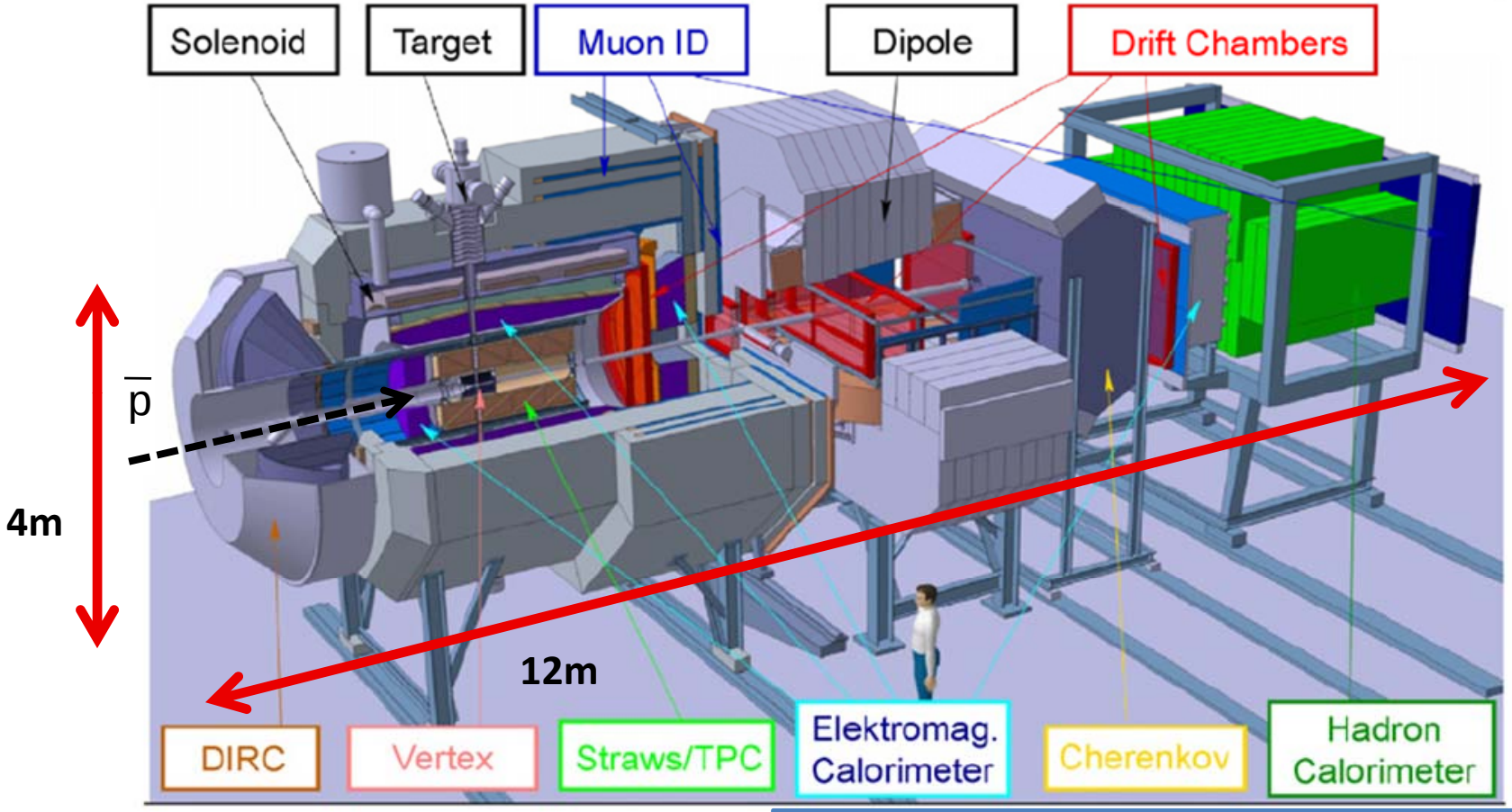
Center of mass energy: **√s = 5.5 GeV**

HESR = High Energy Storage Ring

Momentum: 1.5 GeV/c - 15 GeV/c

	Luminosity	Momentum Resolution (δp/p)
High luminosity mode	2×10^{32} cm^{-2}s^{-1}	~10^{-4} (stochastic cooling)
High resolution mode	10^{31} cm^{-2}s^{-1}	~10^{-5} (electron cooling < 8 GeV/c)

The PANDA apparatus



Target Spectrometer

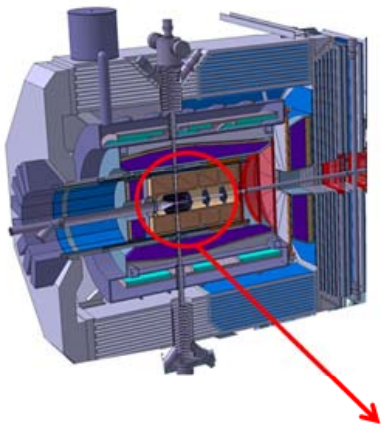
- Surrounds the interaction region

Forward Spectrometer

- With a second magnet provides coverage for the angular region below 10°.

Micro Vertex Detector

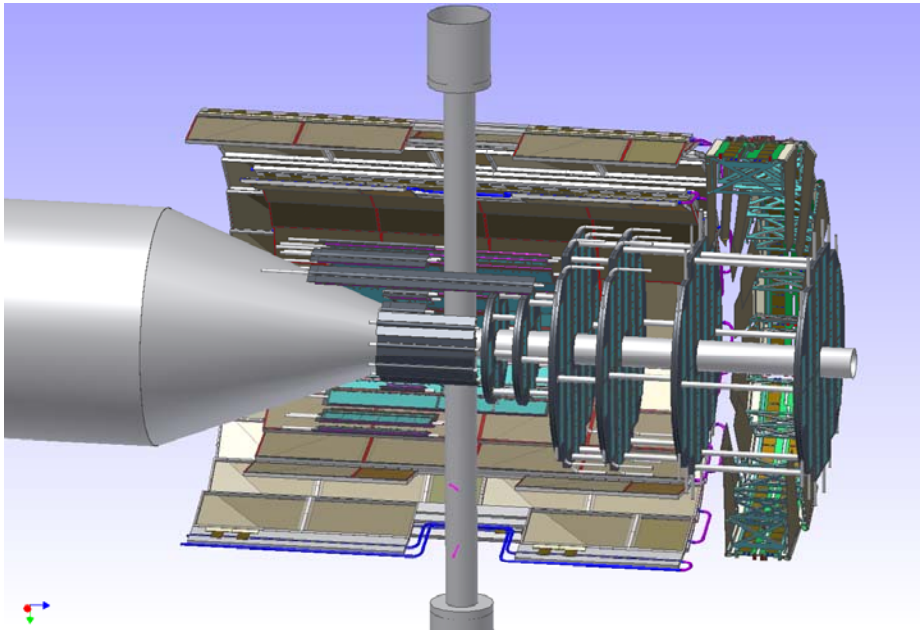
Target Spectrometer



The MVD is the closest detector to the interaction point

Primary function: vertexing.

Additional task: dE/dx information for dE up to 2.3 MeV.



- Four barrels:
  - Two Inner layers: pixels
  - Two outer layers: strip
- Six forward disks:
  - 4 pixel + 2 mixed disks.

Read-Out channels and area coverage:

- Pixels : 11M channels, 0.14 m^2.
- Strips : 70k channels, 0.5 m^2.

Specifications for the pixel detector

Pixel cell specifications	
Pixel Size	100µm x 100µm
Noise Level	< 200 e^- rms
Linear dynamic range	Up to 100fC
Power consumption	< 20µW
Input polarity	Selectable
Leakage compensation	Up to 50 nA

ASIC specifications	
Trigger	Self triggering
Active area	O(1cm^2)
Data rate	O(0.8 Gbit/s)
Radiation tolerance	10 Mrad
Simultaneous time stamping and charge measurement	
Good time resolution 6 ns rms (at 50 MHz clock) with $2 \cdot 10^7$ ann/s	

A custom solution for the readout of the pixel detector is motivated by the high track density (up to 12.3 M hit/(s cm²)) and the absence of a trigger signal.

Technology: CMOS 130nm

Time Over Threshold

The Time over Threshold (ToT) technique permits to measure a charge by measuring the time needed to discharge it with a constant current (I_{dis}).

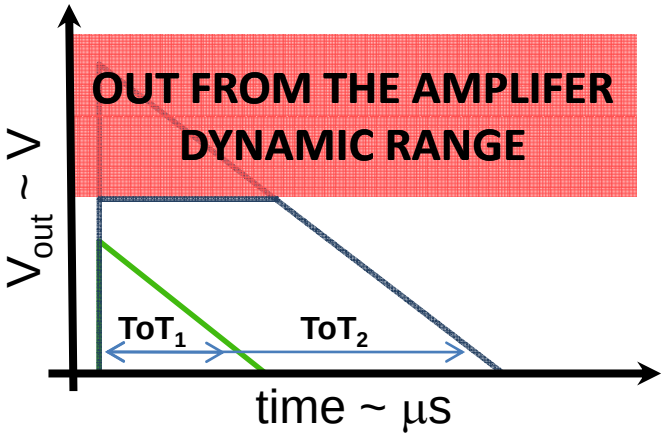
$$v_{out}(t) = \frac{Q_{in}(t)}{C_f} = \frac{1}{C_f}\int_0^t (I_{in}(t') - I_{dis}(t'))\,dt'$$

Since the charge injection time is 10^3 smaller than the discharging time:

$$Q_{inj} = \int_0^{\epsilon} I_{in}(t')\,dt' \qquad v_{out}(t) = \frac{Q_{inj} - I_{dis}\,t}{C_f}$$

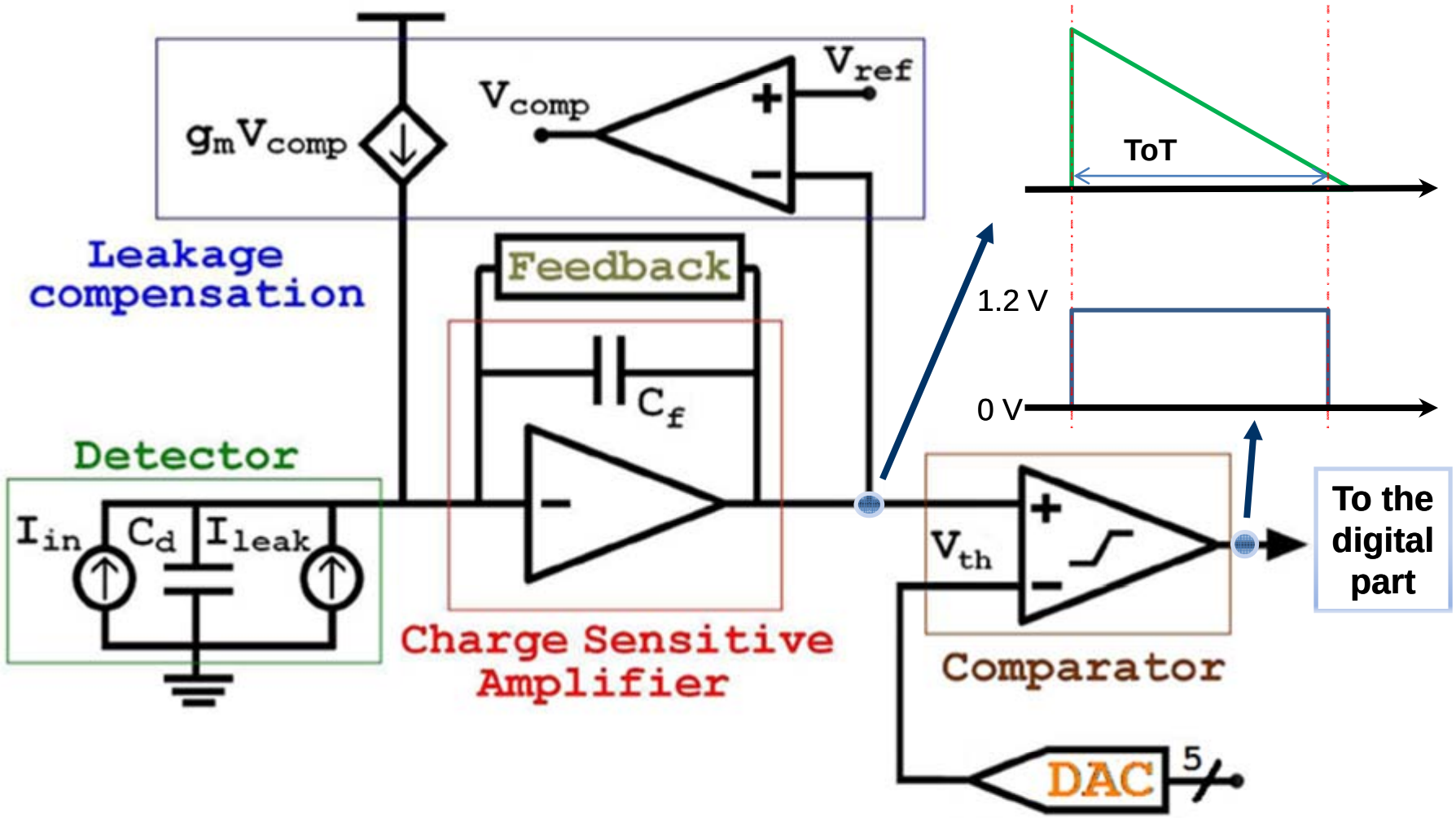
$$v_{out}(ToT) = \frac{Q_{inj} - I_{dis}\,ToT}{C_f} = 0 \rightarrow \boxed{ToT = \frac{Q_{inj}}{I_{dis}}}$$

The ToT allows to achieve good linearity and excellent resolution even when the preamplifier is saturated, thus making room for an high dynamic range.



Analog Front-End

The Analog Front-End generates a pulse whose width is proportional to the injected charge by the sensor.



Charge sensitive amplifier

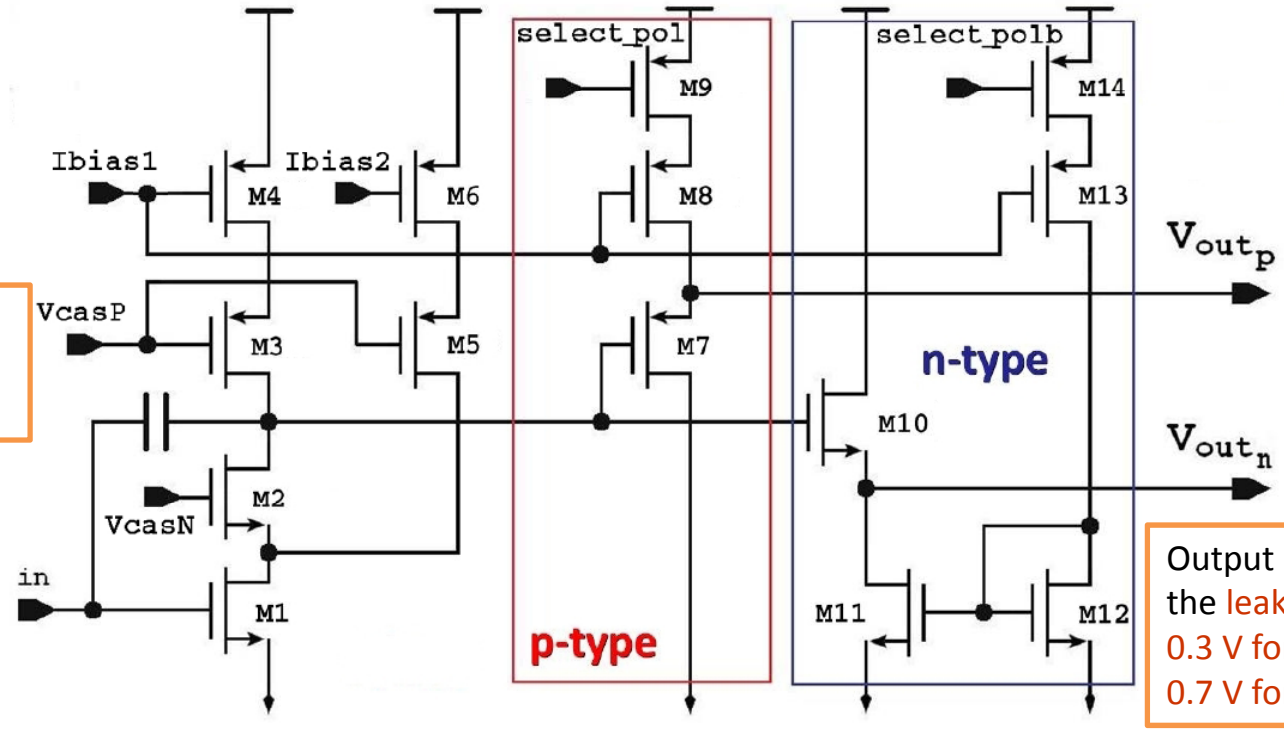
Input stage:

- integrator realized by a direct cascode amplifier with capacitive feedback.

Output stage:

- source follower with selectable polarity in order to maximize the output dynamic range.

DC level fixed by transistor bias: 0.2 V



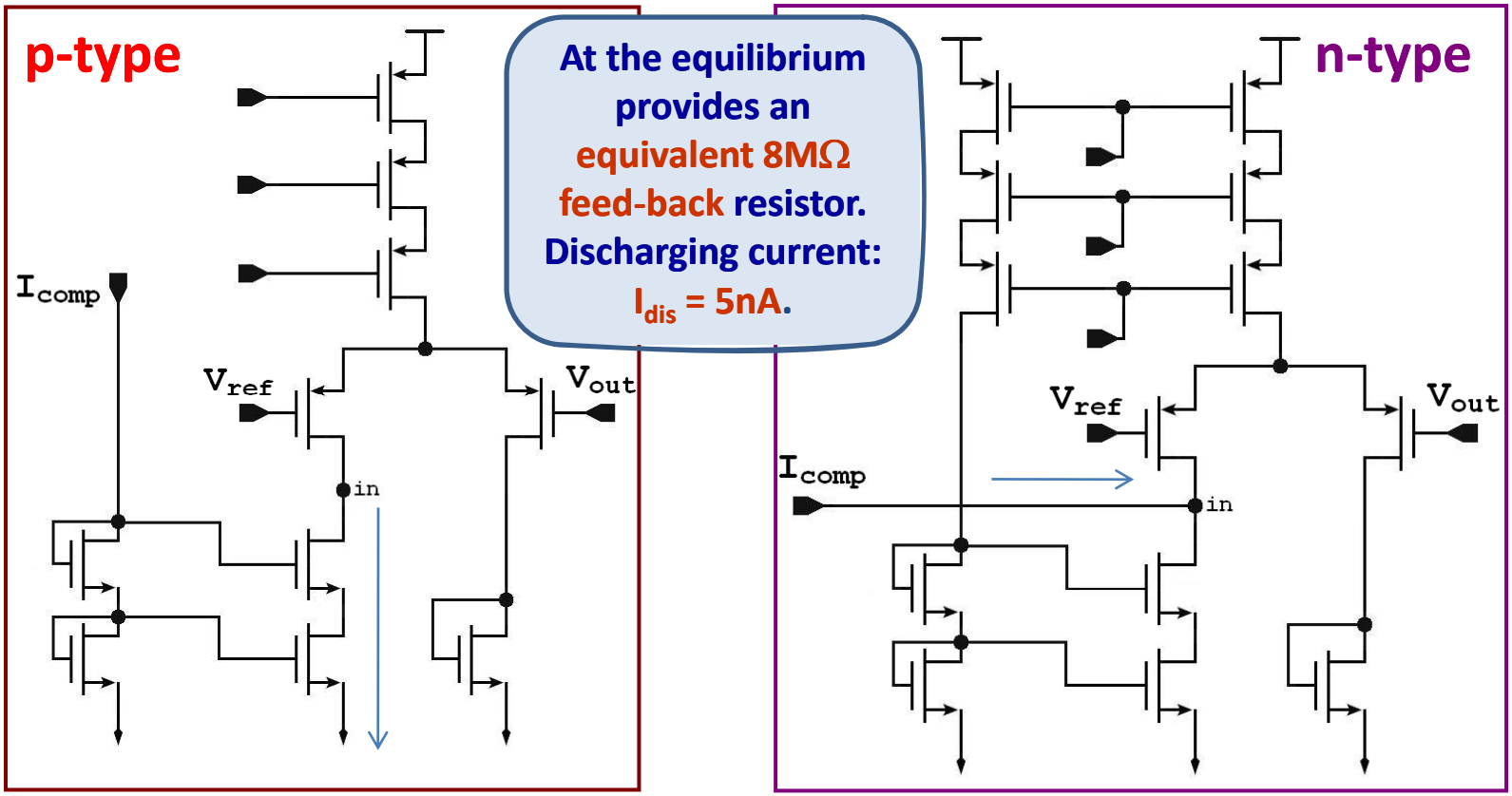
Output DC level regulated by the leakage compensation: 0.3 V for n-type sensor, 0.7 V for p-type sensor.

Current: 2µA in the input device, 1 µA in the source follower.

Feedback circuit

It keeps the output at the reference voltage, discharging the charge deposited on the input node.

This stage provides also the injection of the leakage compensation current at the input node.



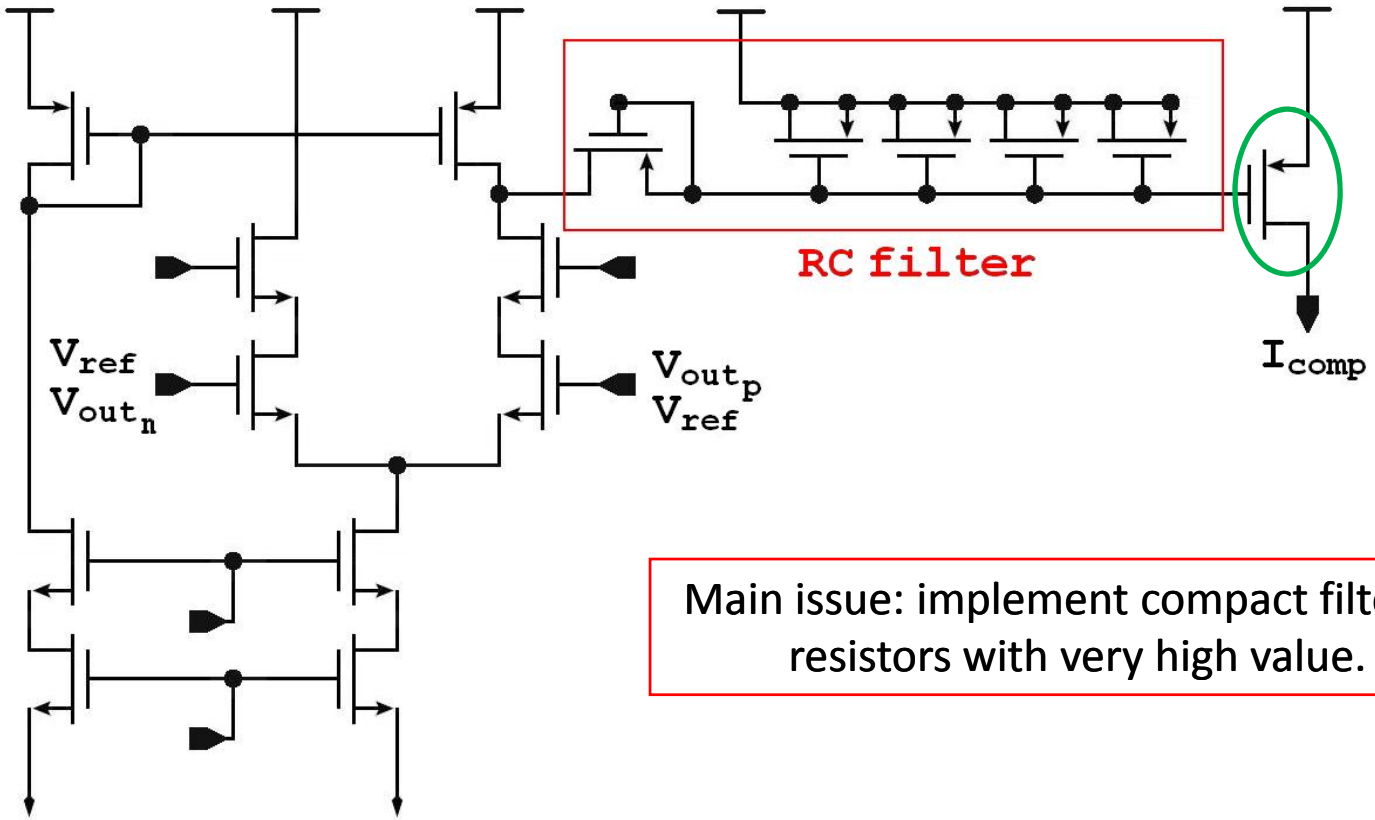
Compensation current injected trough current mirror

Compensation current injected directly

Leakage current compensation

The leakage current may be up to 50nA → It has to be compensated to avoid an output voltage offset.

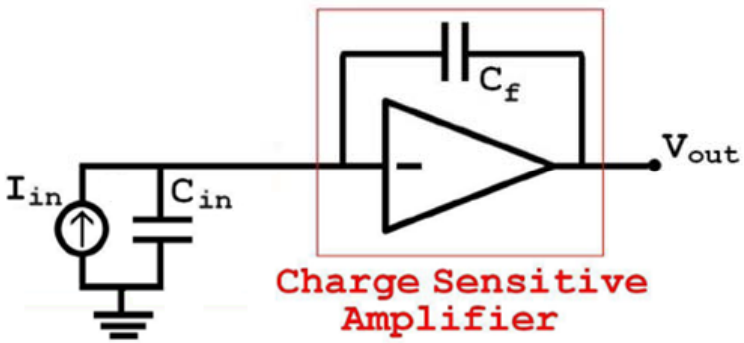
ToT signals can be very long (up to 20us) → In order to preserve the signal a very low cutoff frequency (≈ 10 Hz) is required.



PMOS that injects the compensation current at the input node

Main issue: implement compact filtering resistors with very high value.

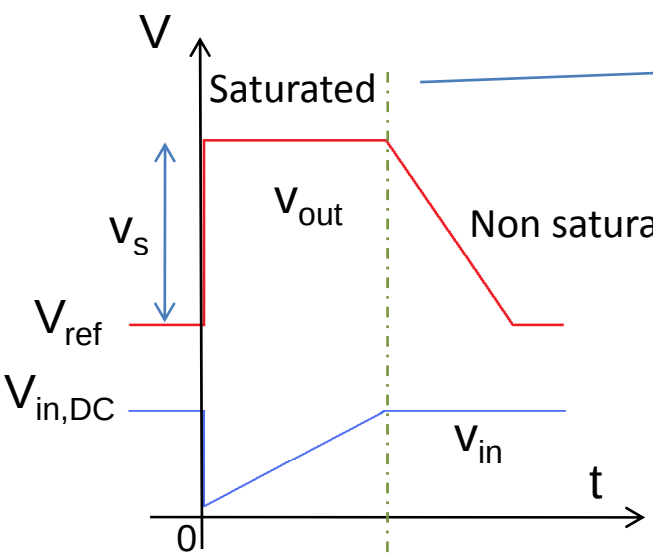
Linear mode and Saturated mode



Core amplifier	Signal charge integration
Non saturated	on the feedback capacitor C_f
Saturated	on the input capacitor C_{in}

C_{in} = 200 fF
C_f = 24 fF

Charge gain in linear mode:
$V_{out}/Q_{in} = 1/C_f$ = 41.7 mV/fF



$$\begin{cases} v_{out}(t) = v_s \\ v_{in}(t) = -\dfrac{Q_{inj} - v_s C_f - I_{dis}\, t}{C_{in}} \end{cases}$$

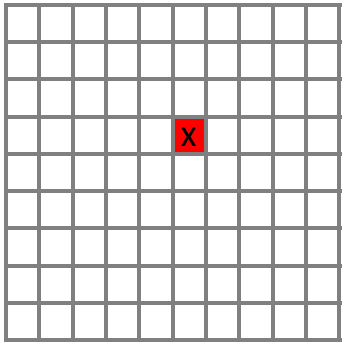
$$\begin{cases} v_{out}(t) = \dfrac{Q_{inj} - I_{dis}\, t}{C_f} \\ v_{in}(t) = 0 \end{cases}$$

Saturation and Cross Talk (1)

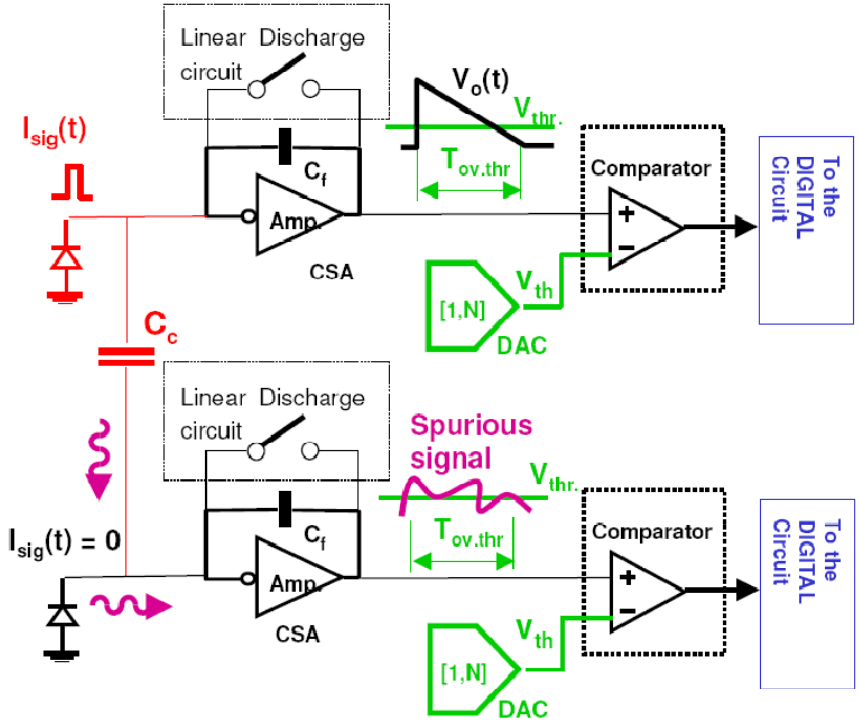
Due to the inter-pixel capacitance a voltage signal at the input of one channel induces a spurious signal at the input of the adjacent pixel.

When the preamplifier saturates the input node is no more a virtual ground and the cross-talk effect turn up.

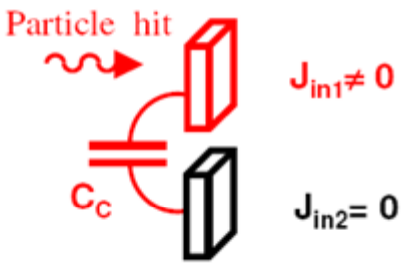
Pixel Matrix



X Hit event
No hit event



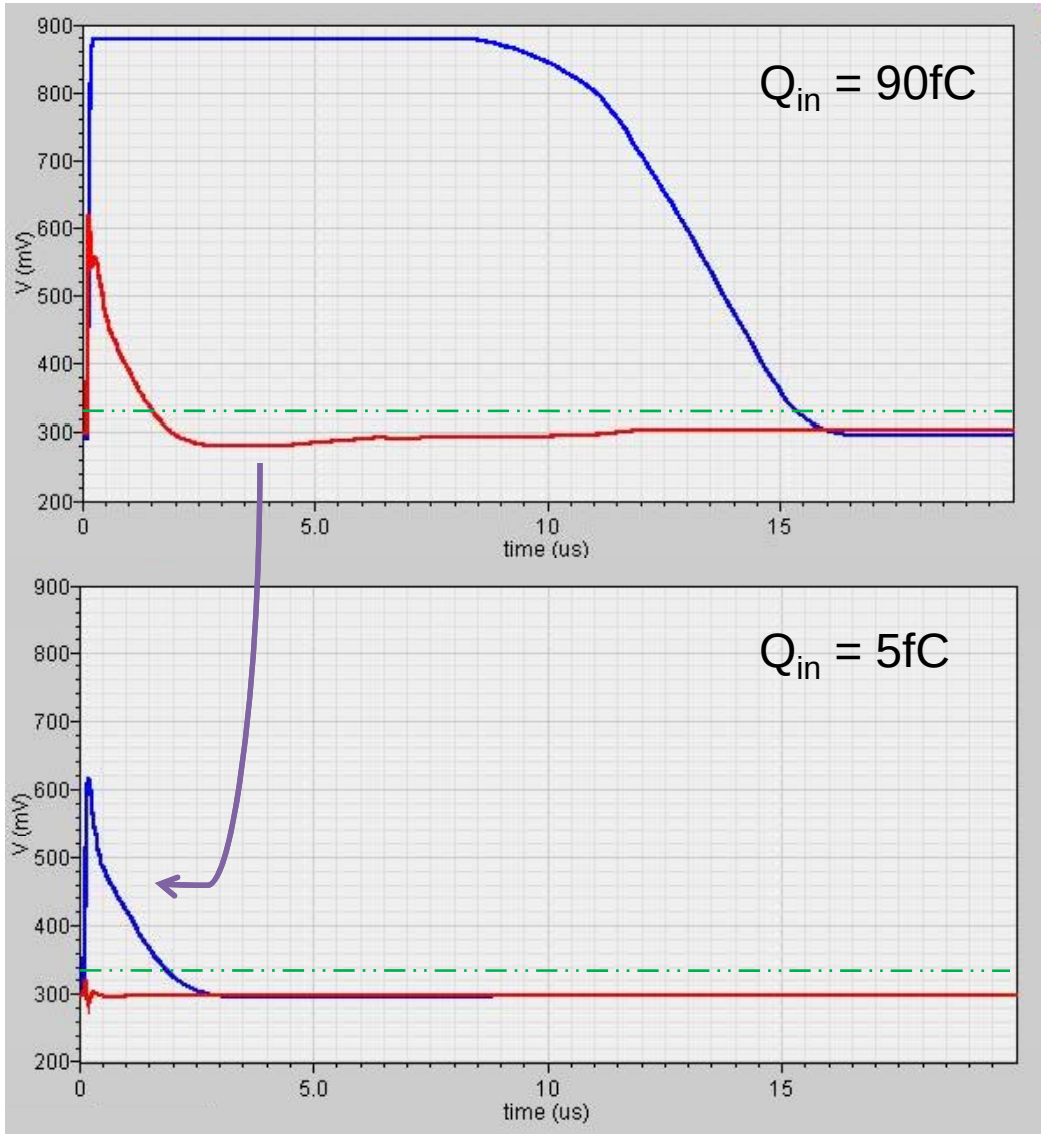
Adjacent Coupled Detectors



Saturation and Cross Talk (2)

Saturated

Non saturated

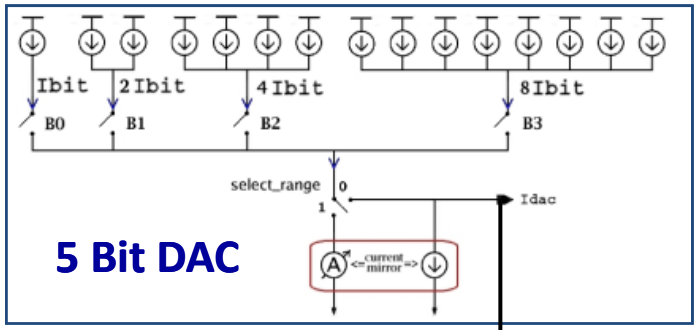


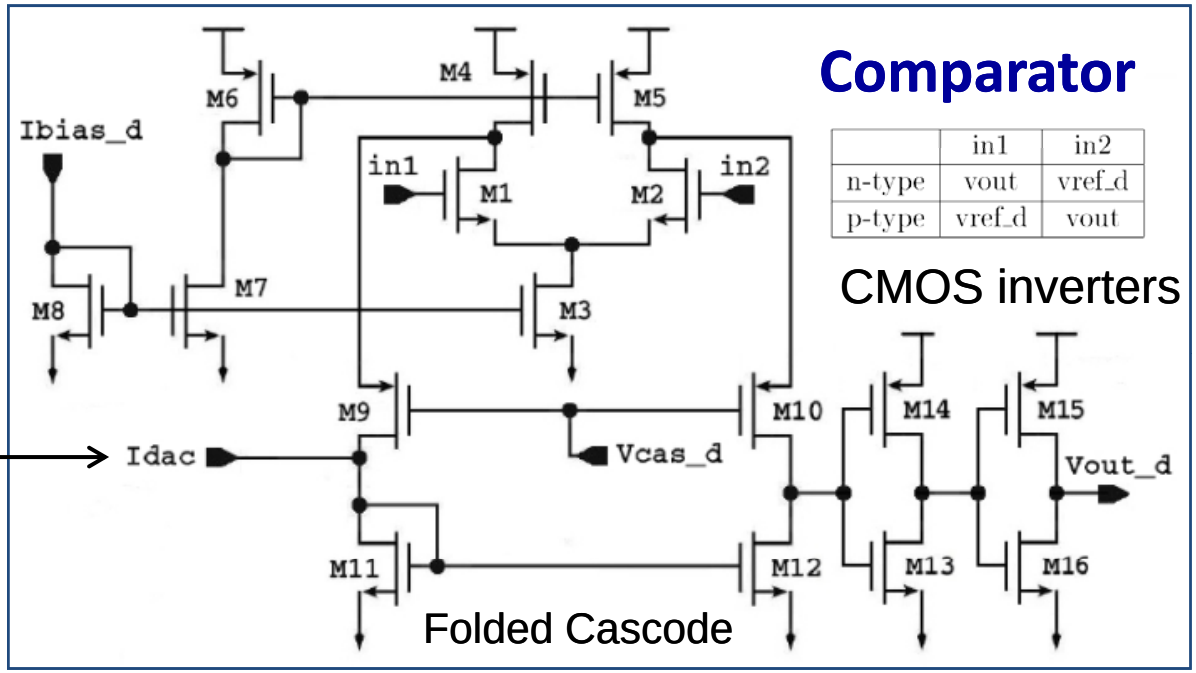
Simulation done by a inter-pixel coupling capacitance:
C_c = 100fF

Pixel readout channel output

- Hit signal
- Spurious signal

Comparator

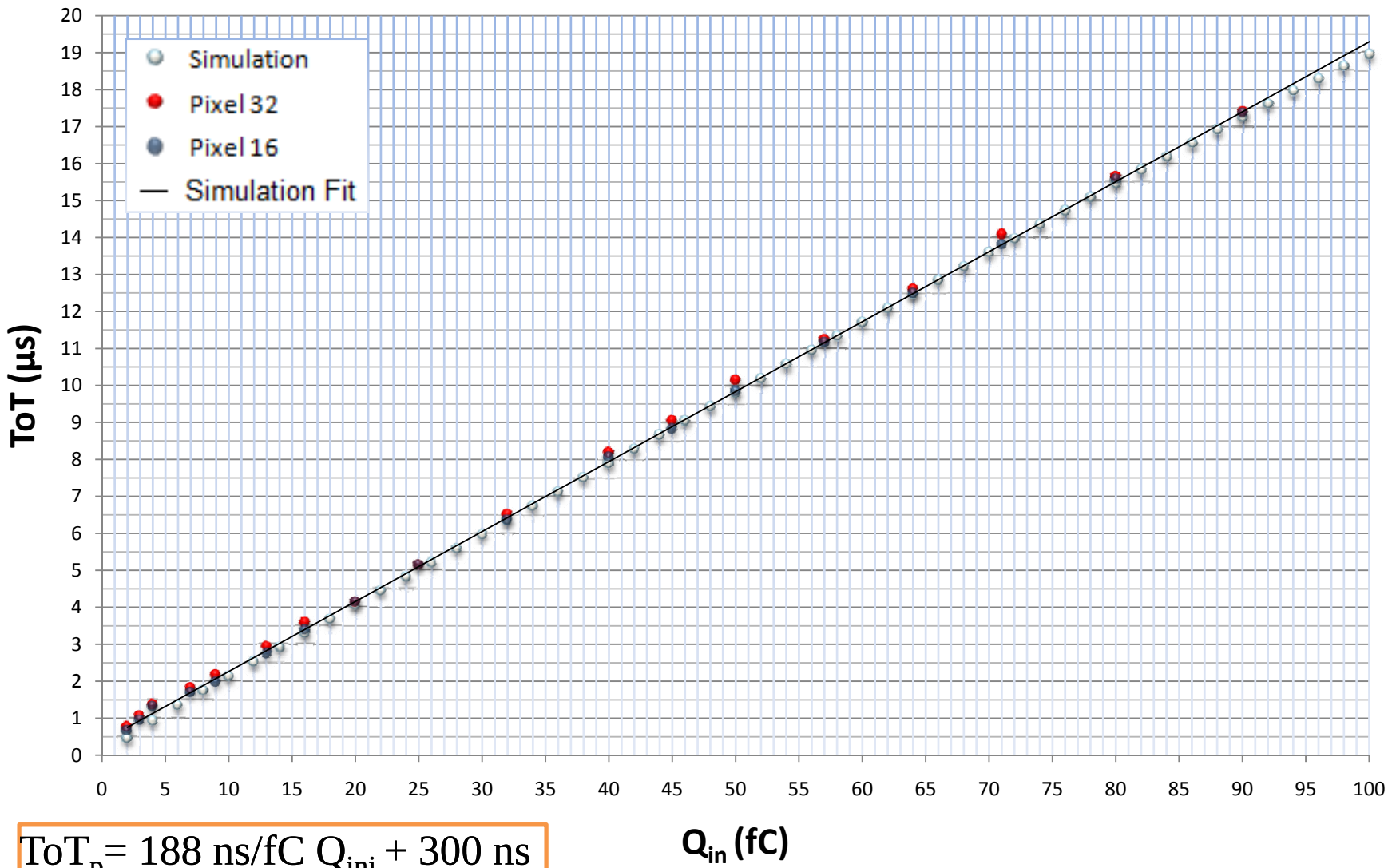




To mitigate the threshold dispersion a local five bit DAC is added in each pixel, to allow a fine tuning of the threshold on a pixel by pixel basis:

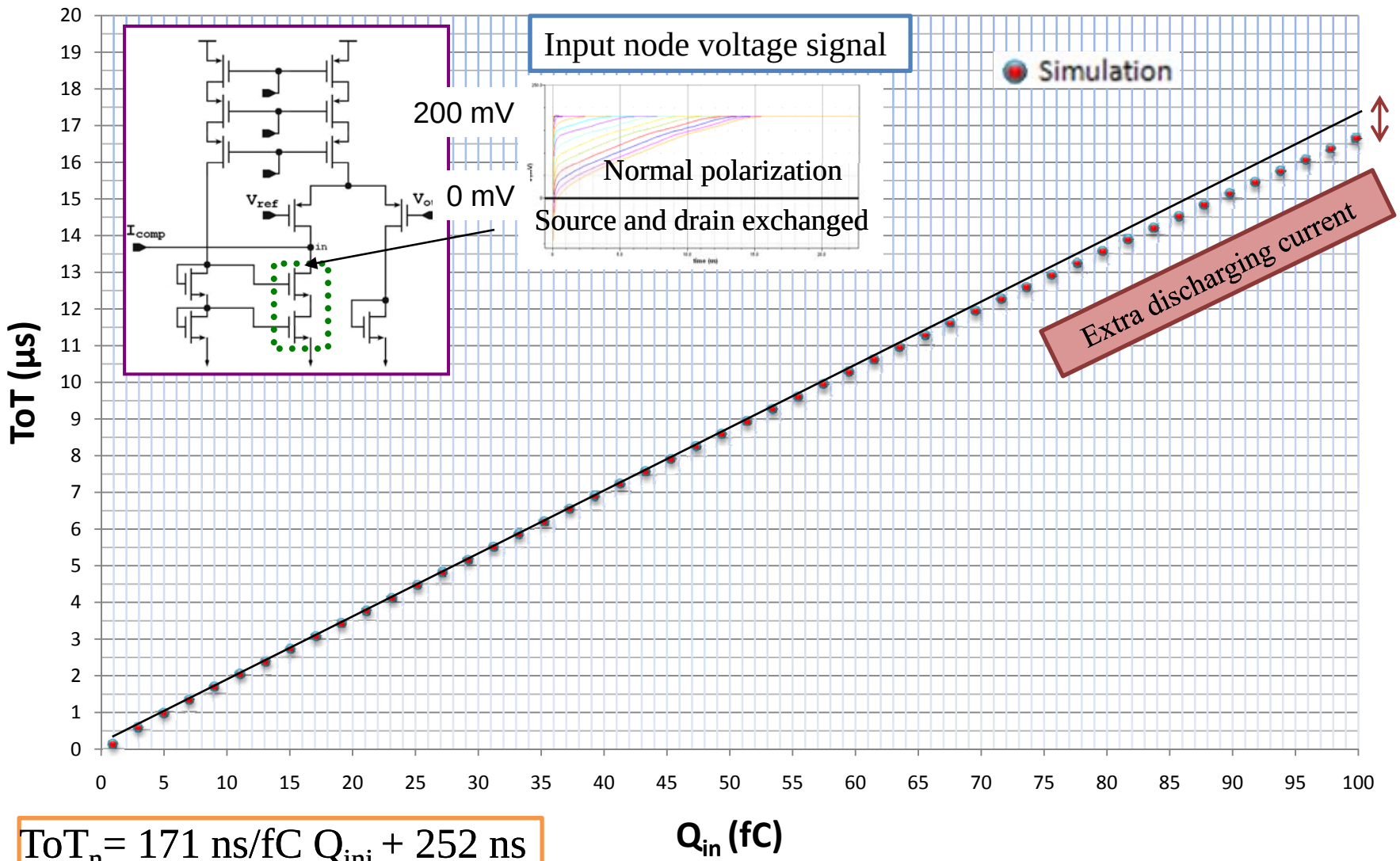
- DAC can sink or source current to a low impedance node: 4+1 bit operation.
- DAC full scale range depends on external biasing.

P-Type sensors ToT Linearity



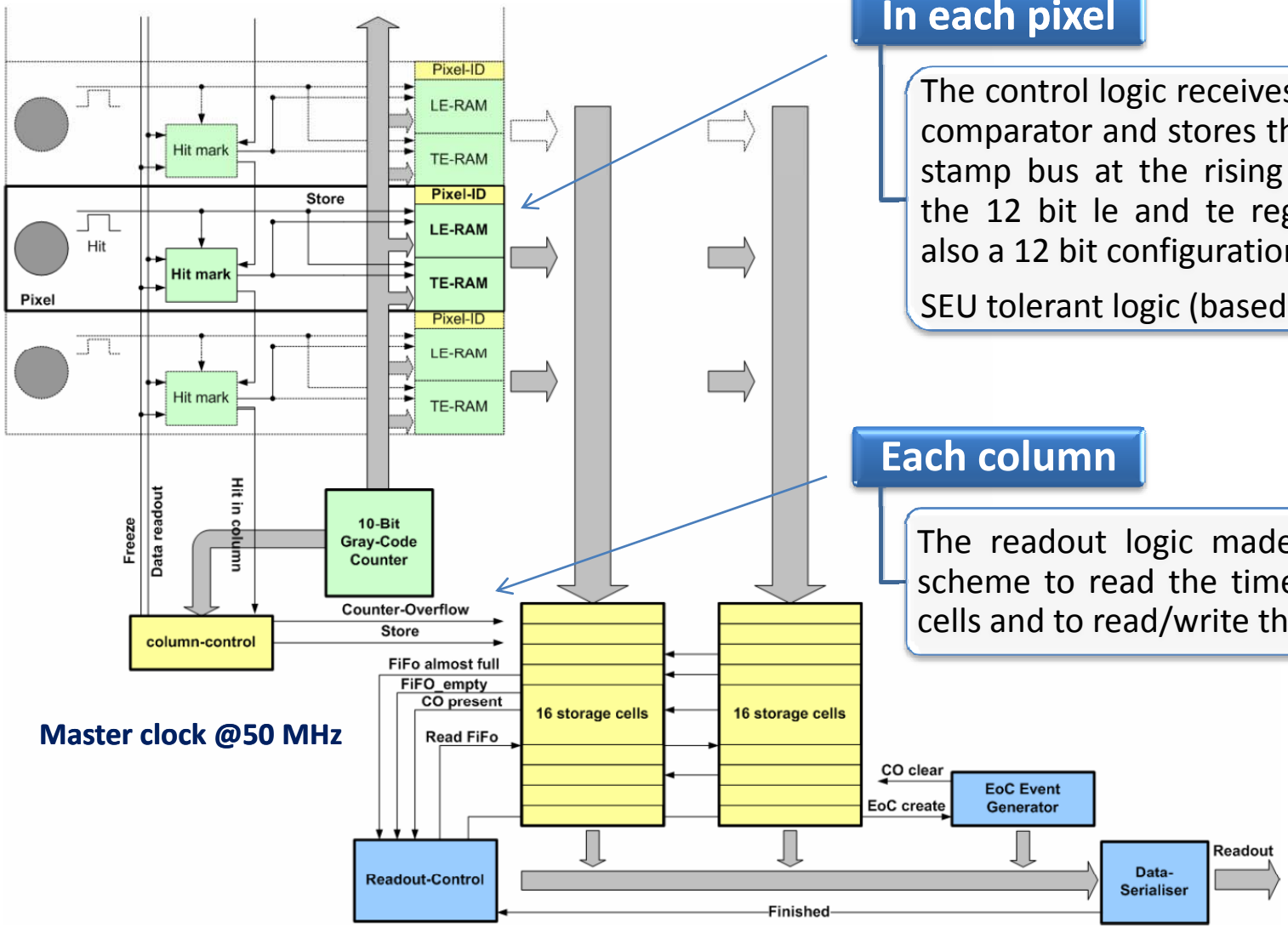
$ToT_p = 188\ ns/fC\ Q_{inj} + 300\ ns$

N-Type sensors dynamic Range



$ToT_n = 171\ ns/fC\ Q_{inj} + 252\ ns$

Digital Read Out



Master clock @50 MHz

In each pixel

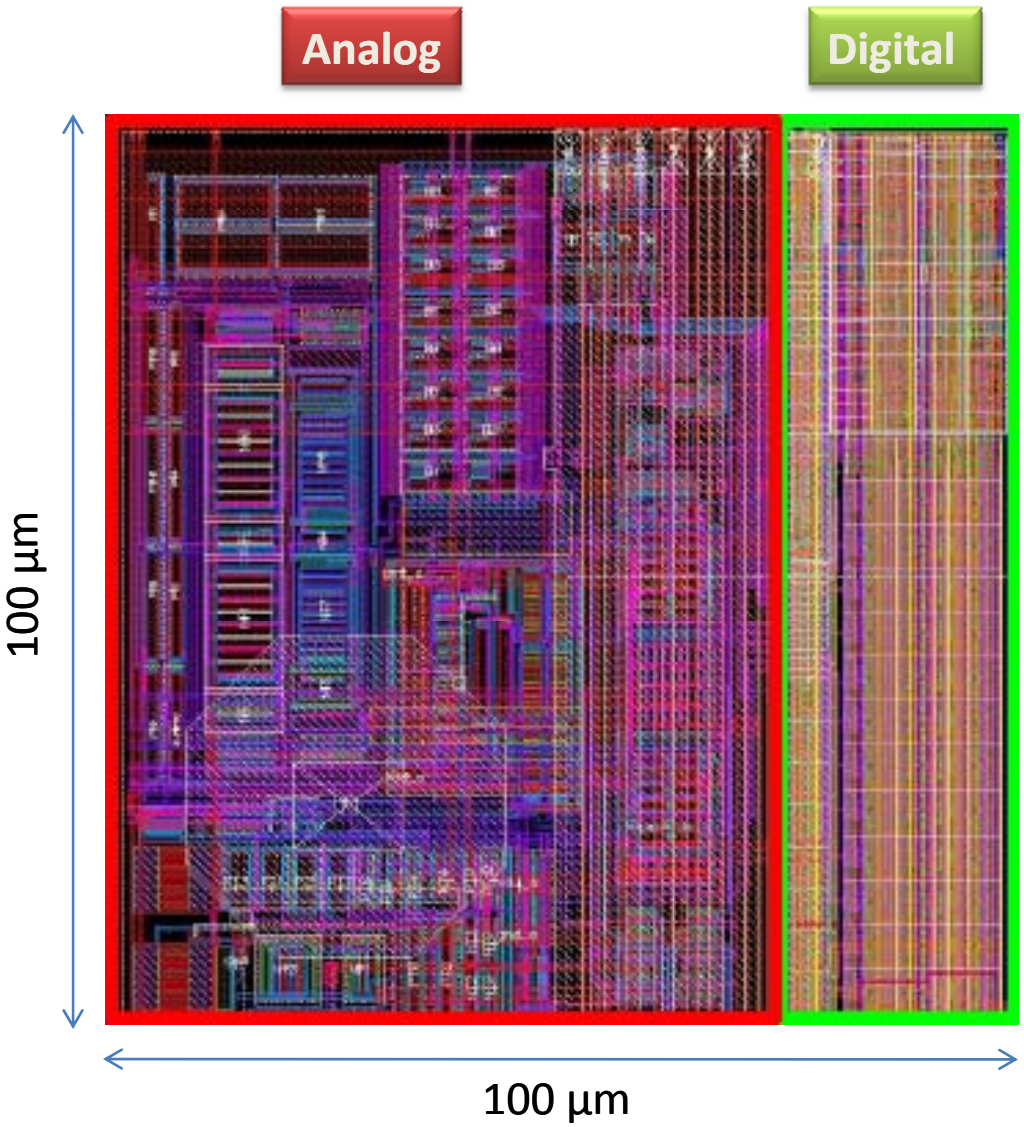
The control logic receives the signal from the comparator and stores the value on the time stamp bus at the rising and falling edge in the 12 bit le and te registers. It is present also a 12 bit configuration register.

SEU tolerant logic (based on the DICE cell)

Each column

The readout logic made in a fixed priority scheme to read the timestamps of the pixel cells and to read/write the configuration bits.

Pixel Layout



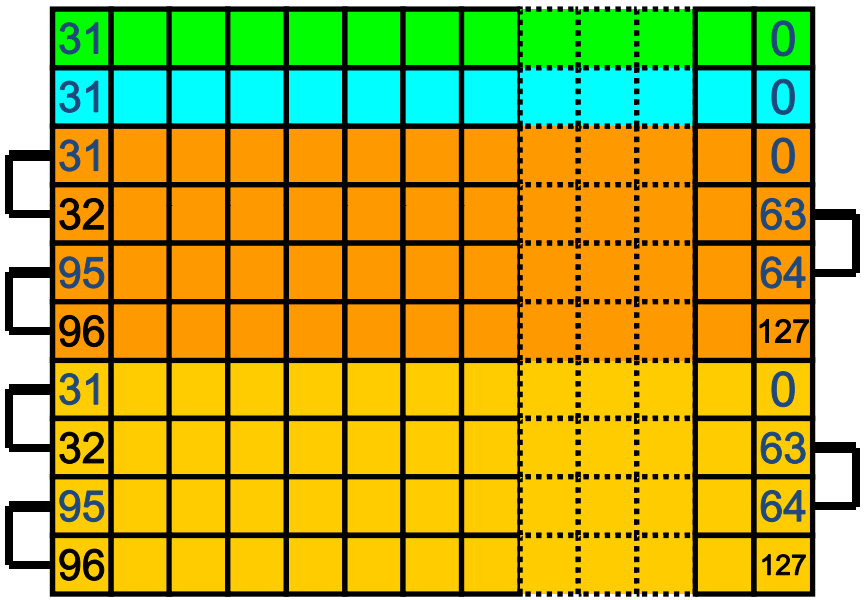
Each cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information.

Single Pixel Power dissipation of 15 µW from a 1.2 V power supply.

ToPix 2.0

ToPix 2.0 is a reduced scale prototype chip for the hybrid pixel sensors.

It has been designed in a CMOS 0.13 µm technology **and successfully tested.**



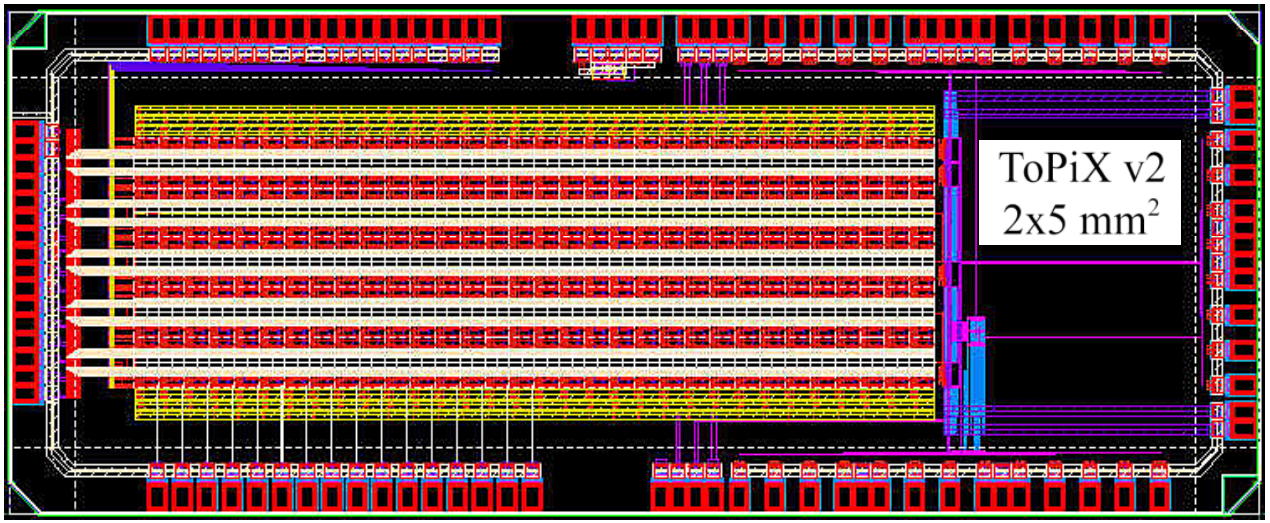
It has 320 pixel cell in four columns:

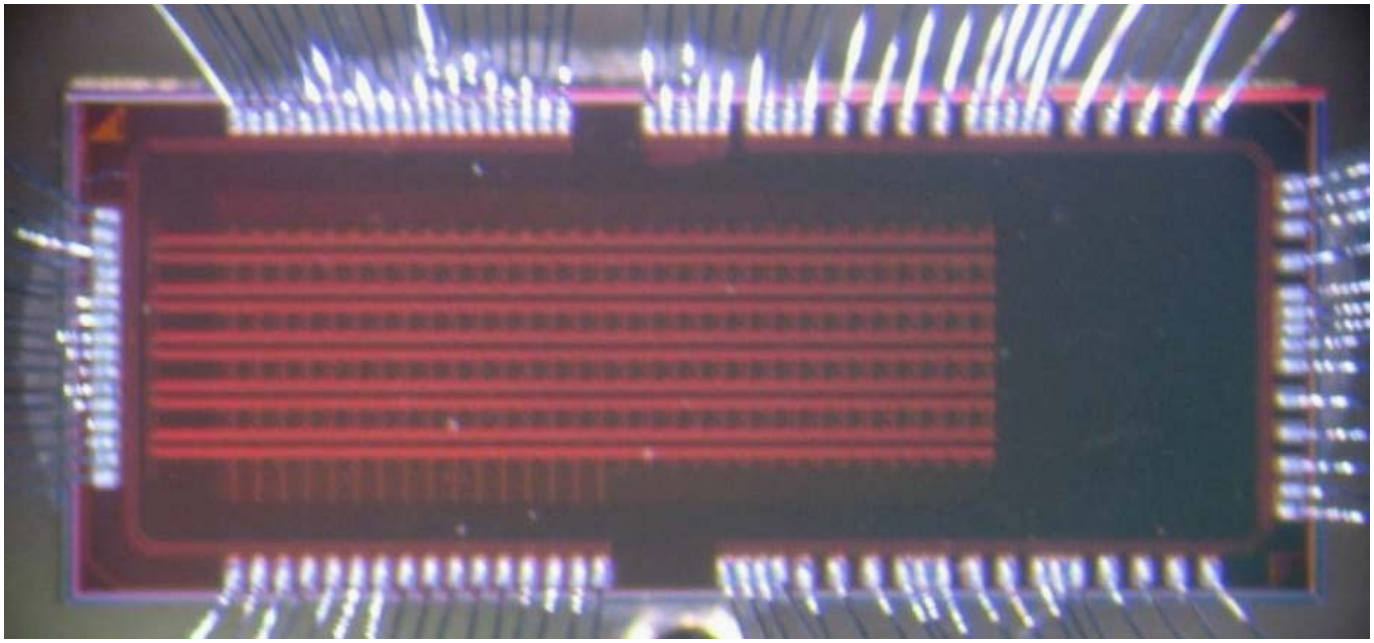
- Two short columns with 32 pixels.
- Two folded column with 128 pixels.

- Simplified end-of-column logic.
- Sixteen pixels with wire bonding pad.

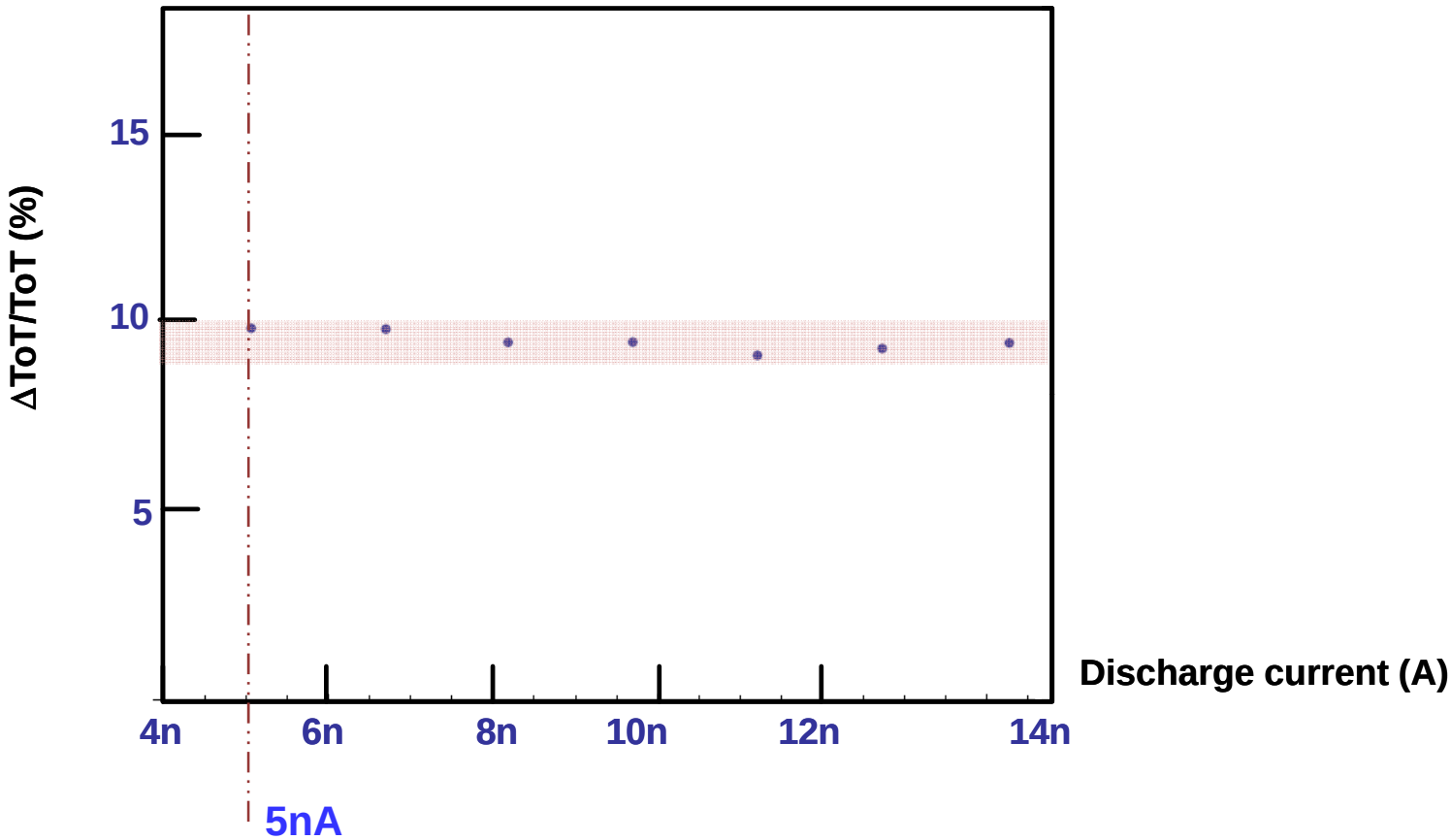
The final version of ToPiX will consist of a matrix of 116x110 cells with a pixel size 100 µmx100 µm, thus covering a 1.27 cm^2 active area.

ToPix 2.0 – Layout and Photo





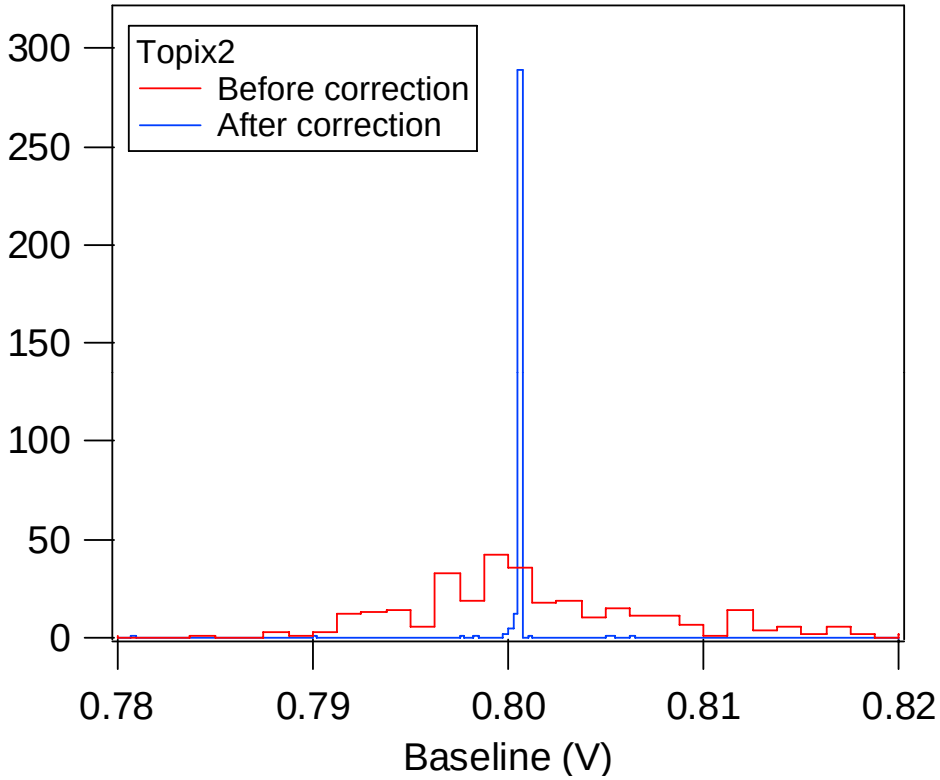
Measure: ToT uniformity

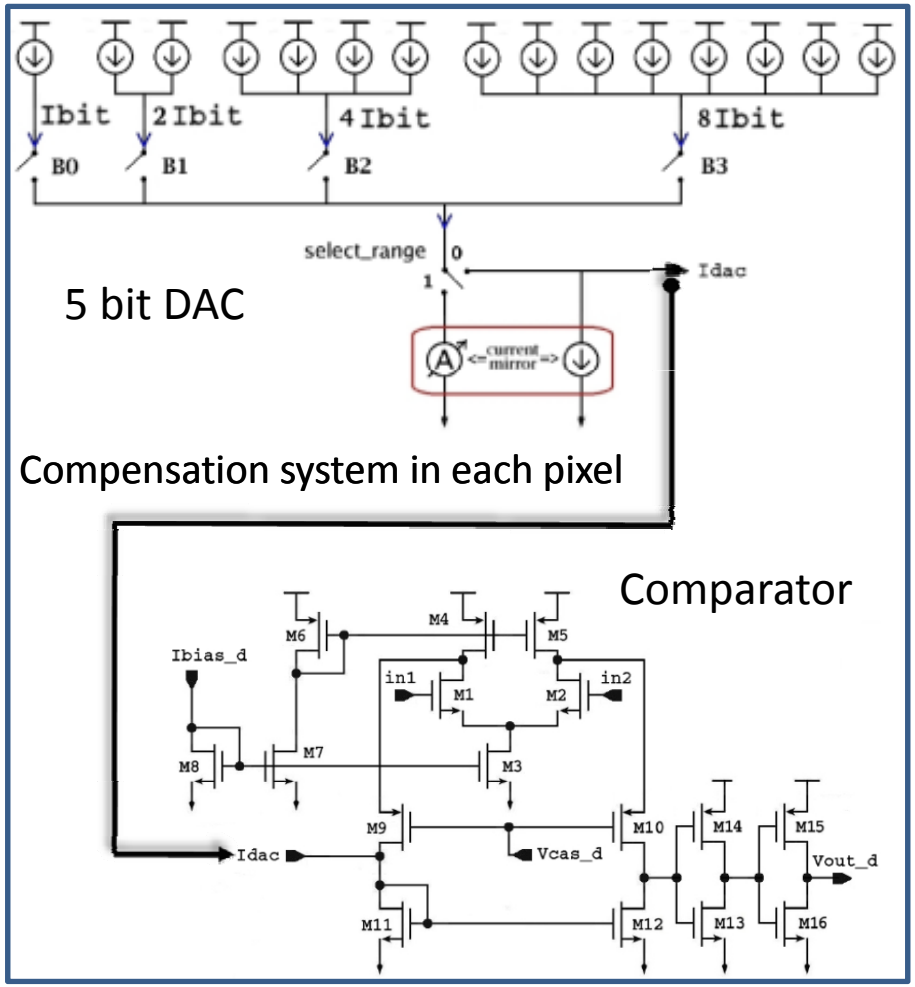


The discharging feedback current has no implication on the uniformity between the different channels.

ToT uniformity may be improved by reducing the mismatch effects of the leakage compensation stage input transistors

Measure: threshold dispersion

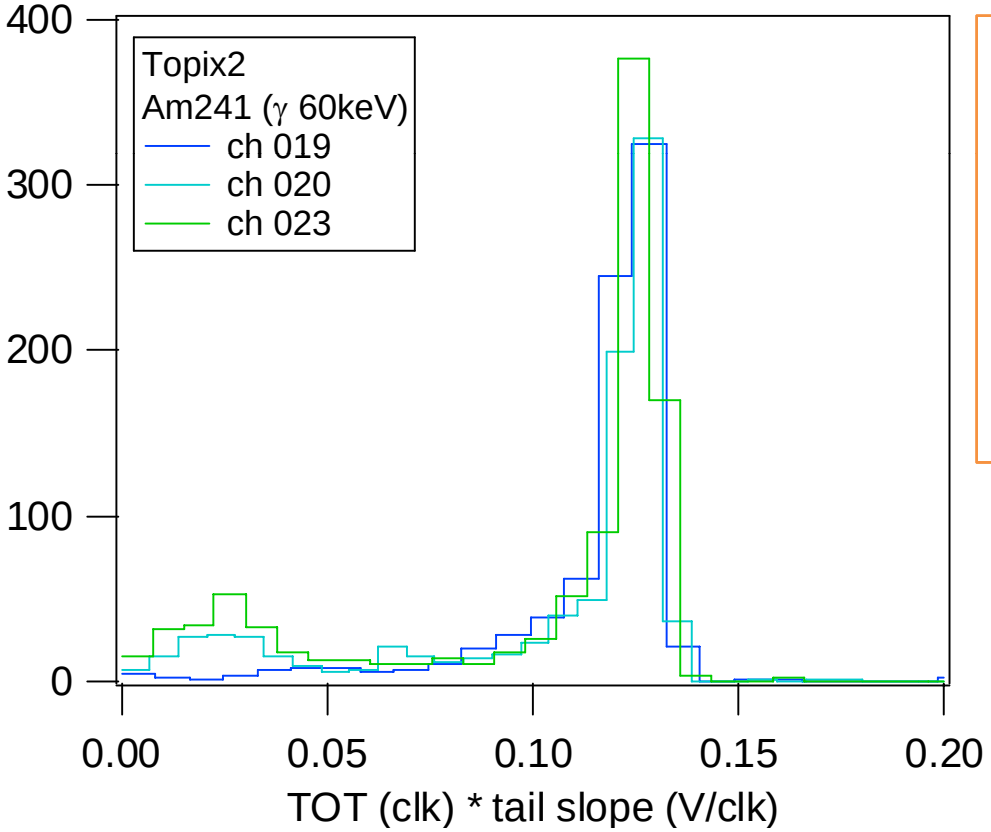




To mitigate the threshold dispersion a local 5 bit DAC is added in each pixel, to allow a fine tuning of the threshold on a pixel by pixel basis.

Measure: Calibration with Am source

Calibration with 60 KeV γ (Americium source)
Standard Floating Zone p-type sensor 300 μm thick, size: 50μm x 425 μm



$$\text{n° of } e^- h \text{ pairs} = \frac{E_\gamma}{E_{ion}} = \frac{60\ \text{keV}}{3.6\ \text{eV}} = 1.67\ 10^4$$

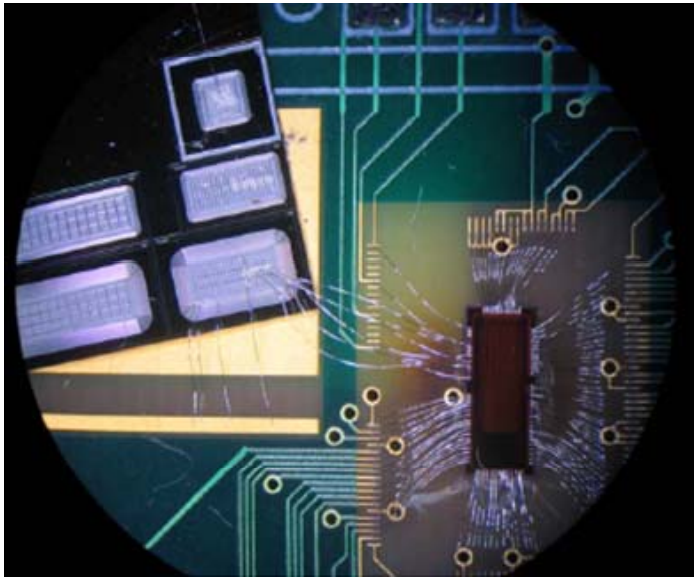
$$Q_{in} = \text{n° of } e^- h \text{ pairs} * e = 1.67\ 10^4 * 1.6 * 10^{-19}\ \text{C} = 2.67\ \text{fC}$$

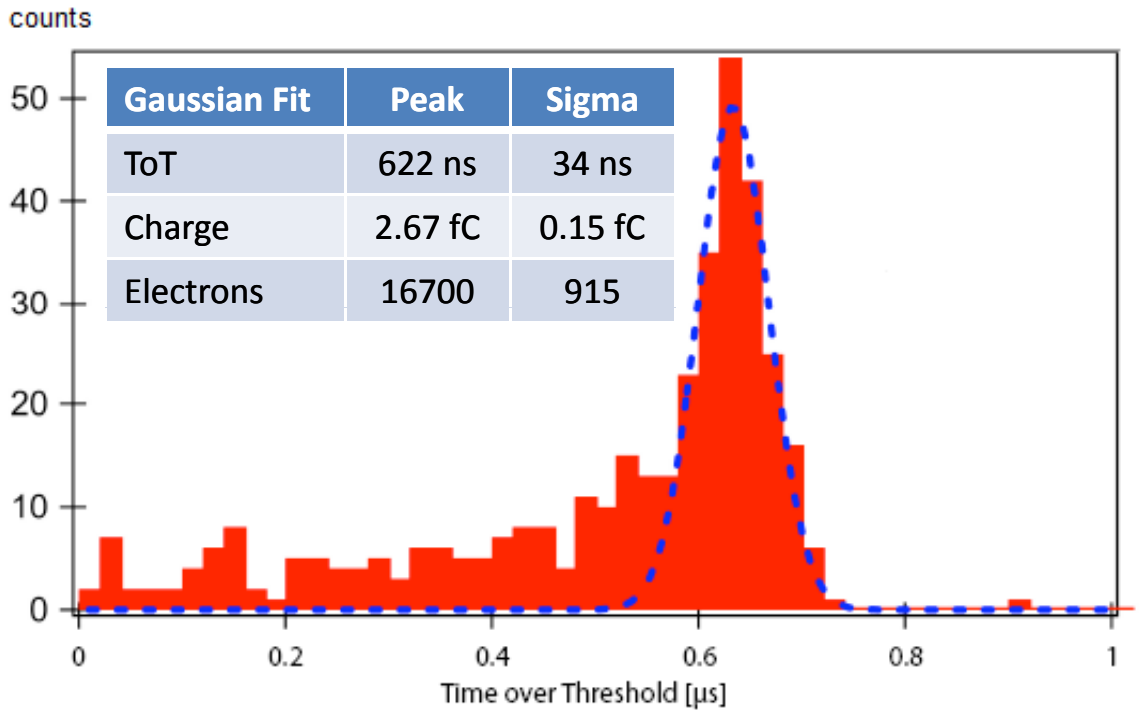
$$\text{ToT (clk)} * \text{tail slope (V / clk)} = Q_{in} * \text{Preamp\_Gain} = 111\ \text{mV}$$

Expected value: 111 mV
Good response

First spectra with an epi-sensor

Epitaxial sensor 50 μm thick, size: 125μm x 325 μm





Gaussian Fit	Peak	Sigma
ToT	622 ns	34 ns
Charge	2.67 fC	0.15 fC
Electrons	16700	915

Signal to noise ratio is limited by parasitics capacitance due the external connections: Bonding pad + wirebonding + protection diodes

Conclusion

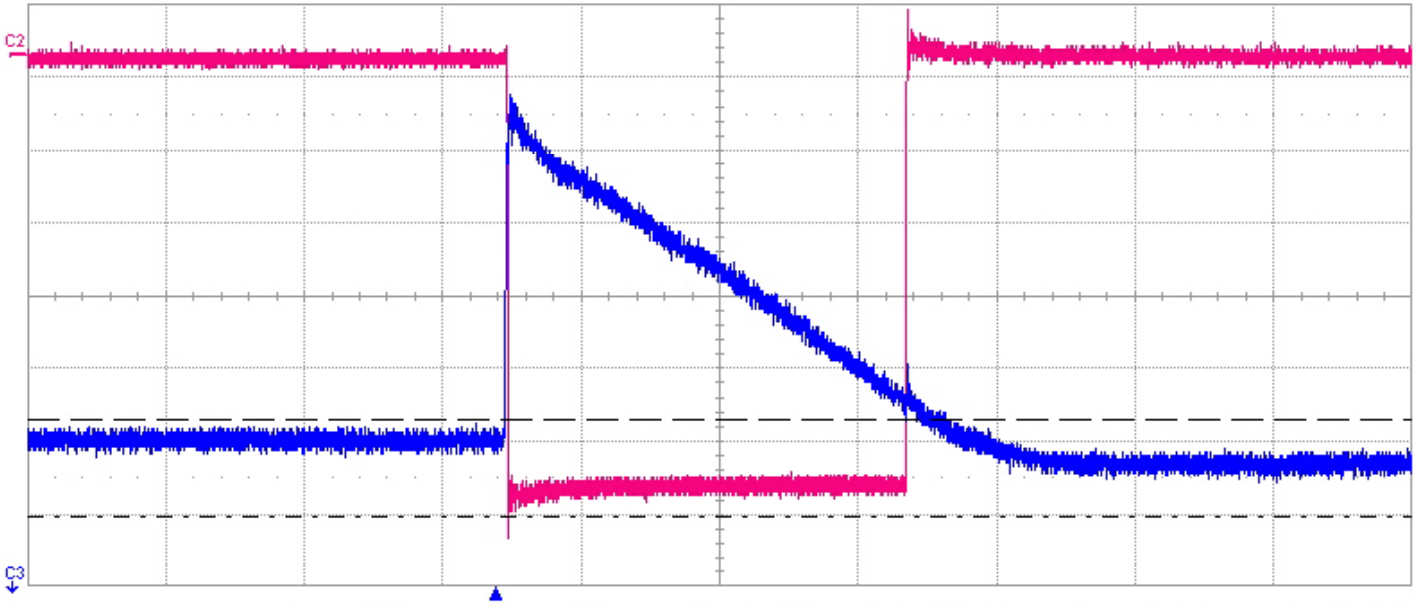
Tests show good agreement between specifications and measurements.

An upgrade of Topix 2.0. is currently under design:

- ToT uniformity has to be improved (< 10%).
- A more compact leakage compensation stage.
- Compatible with 160 MHz Clock.

Backup Slides

Topix 1.0 – Analog Output (1)



Measure	P1:ampl(C2)	P2:sdev(C3)	P3:delay(C2)	P4:ddelay(C3,C2)	P5:time@lv(C3)	P6:wid@lv(C3)
value	1.1789 V	129.8 mV	44.108 ns	-7.116 ns	38.872 ns	---
mean	1.178950 V	129.771 mV	44.10798 ns	-7.11647 ns	38.87209 ns	---
min	1.1789 V	129.8 mV	44.108 ns	-7.116 ns	38.872 ns	---
max	1.1789 V	129.8 mV	44.108 ns	-7.116 ns	38.872 ns	---
sdev	---	---	---	---	---	---
num	1	1	1	1	1	0
status	✔	✔	✔	✔	✔	

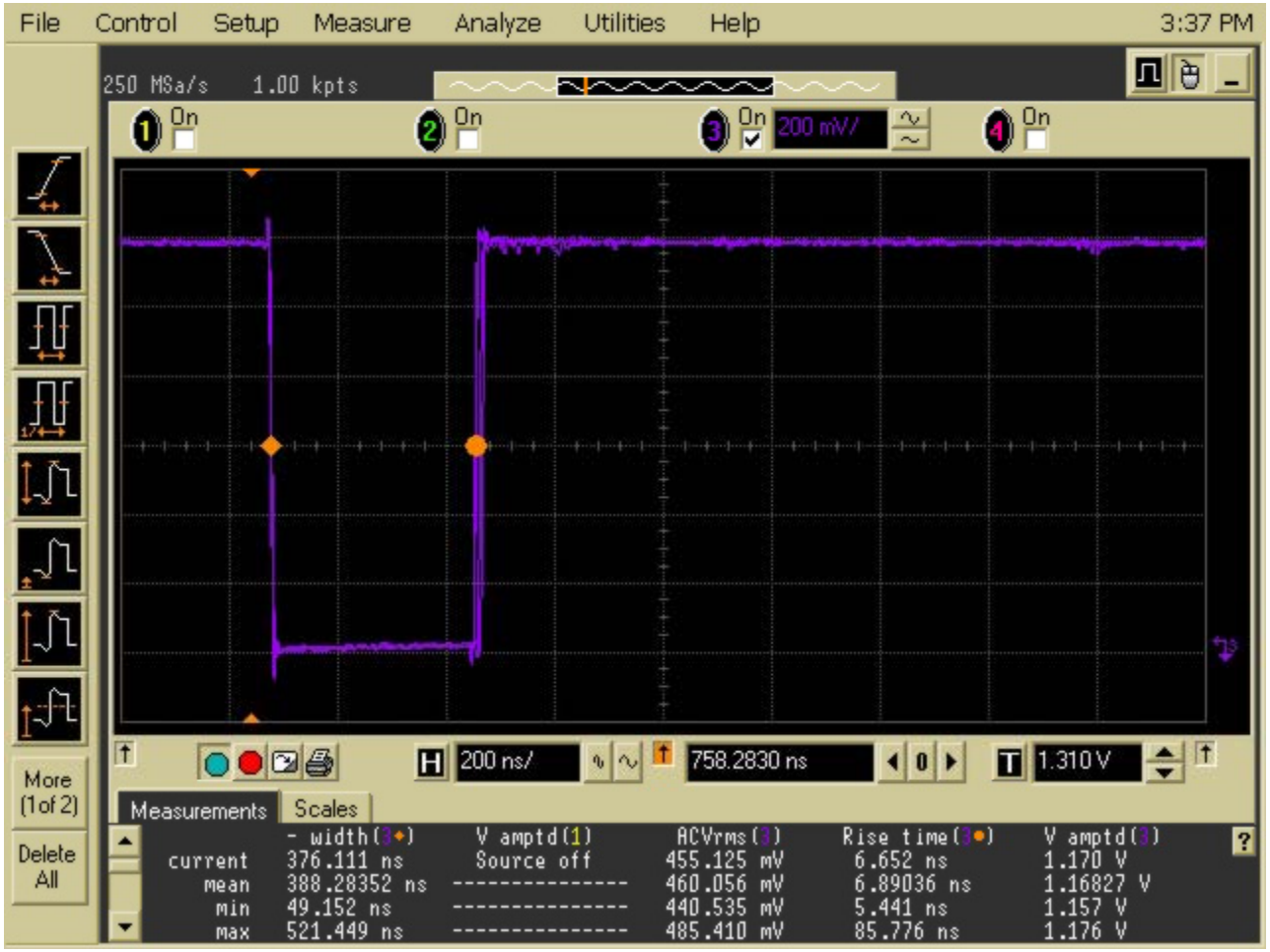
C2 AC1M 200 mV/div 660.0 mV Δy 264 mV

C3 DC1M 100 mV/div -520.0 mV Δy 132 mV

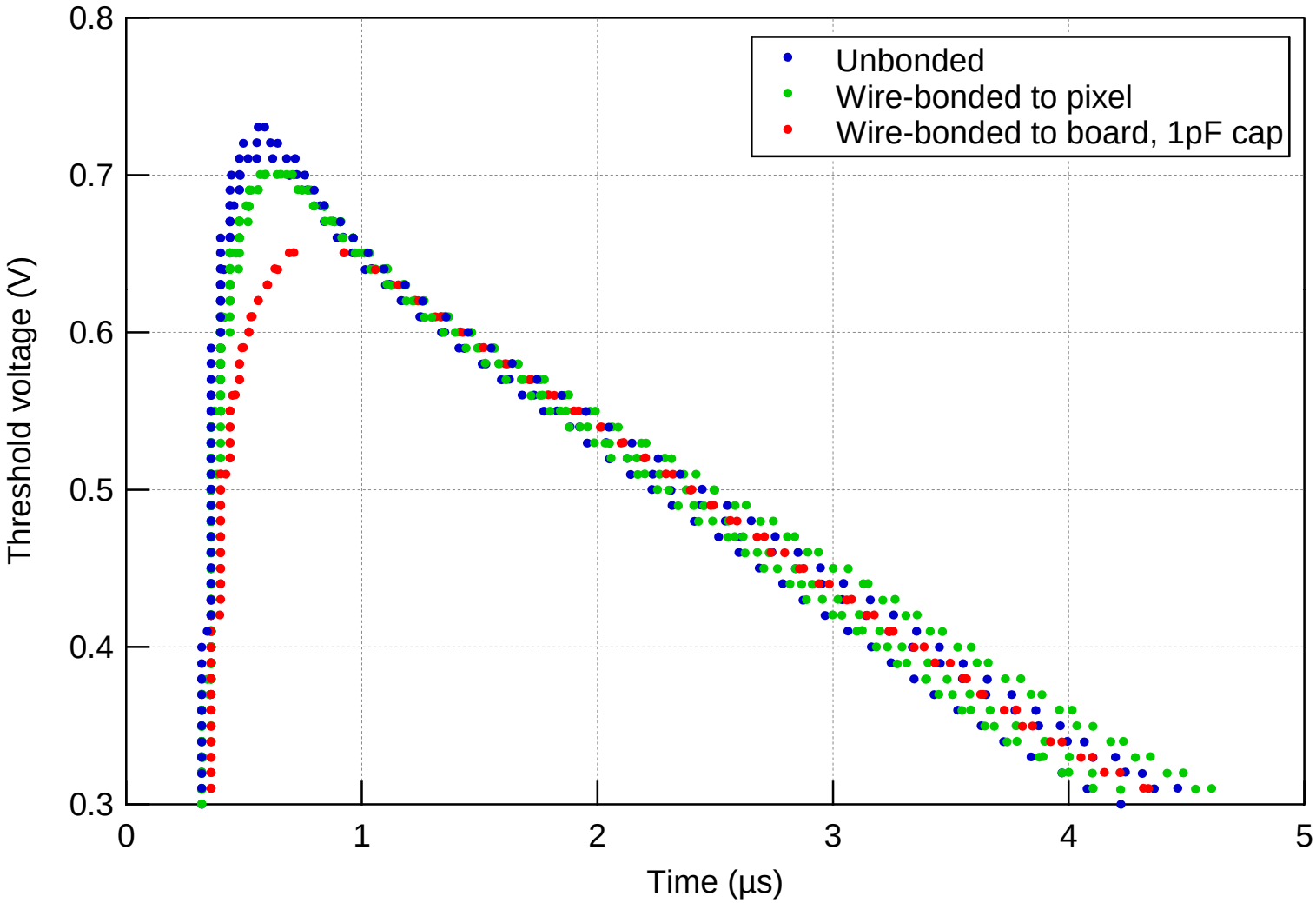
Timebase -810 ns 500 ns/div 25.0 kS 5.0 GS/s

Trigger Ext DC50 Stop -133 mV Edge Negative

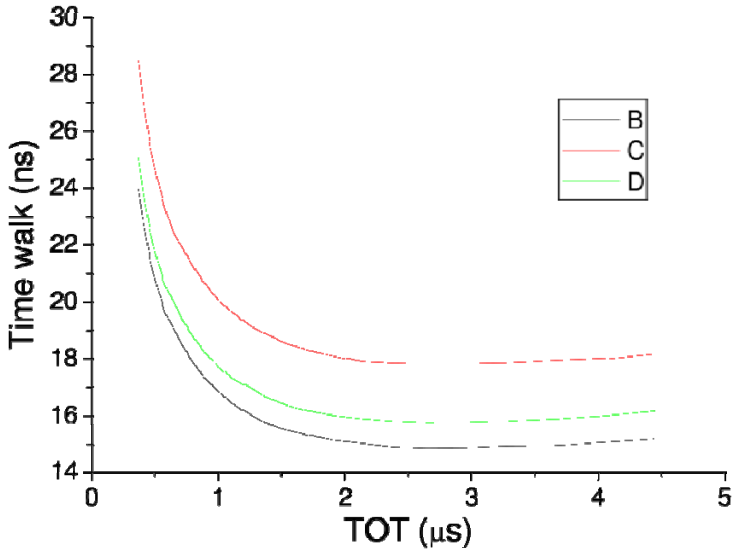
Topix 1.0 – Analog Output (2)



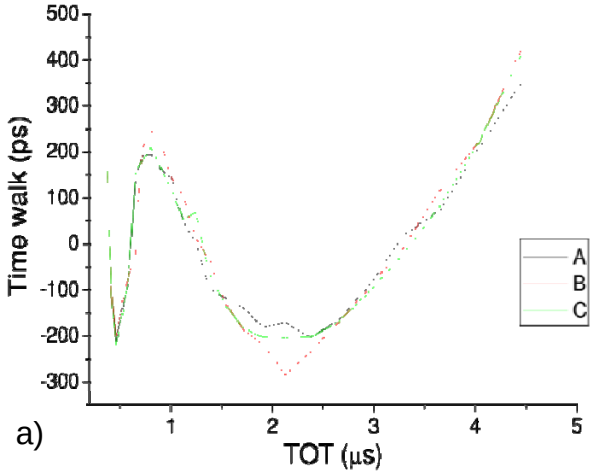
ToT measurement



Time Walk

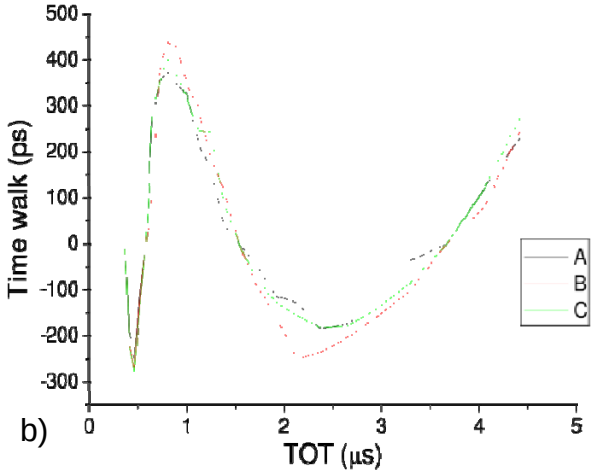


24 Calibration points



a)

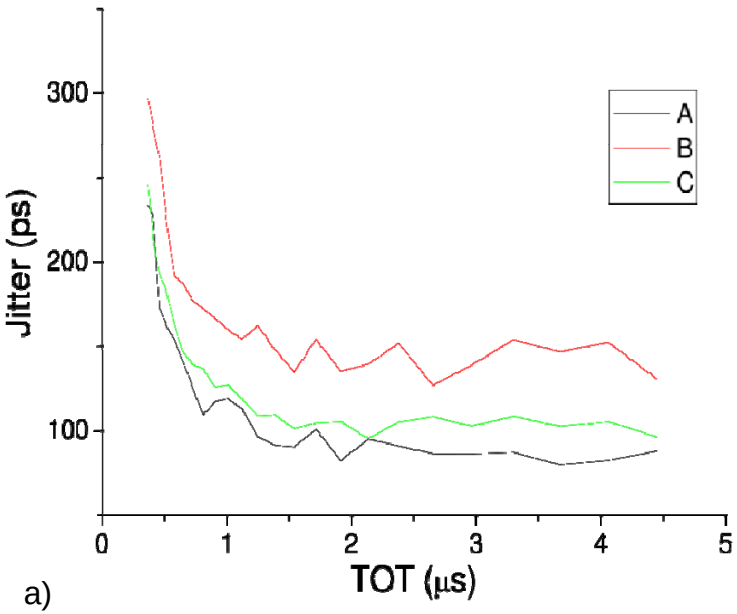
5 Calibration points



b)

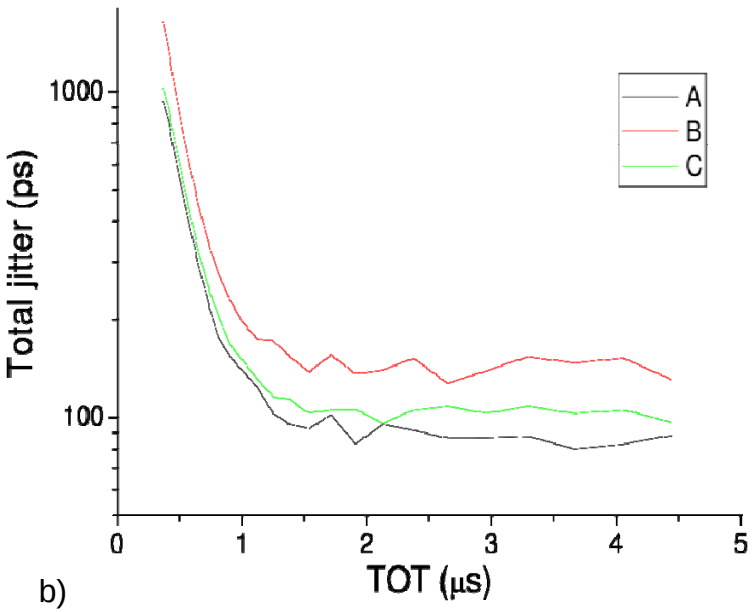
Jitter

Leading edge jitter



a)

Total jitter



b)