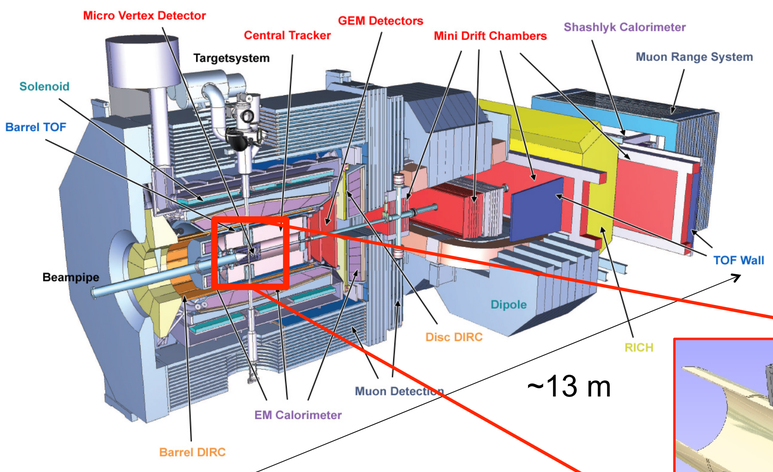
Upgrade of the Jülich Digital Readout System for the Development of the $\bar{P}$ANDA-MVD

JÜLICH FORSCHUNGSZENTRUM

Motivation

- Frontend ASIC testing and characterization for the PANDA MVD
  → Readout system has been developed in Jülich
- Modular design for fast and simple adaption to new front end prototypes
- Hardware upgrade to use off the shelf components in the lab

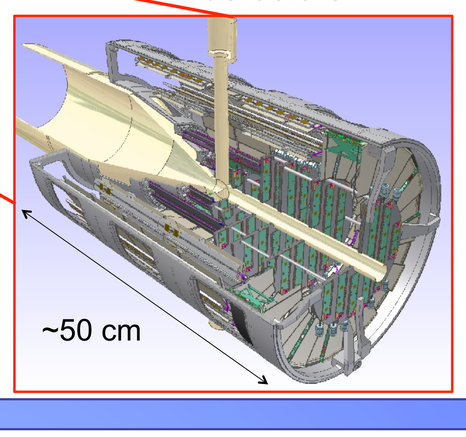
The PANDA Detector



- Fixed target experiment
- Triggerless readout concept
- Phasespace cooled antiproton beam with a momentum range from 1.5 to 15 GeV/c

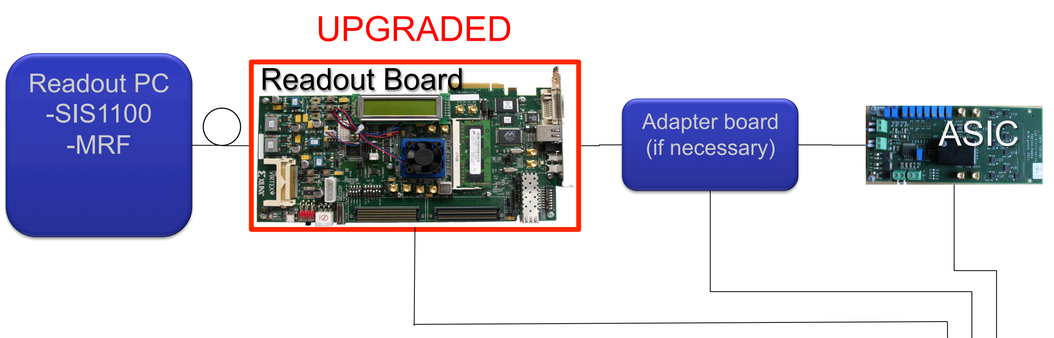
The Micro Vertex Detector

- Innermost tracking detector
- Main task is the vertexing of short living hadrons e.g. $D^{\pm}$-meson ($c\tau \sim 312\ \mu m$)
- Four barrel layers and six disks of semiconductor detectors

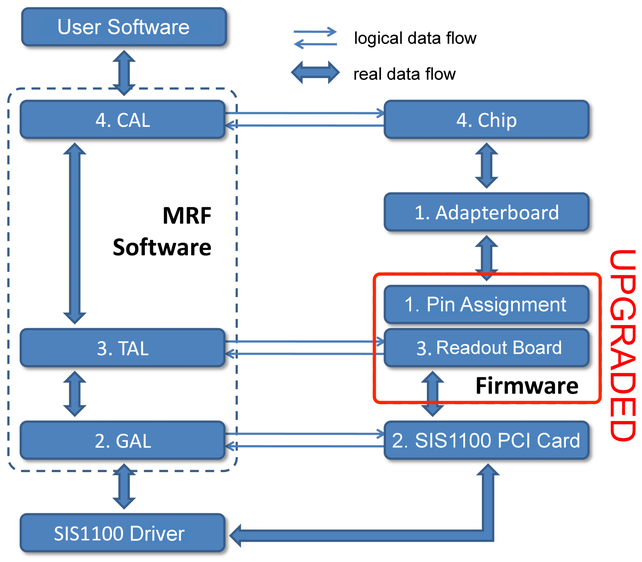


- Vertex resolution of MVD < 100 µm
- Hybrid silicon pixel detectors with custom readout ASIC
  → ToPix (TOrino PIXel)
- Double side silicon strip detectors

The Jülich Digital Readout System

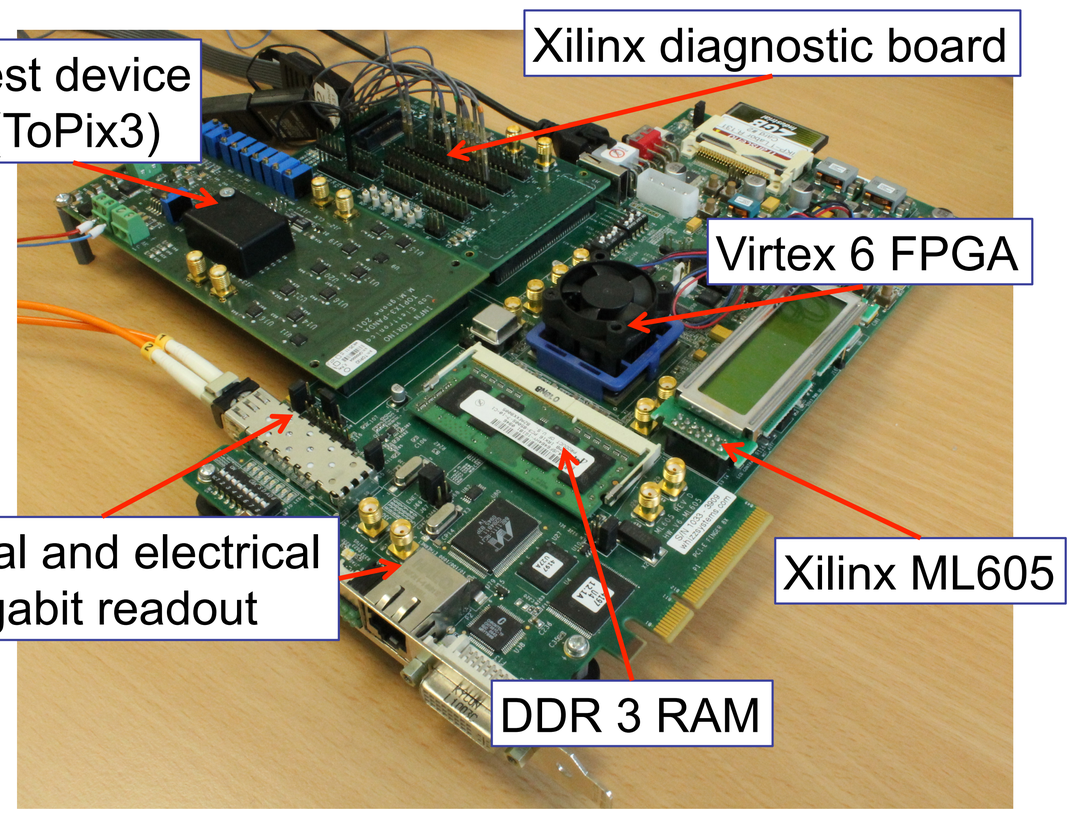


- The system consists of readout hardware, firmware and software (MVD Readout Framework – MRF)
- Central component is a FPGA based readout board.
- Modular concept – minor changes necessary to adapt the system to different ASICs.
- Data is transferred over a 1 gigabit optical connection (SIS1100)
- Four communication layers implemented. Every hardware component is treated by a software class (modular design)



CAL – Chip access layer
TAL – Transport access layer
GAL – Generic access layer

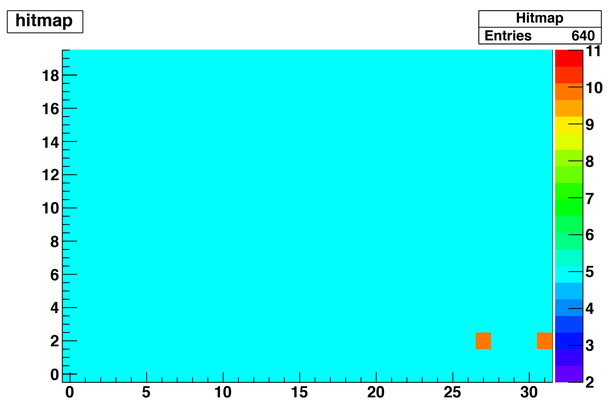
Hardware Upgrade



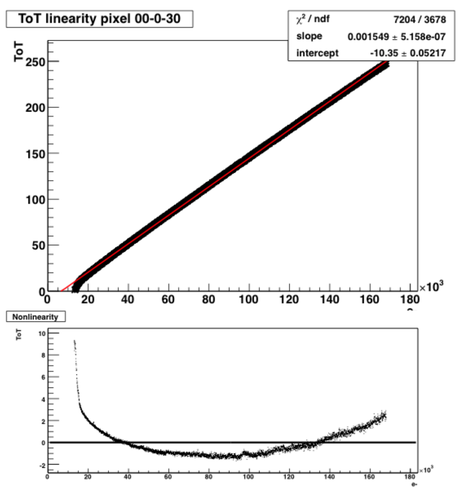
- New central hardware component: Xilinx ML605 Evaluation Board
- Cheap and easy to obtain
- Virtex 6 FPGA
- Expandable DDR3 RAM
- Optical and electrical gigabit connection
- FMC connectors (HPC and LPC)
- LC Display

Measurements with ToPix3

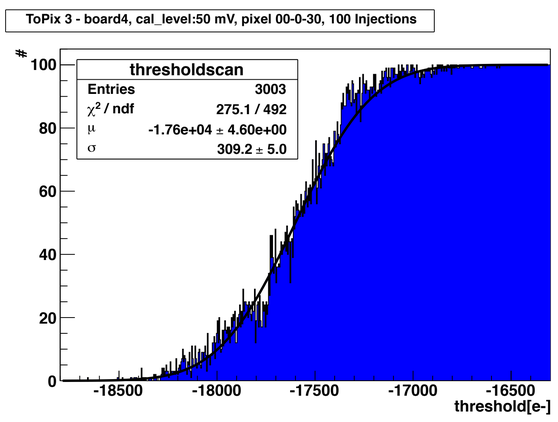
Front end ASIC of pixel part – ToPix. Time over Threshold (ToT) charge measurement.



Pixel tests with ToPix3 – inject 5 times into each pixel and count number of detected hits – two broken pixels found



Measurement of the ToT linearity



Threshold scan of a single pixel:
Inject constant charge, vary threshold

Summary

- A readout system exists to characterize front end ASICs
- A hardware upgrade has been developed to extend the memory and FPGA resources
- Measurements with the recent ToPix 3 prototype have been done to prove the functionality of the readout system
- Next step: implementation of ethernet based protocol

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