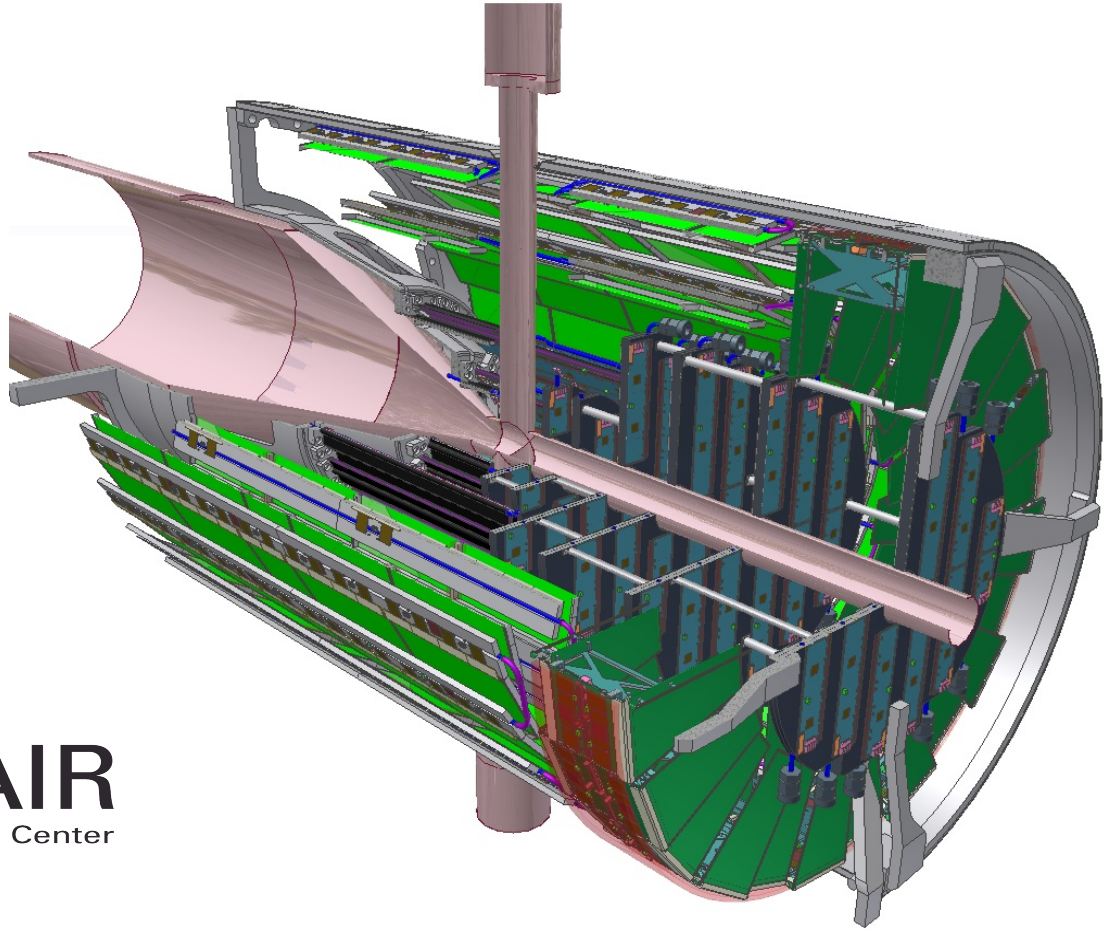
The $\overline{\text{P}}$ANDA MVD



Robert Schnell
II. Physikalisches Institut, JLU Gießen
On behalf of the $\overline{\text{P}}$ANDA collaboration

II. Physikalisches Institut

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

The $\overline{\text{P}}$ANDA Detector @ FAIR

- The existing GSI facility in Darmstadt

The $\overline{\text{P}}$ANDA Detector @ FAIR

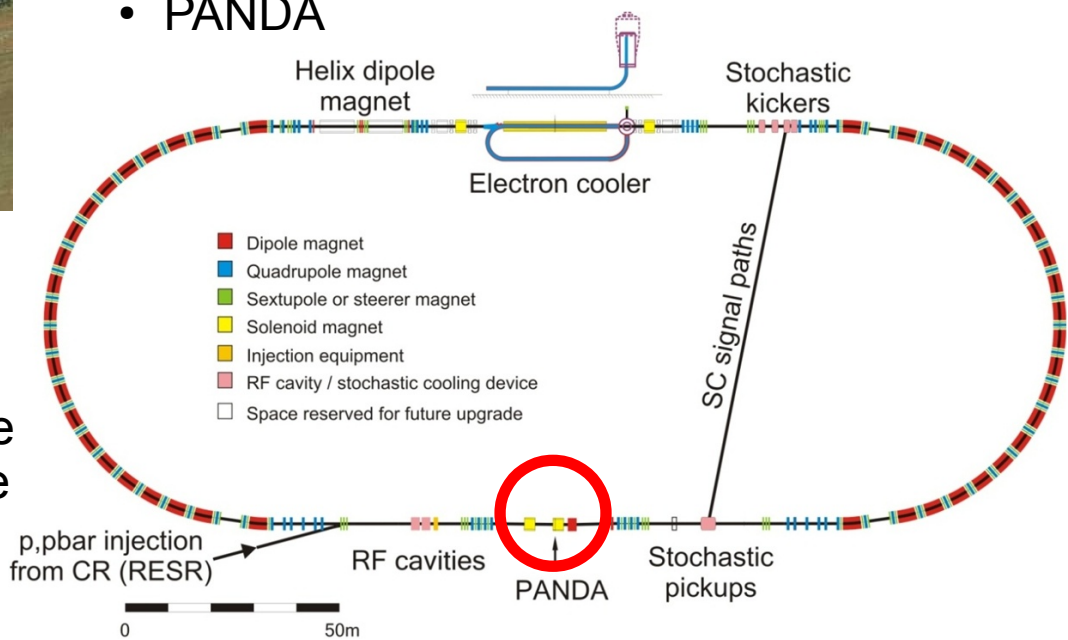
- The existing GSI facility in Darmstadt will be extended to FAIR
  (**F**acility for **A**ntiproton and **I**on **R**eseach)
- FAIR will deliver
  - Protons
  - Antiprotons
  - Ions
- To several experiments
  - APPA
  - CBM
  - NUSTAR
  - $\overline{\text{P}}$ANDA
    (anti**P**roton **An**nihilation at **Da**rmstadt)

The $\overline{\text{P}}$ANDA Detector @ FAIR

- The existing GSI facility in Darmstadt will be extended to FAIR (**F**acility for **A**ntiproton and **I**on **R**eseach)
- FAIR will deliver
  - Protons
  - Antiprotons
  - Ions
- To several experiments
  - APPA
  - CBM
  - NUSTAR
  - $\overline{\text{P}}$ANDA

- Antiproton Storage Ring HESR
  - up to 10^{11} stored antiprotons
  - Momentum range 1.5 to 15 GeV/c
  - Stochastic cooling → high luminosity mode
  - Electron cooling → high resolution mode

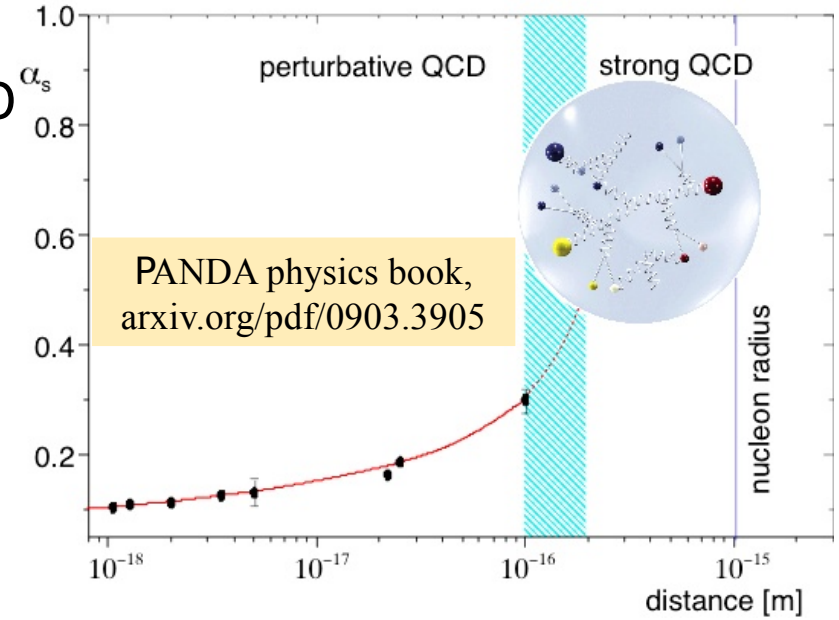
    $dp/p < 4 \cdot 10^{-5}$



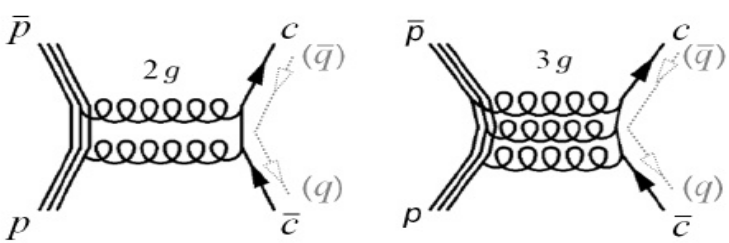
$\overline{\text{P}}$ANDA physics

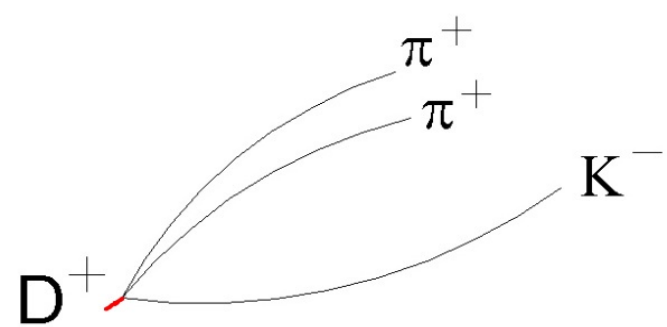
Very broad physics program:

- Open Questions in strong (non-pertubative) QCD
  - Charmonium
  - Open charm
  - Hybrids, glue balls and exotics
- In medium modifications of hadrons
- Hypernuclear physics
- Electromagnetic channels and processes
  - Generalized parton-distributions
  - Drell-Yan
- Rare decays
- Baryon spectroscopy
- CP violation in the charm sector
- Antiproton physics at low energies

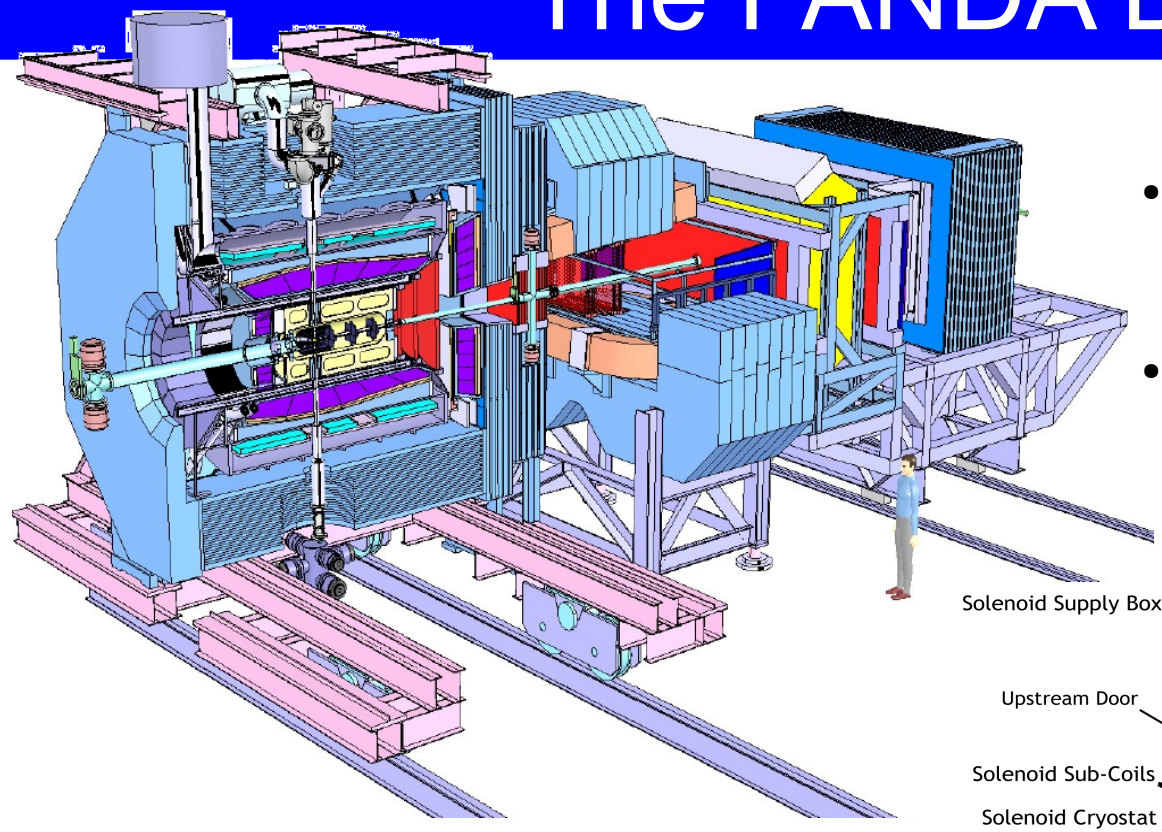


PANDA physics book, arxiv.org/pdf/0903.3905

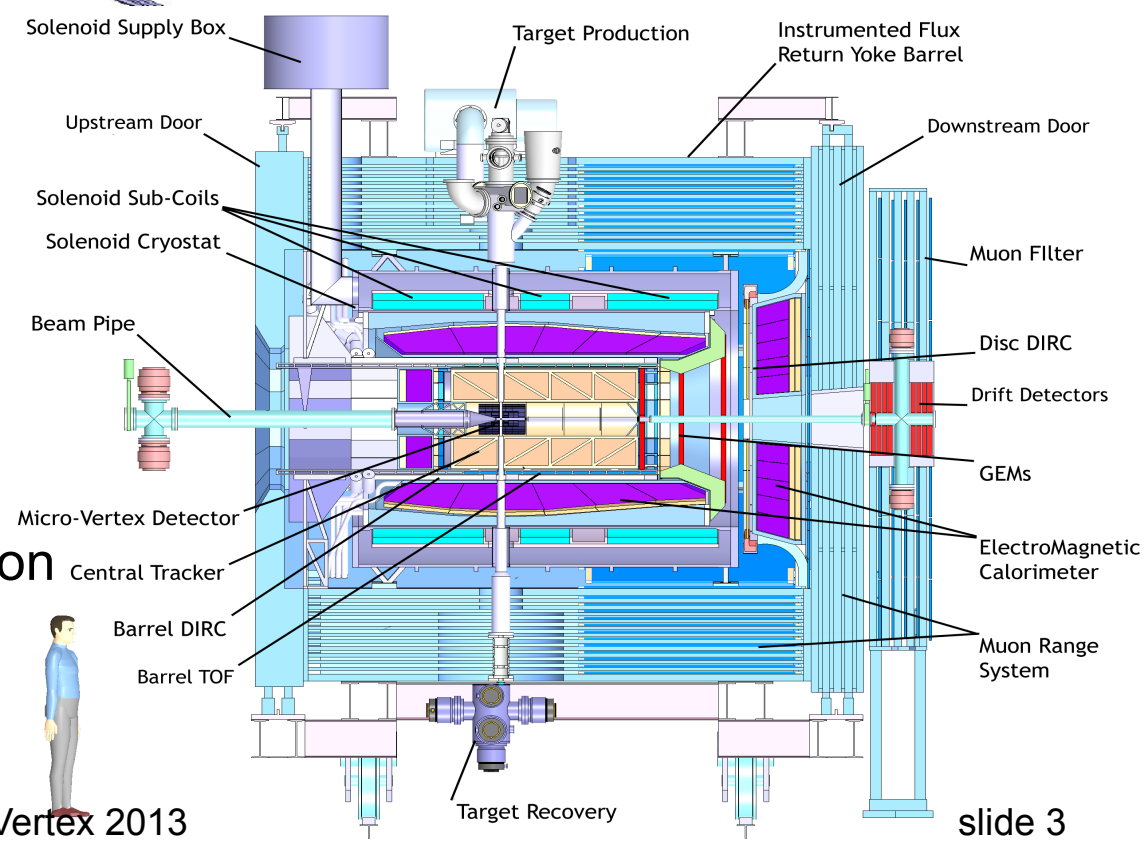




The $\bar{P}$ANDA Detector

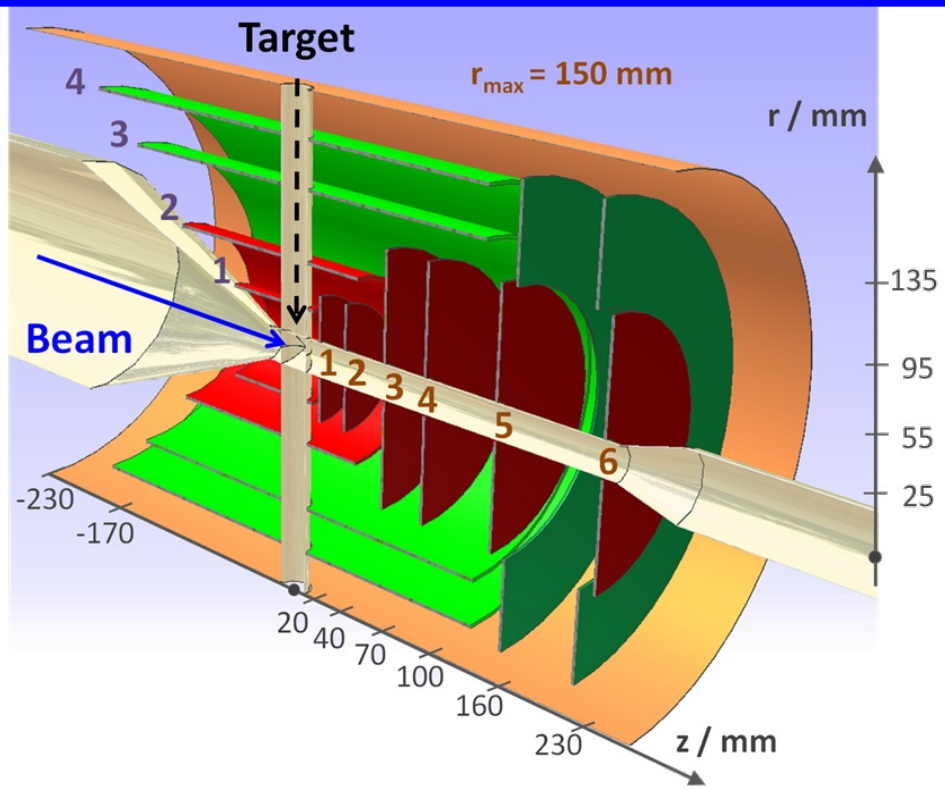


- Fixed target experiment
  - Target spectrometer, 2 T solenoid
  - Forward spectrometer, 2 Tm dipole
- 4π acceptance

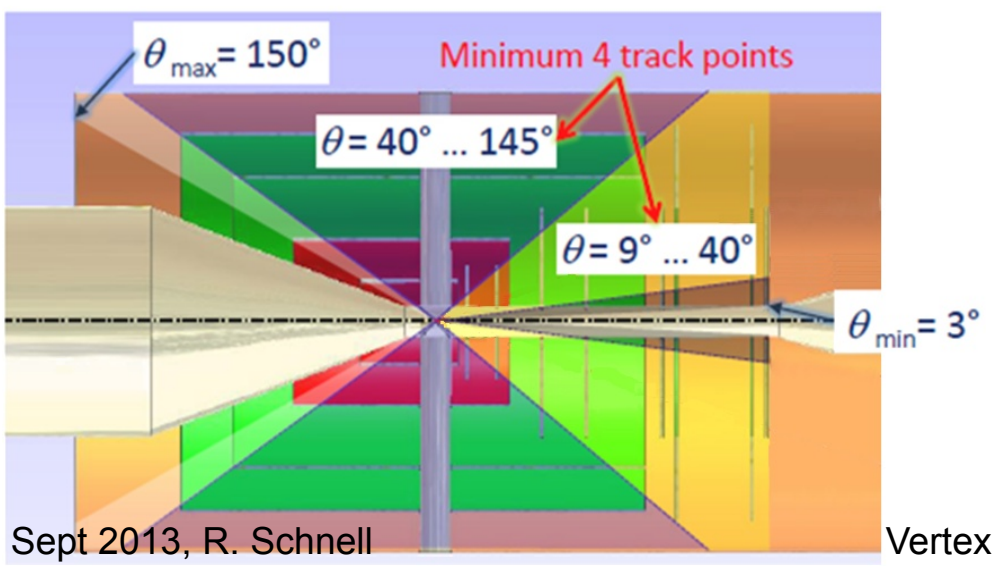


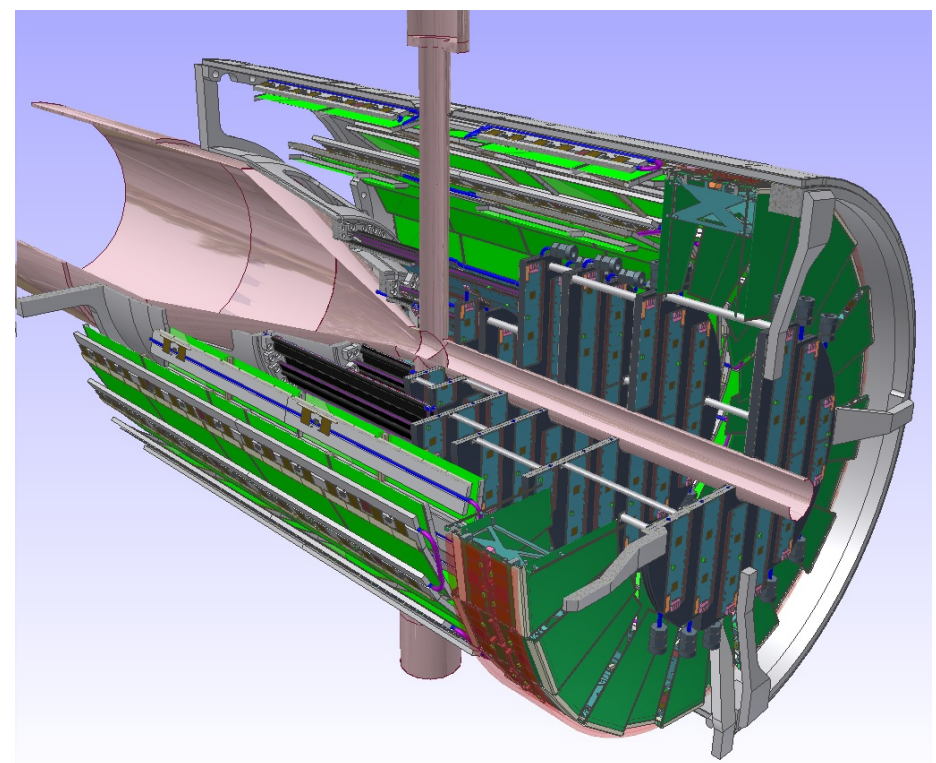
- Detector layers for:
  - Tracking
  - Particle identification
  - Calorimetry
- High spacial and momentum resolution
- High interaction rate beyond $2 \cdot 10^7 s^{-1}$
- No hardware trigger

The Micro-Vertex Detector



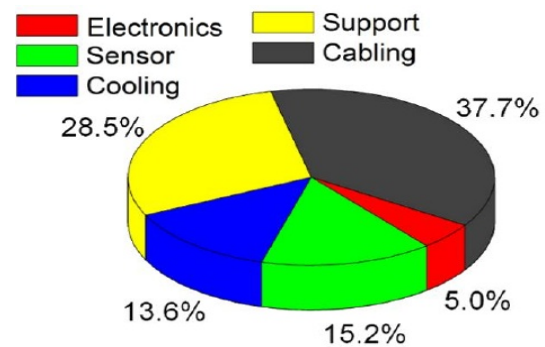
- 2 barrel pixel layers
- 4 pixel disks
- 2 barrel strip layers
- 2 mixed disks
- 2 optional forward wheels (@40 & 60 cm)

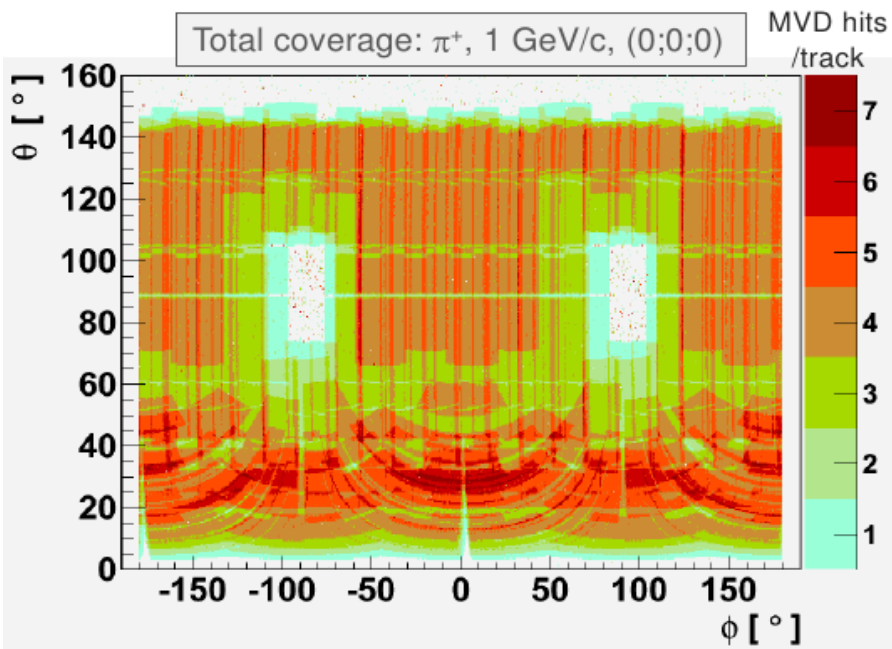


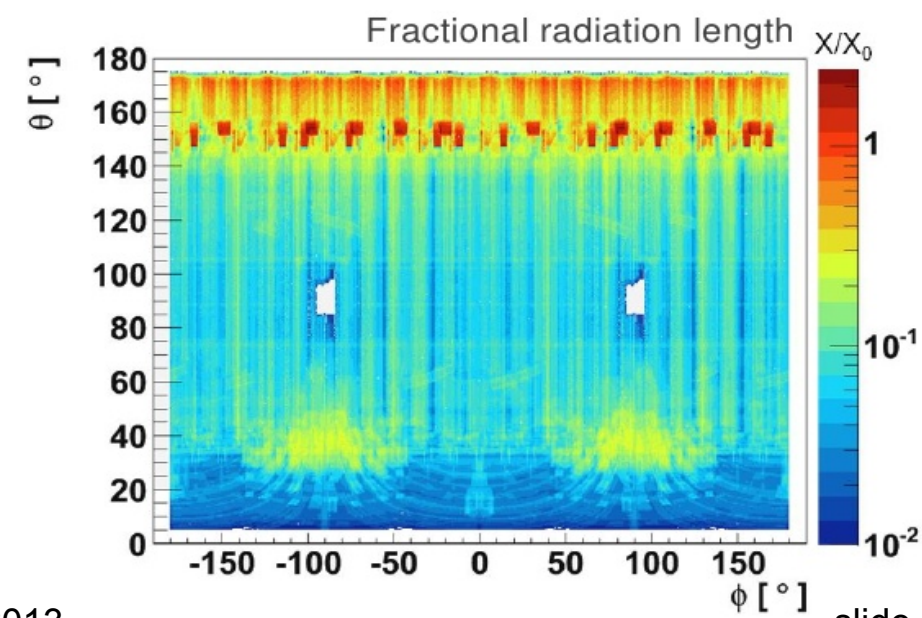


Numbers

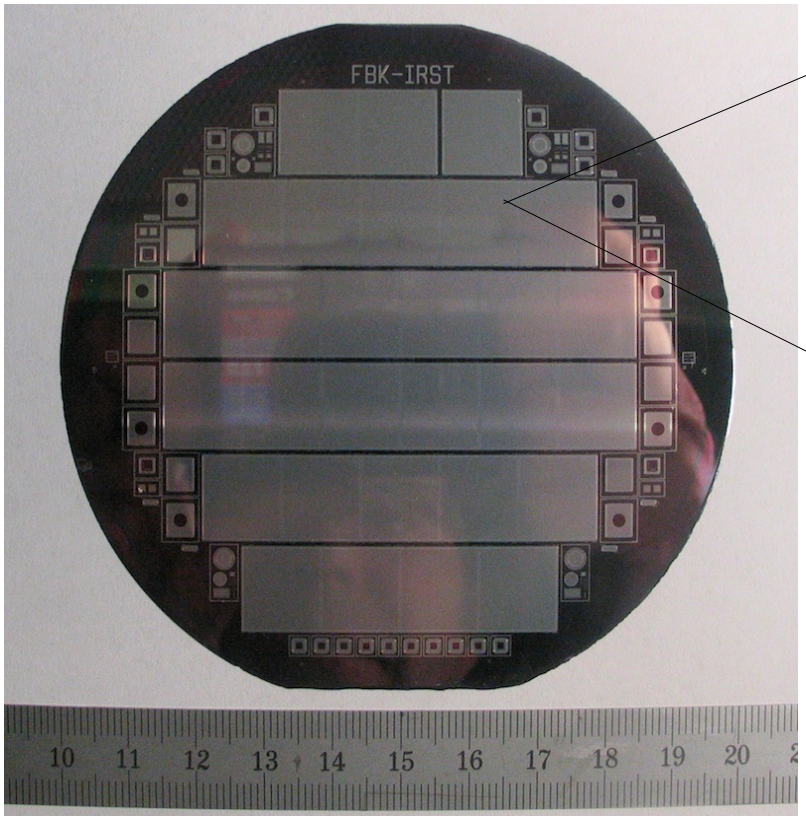
- Number of sensors: 176 (pixel) 296 (strip)
- Number of front-ends: 810 (pixel) 1744 (strip)
- Number of channels: 10.3 M (pixel) 200k (strip)
- Active area (m²): 0.106 (pixel) 0.47 (strip)
- Cables off MVD: 1584 (disks) 3592 (barrels) 614 (GBT)
  5790 (total)
- Cable cross section: 21835 mm² (total)

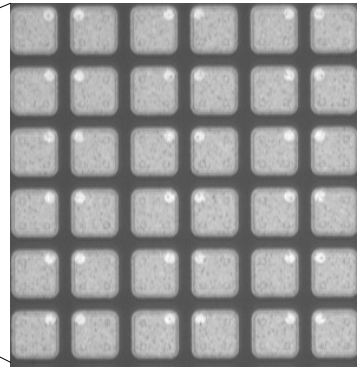






Pixel Subdetector - Sensors





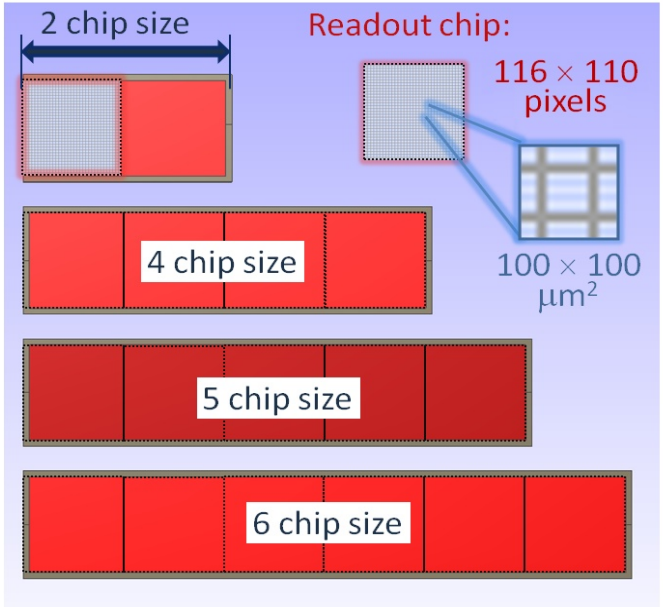
INFN Torino

Epitaxial silicon pixel sensors

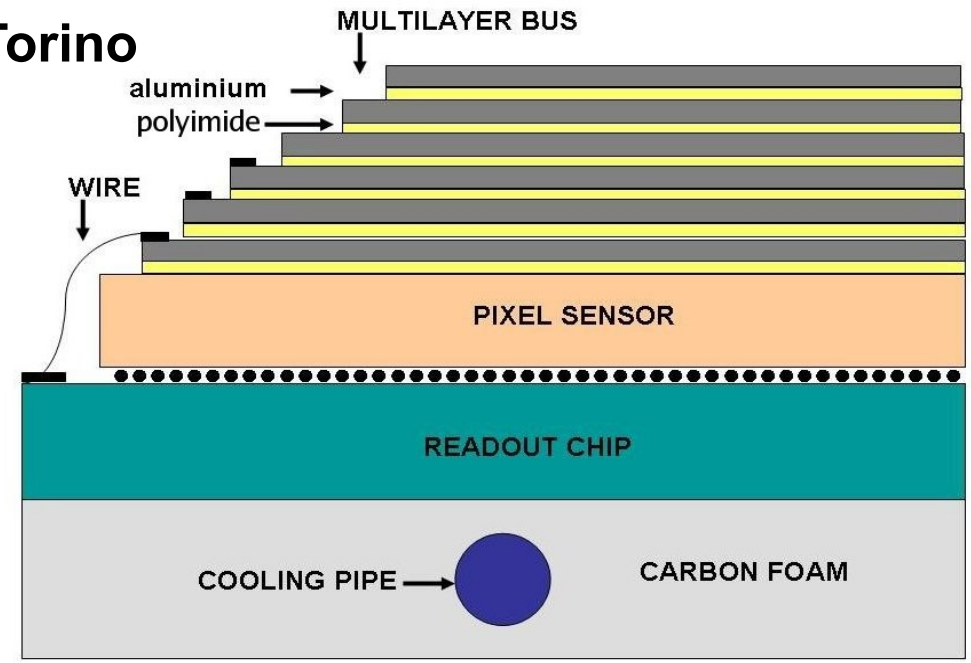
- Epitaxial layer on Czochralski substrate
- Several thicknesses evaluated,
  100 µm epitaxial layer chosen for $\overline{\text{P}}$ANDA
- Small pixel size of 100 x 100 µm²
- Full qualification of prototypes done
- Full size PANDA geometry

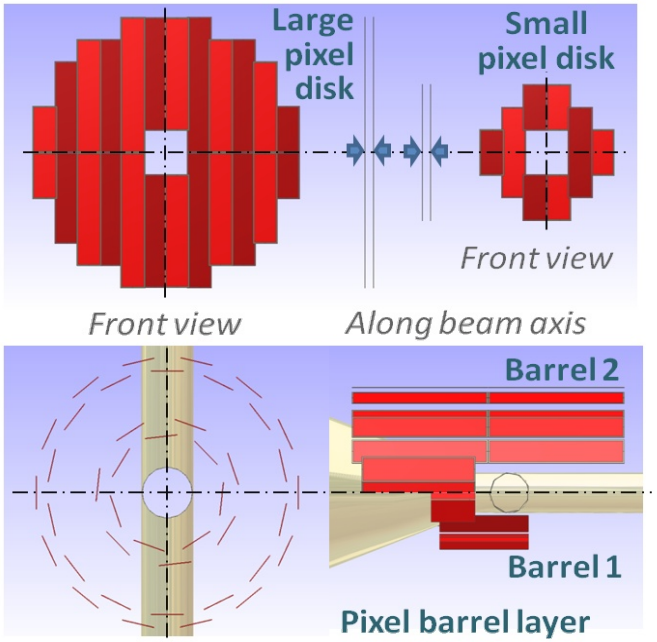
NIMA 594 (2008) p.29

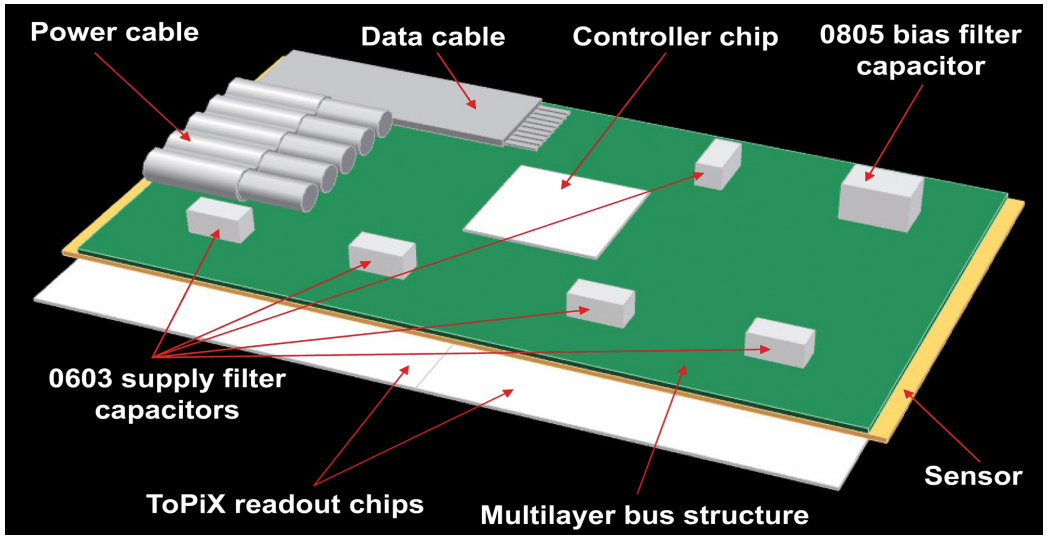
Pixel Subdetector - Modules



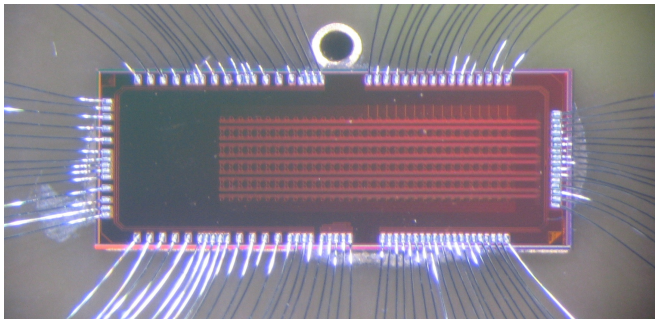
INFN Torino







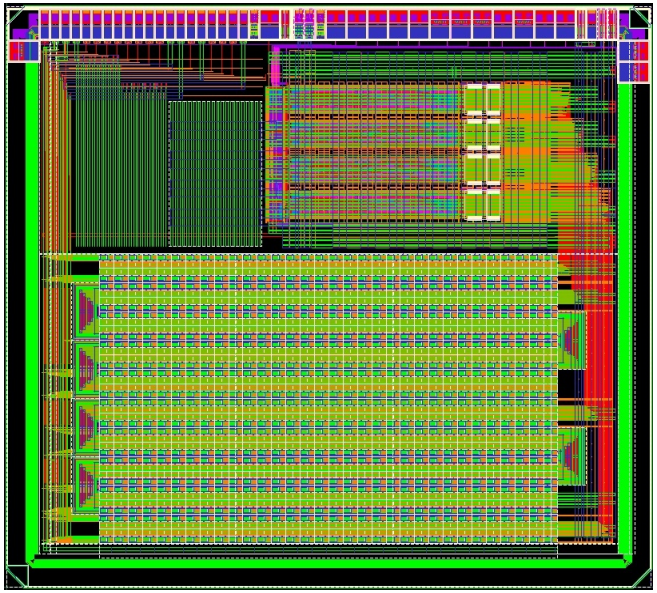
Pixel Subdetector - Front-end



ToPix v2

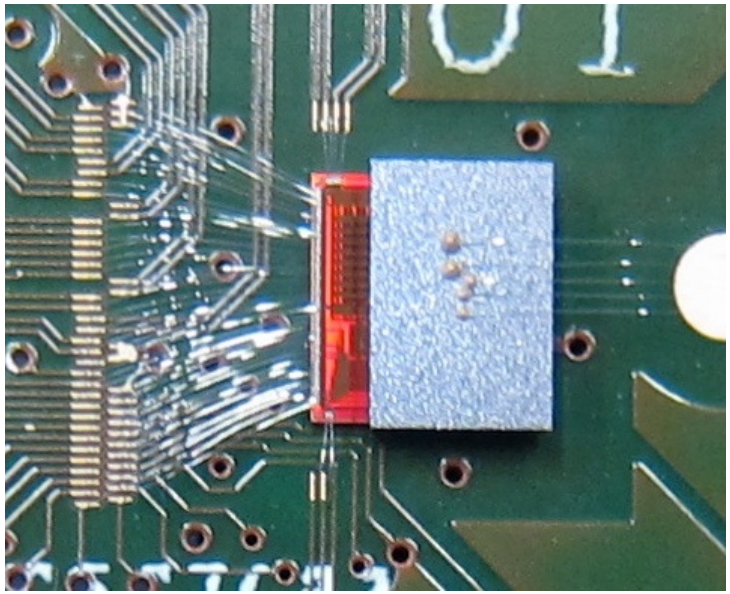
INFN Torino

NIMA 596 (2008) p.96

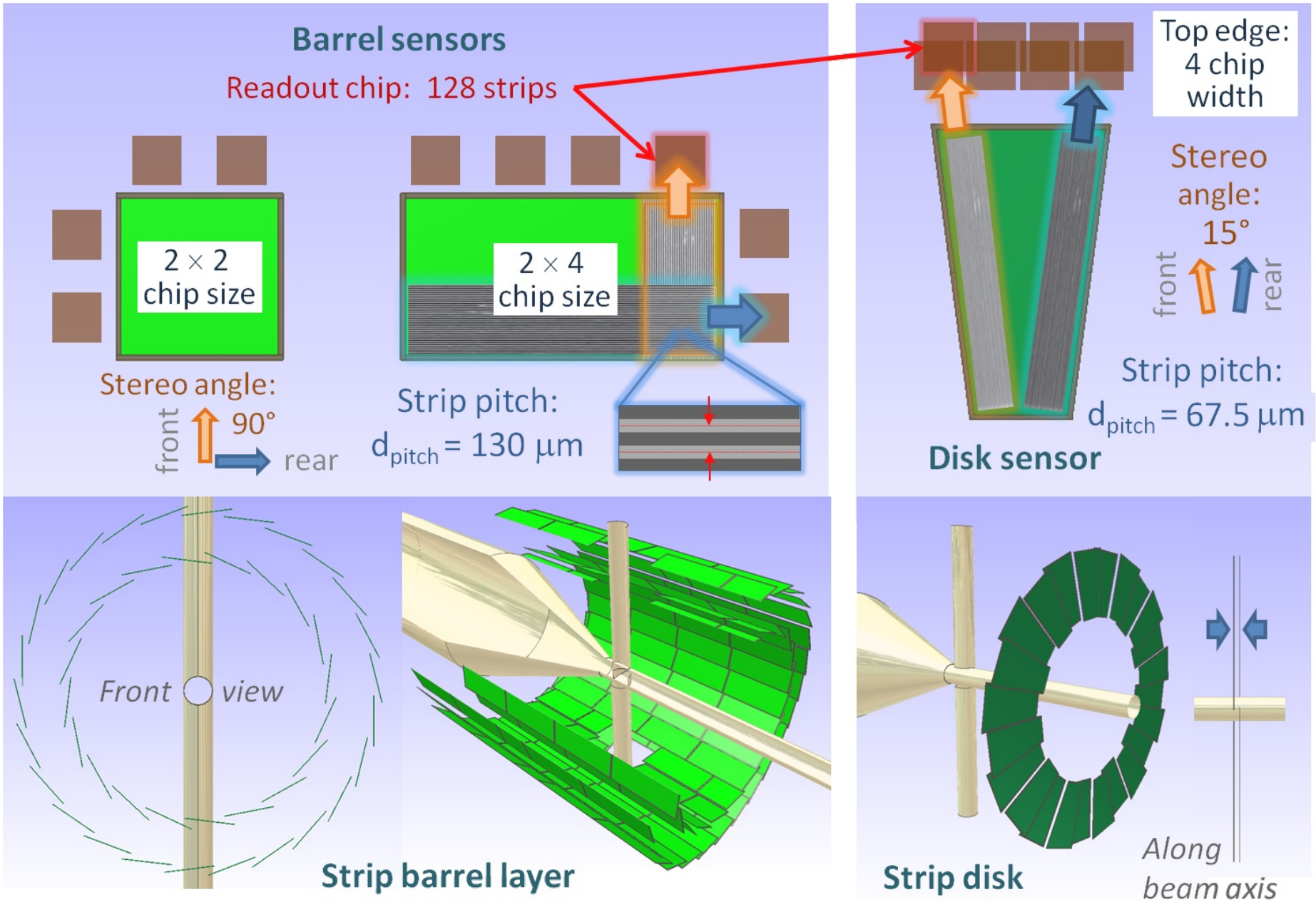


ToPix v3

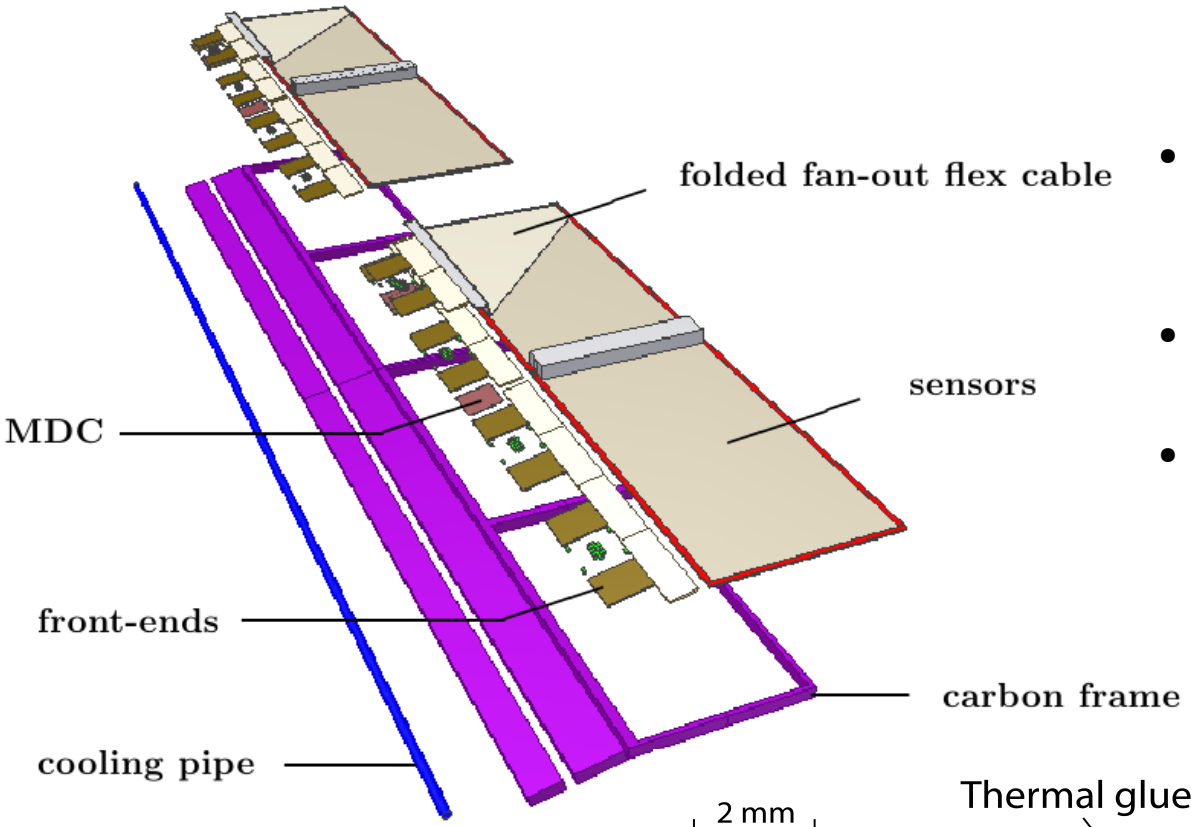
- Torino Pixel Readout Chip
- IBM CMOS 0.13 µm
- Time-over-Threshold
- Current prototype version ToPix v3
- 2 x 128 + 2 x 32 double columns
- Size 4 x 4.5 mm²
- Complete pixel cells with full column architecture, end-of-column logic and buffers
- Triple redundancy-based SEU protection
- Fully tested in lab and beam setups
- Next prototype ToPix v4: submission planned in November 2013 including GBT e-link interface SDR and DDR



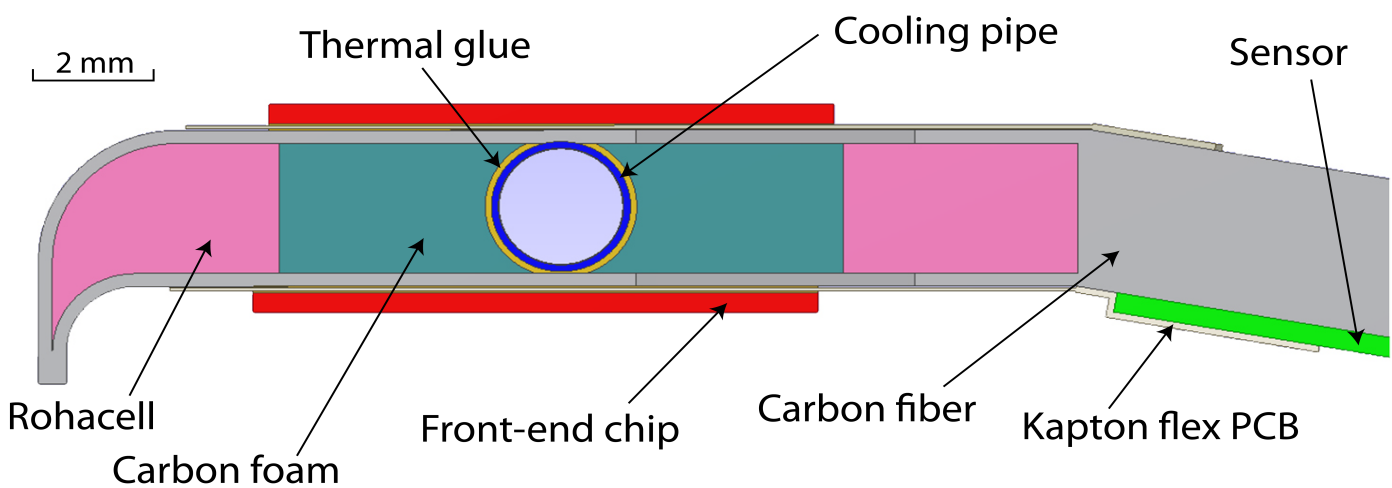
Strip Subdetector - Setup



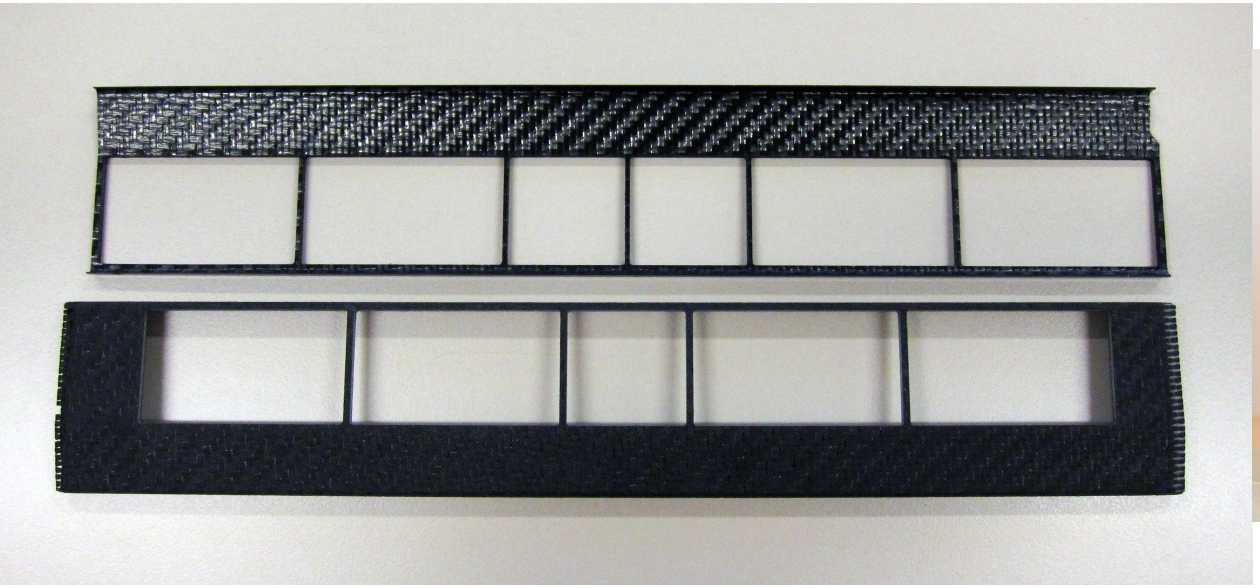
Strip Subdetector – Barrel Stave

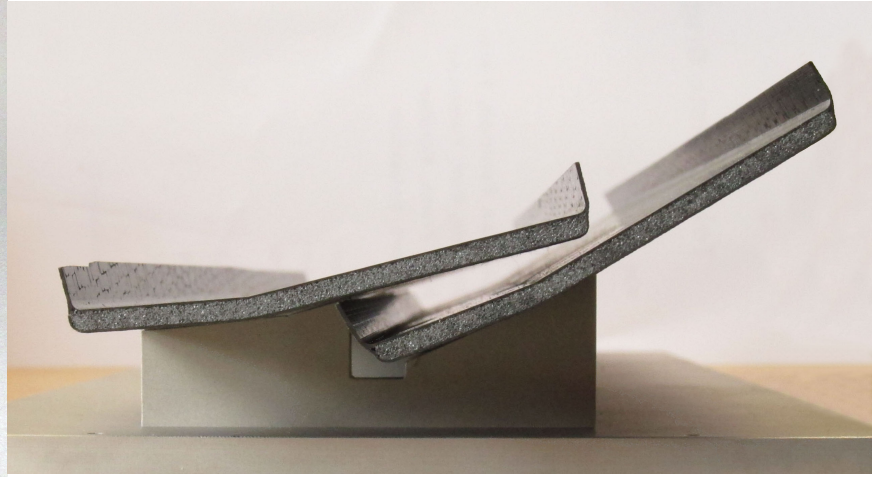


- Ultralight carbon foam molded in carbon fiber form sheet reinforcements
- High thermally conducting carbon foam beneath front-ends
- Integrated cooling pipe



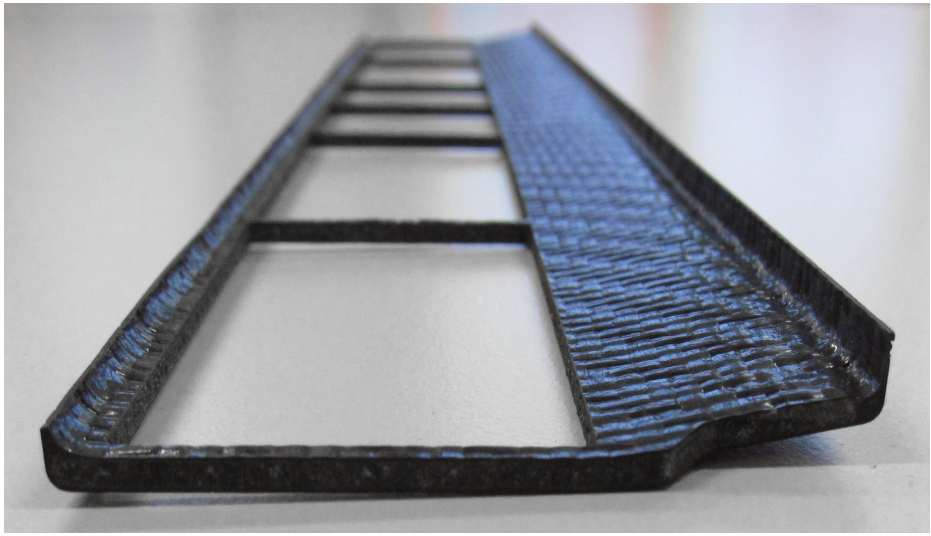
Stave prototypes





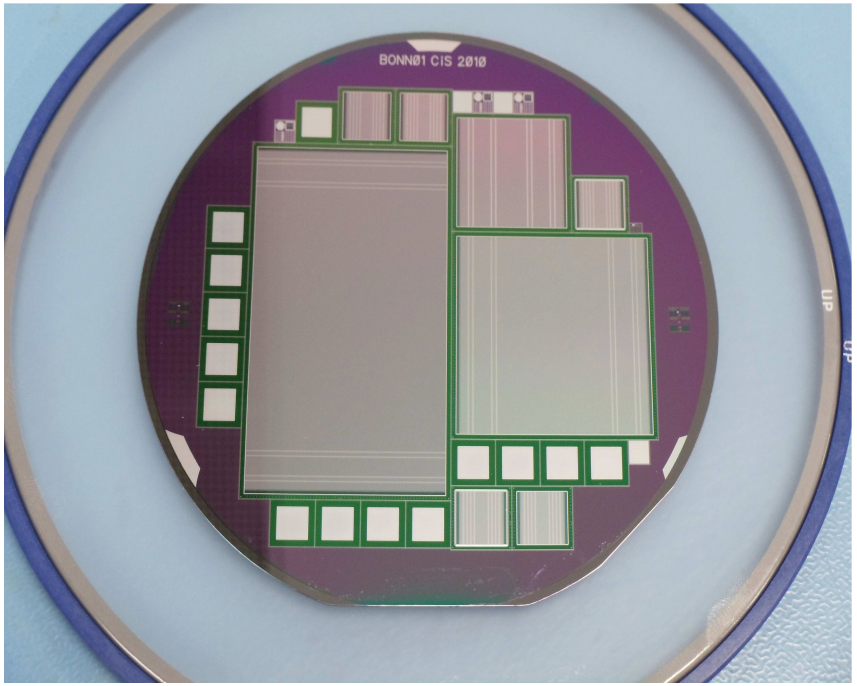
ZEA Jülich

- Cutouts at sensor position
- Prototype with cooling pipe for tests

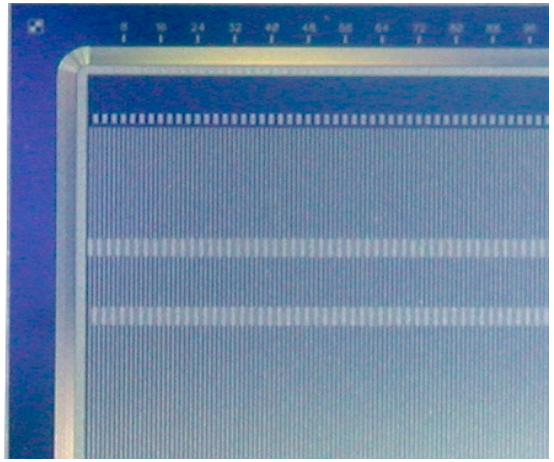


Sensors

1st prototyping run (CiS Erfurt) 2010



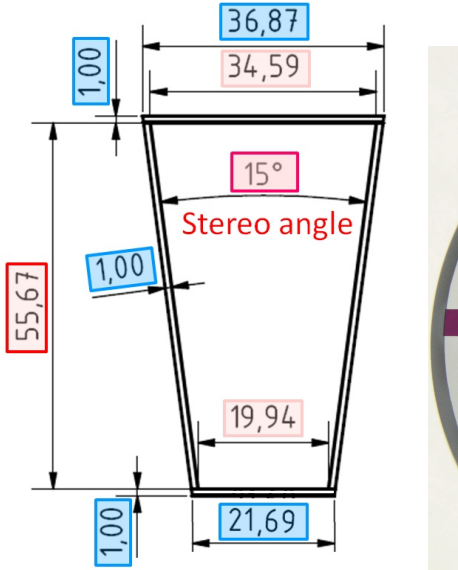
JLU Gießen



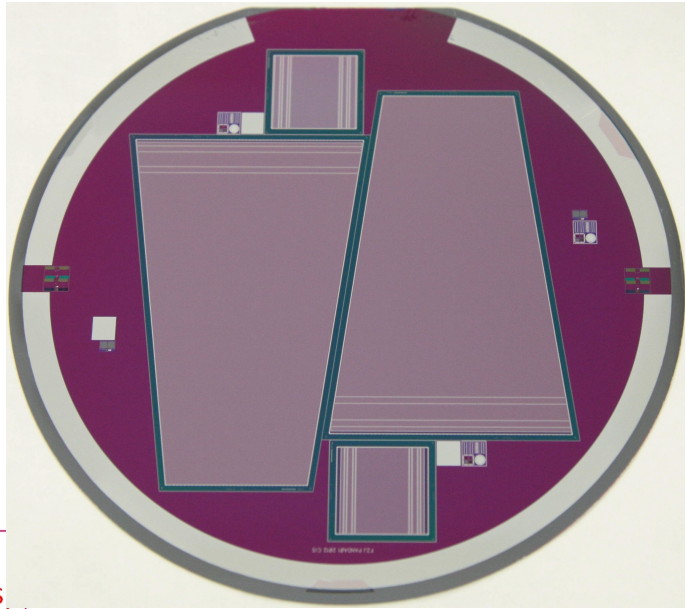
Silicon Strip Sensor Prototypes

- Full size PANDA geometry
- 285 µm thickness
- 65 and 50 µm strip pitch and 90° stereo angle (barrel sensors)
- 67.5 µm strip pitch and 15° stereo angle for trapezoidal sensors
- Punch-through biased
- 2nd run using poly-Si biasing (received July 2013)

IKP Jülich

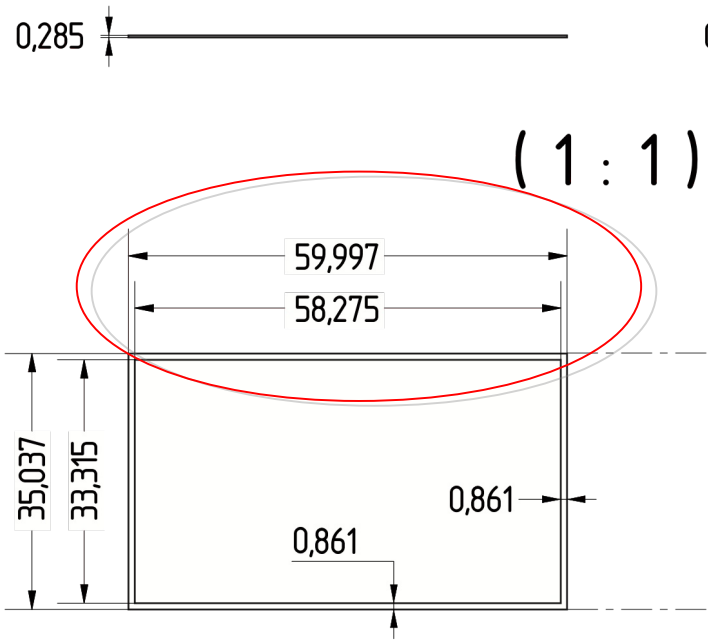


Strip pitch: 67.5 µm
No. of channels: 512 (both sides)

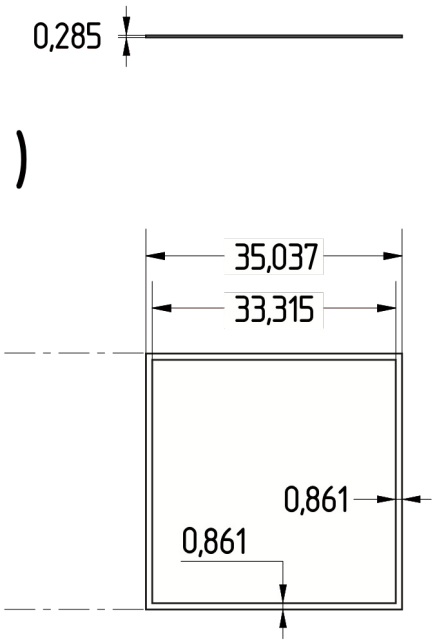


Sensors

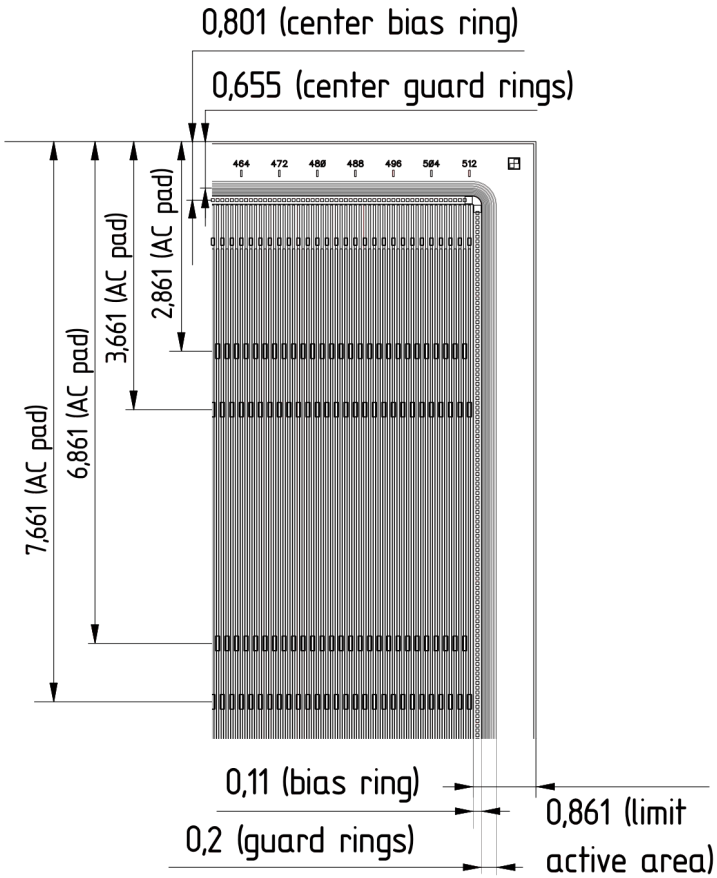
Strip_Sens_RectL



Strip_Sens_RectS



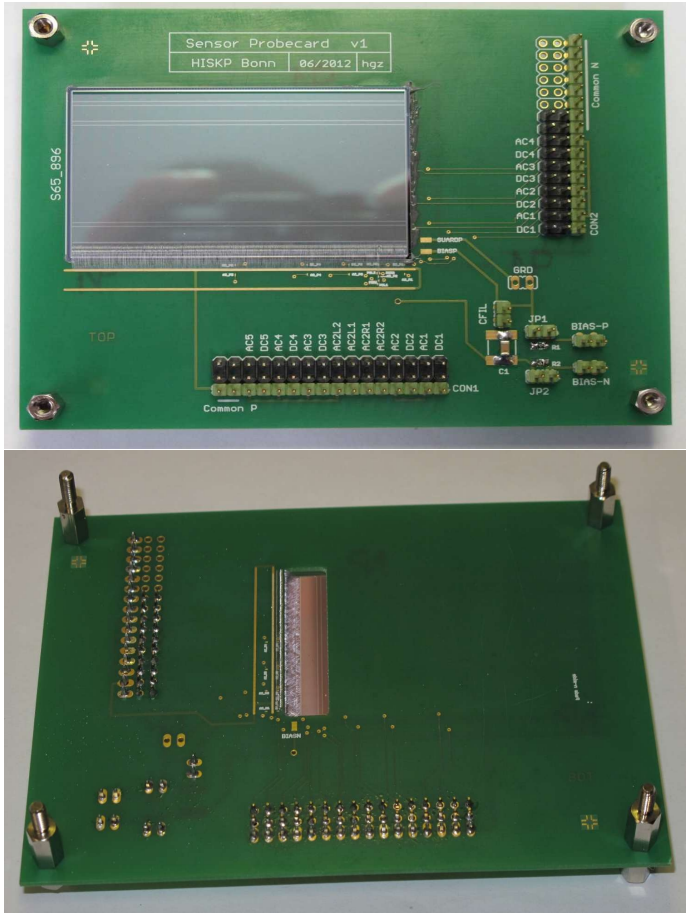
Sensor Detail (10 : 1)



Stereo angle:	90°	90°	
Pitch	0,130 (altern. 0,065)	0,130 (altern. 0,065)	
No. of channels:	448 (896) short strips	256 (512)	p-side (with Guard Ring)
	256 (512) long strips	256 (512)	n-side
No. of FE:	4 (7)	2 (4)	
	2 (4)	2 (4)	

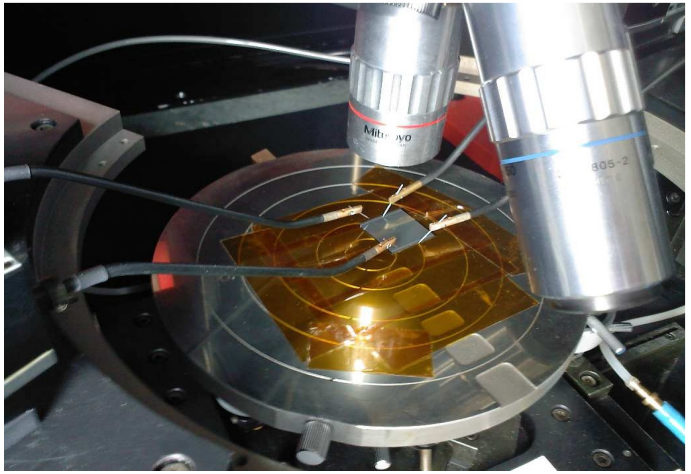
Sensors

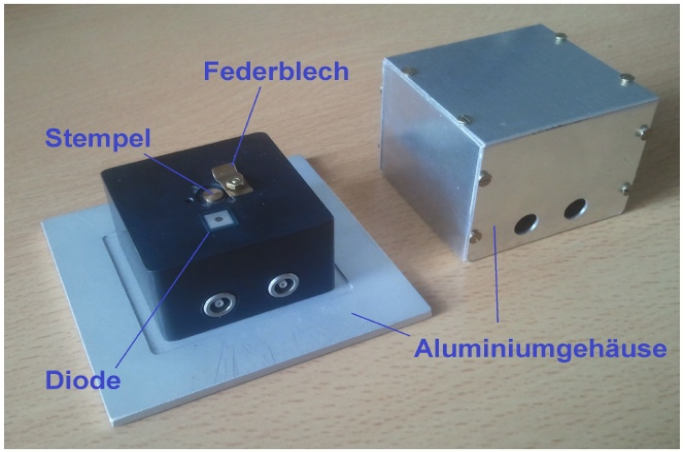
Many sensor characterization options available



"Probecard": fixed sensor assembly with all strips bonded to common lines (top and bottom)

Probe station

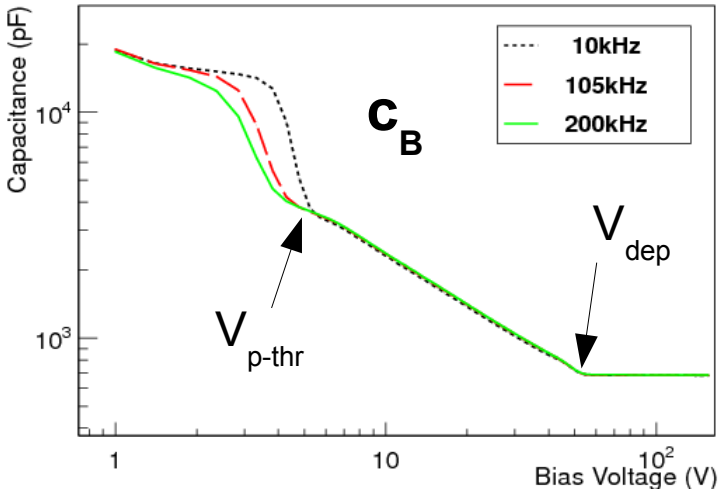


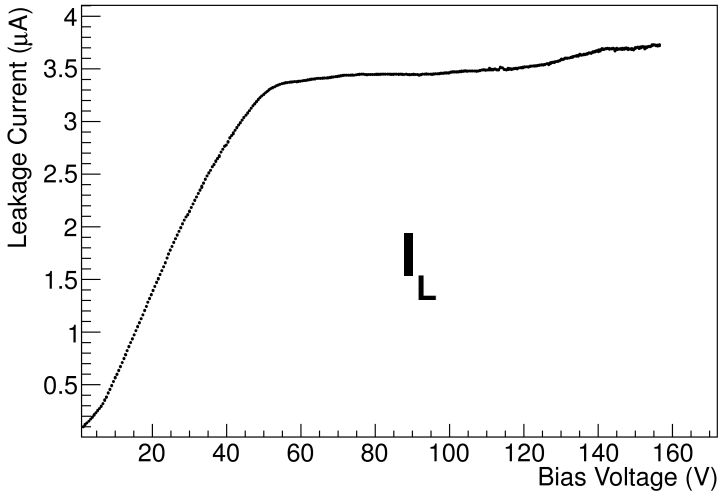


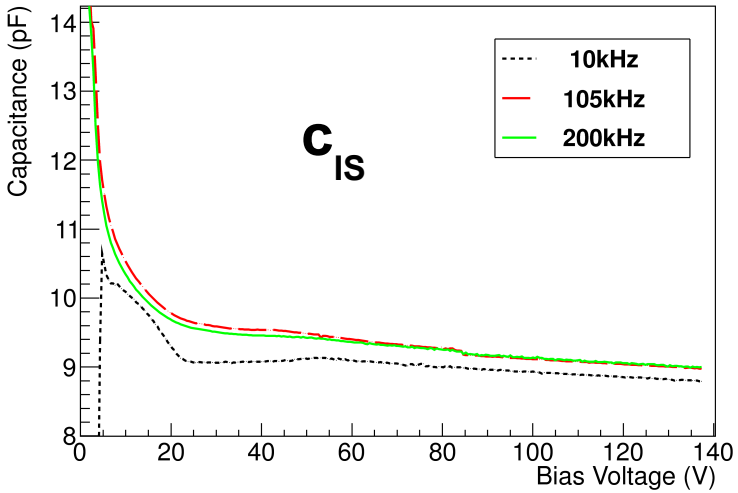
Wafer test diode fixture

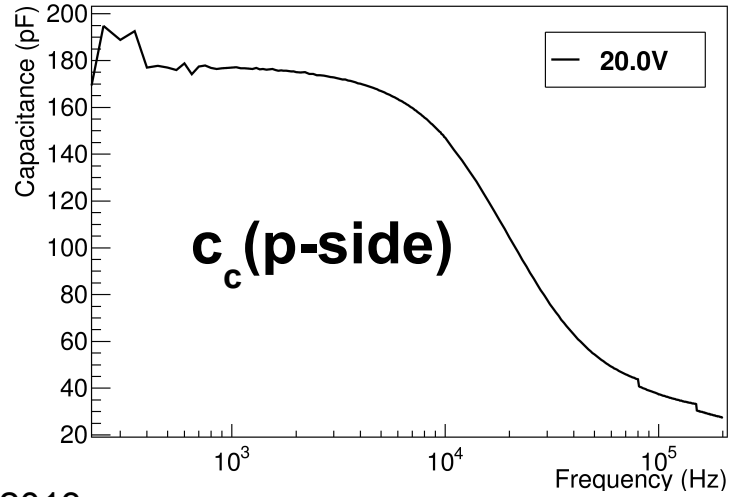
Sensors

- All relevant parameters monitored
→ full sensor characterization done
- Analysis of irradiated sensors
(proton and neutron irradiation)

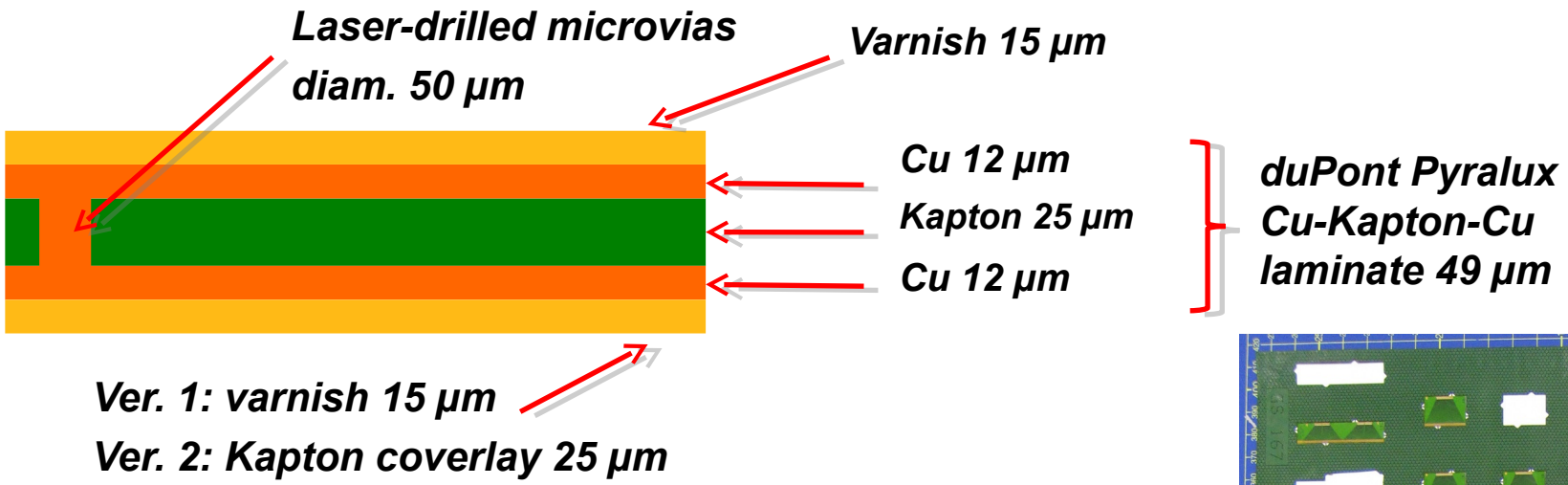


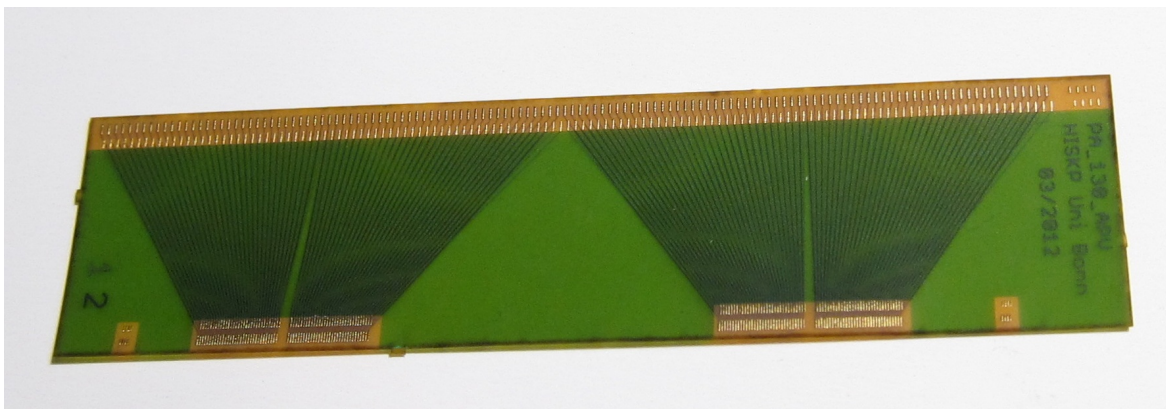


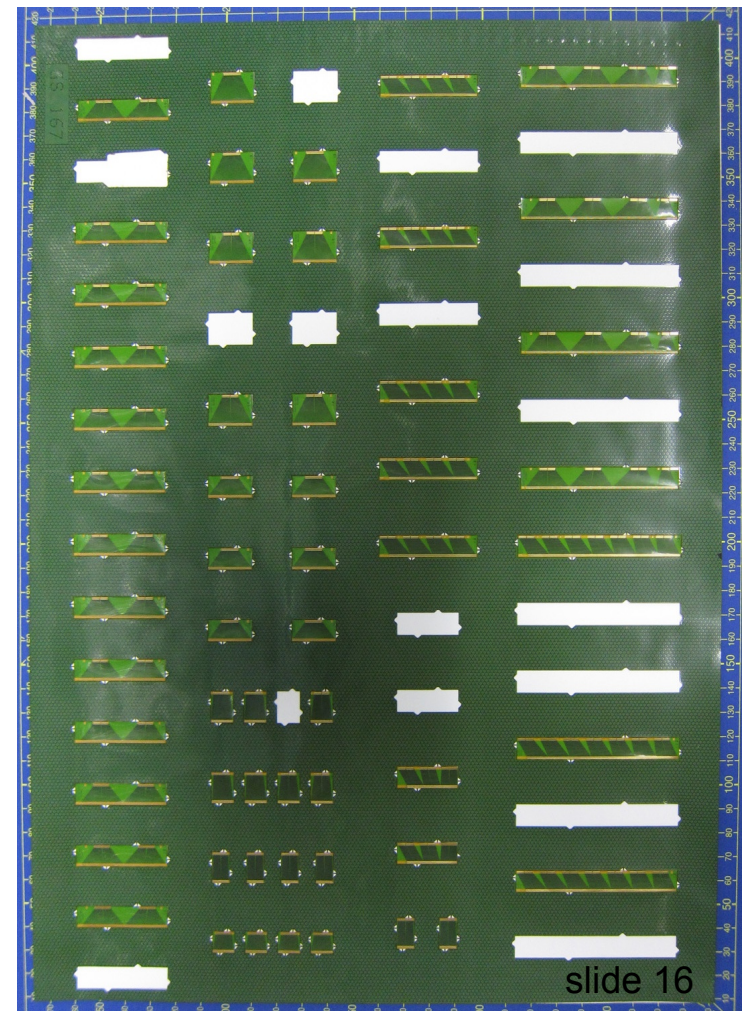




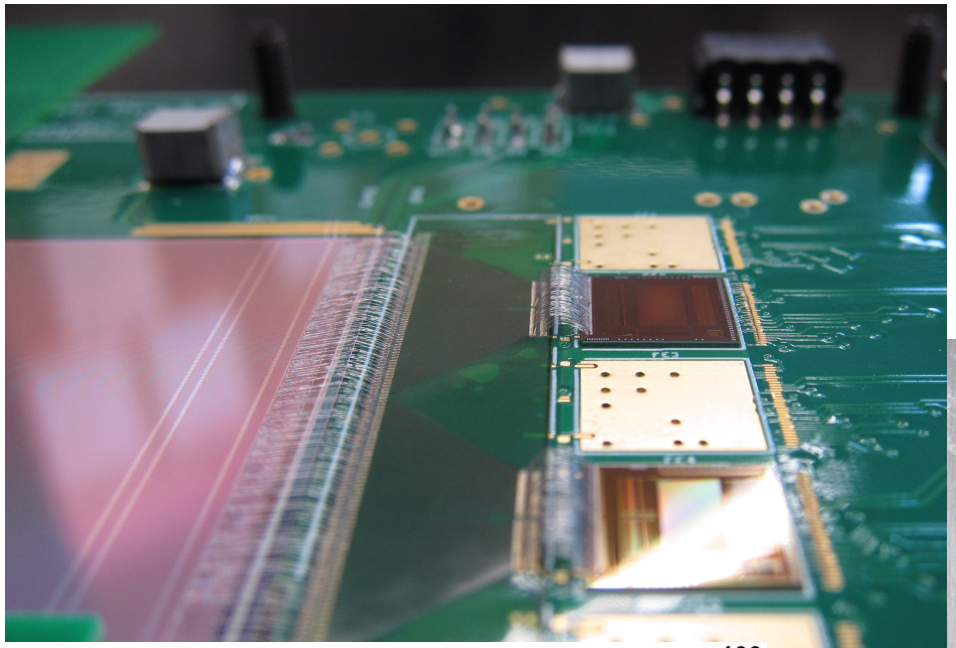
Flex Pitch-Adapters

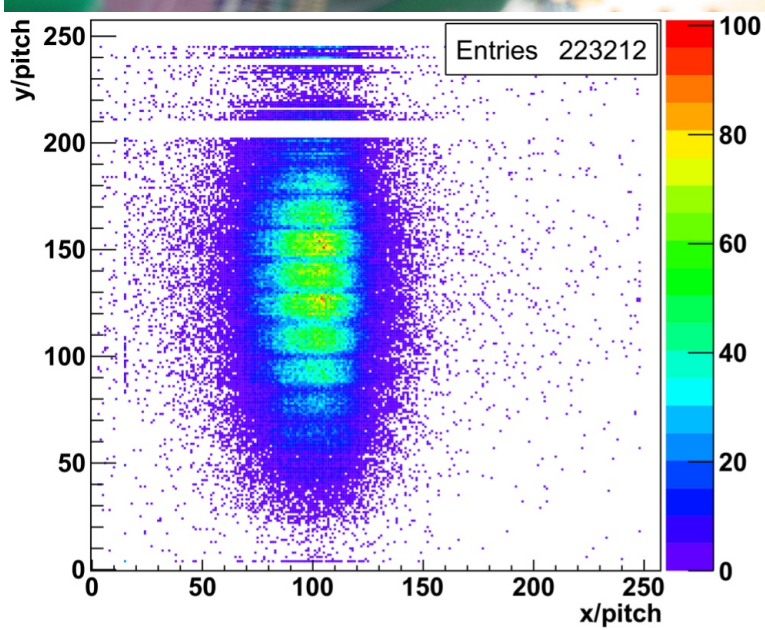




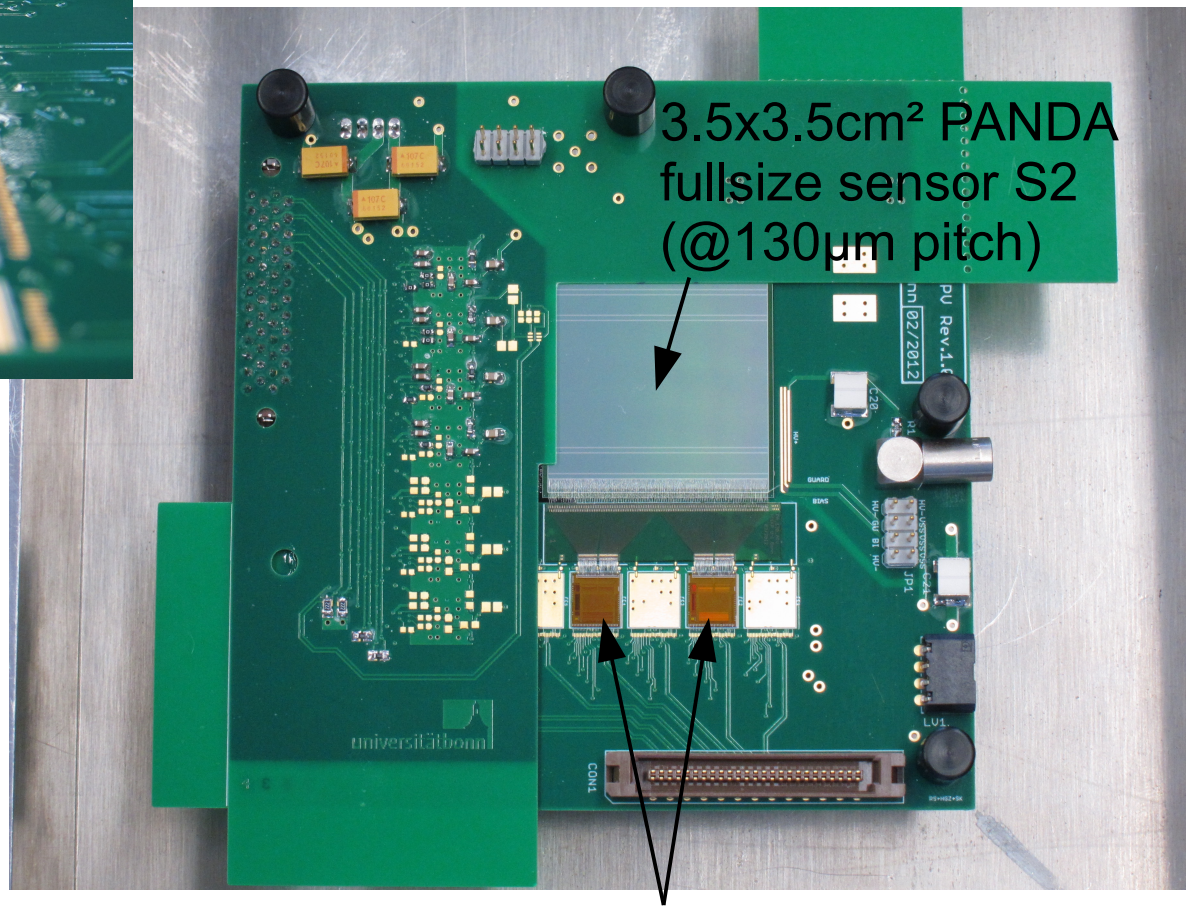


Flex Pitch-Adapters



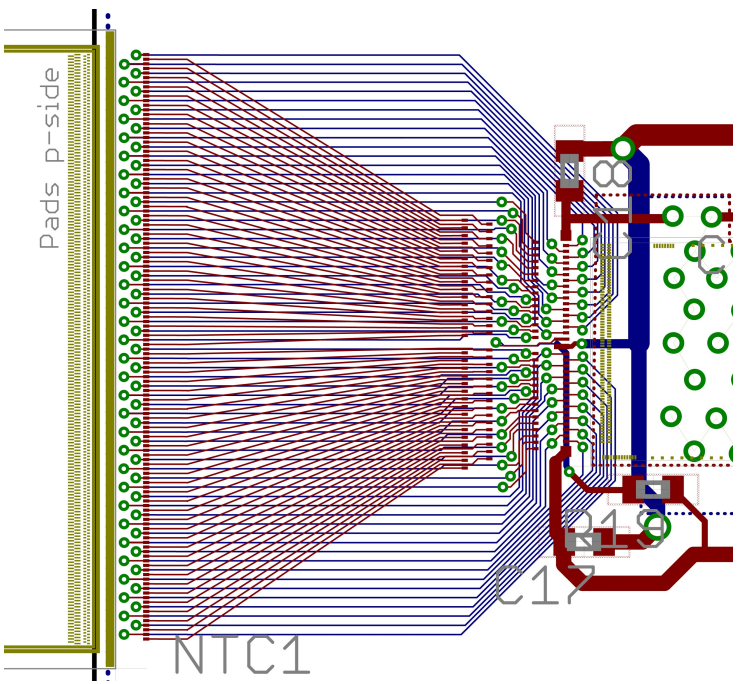


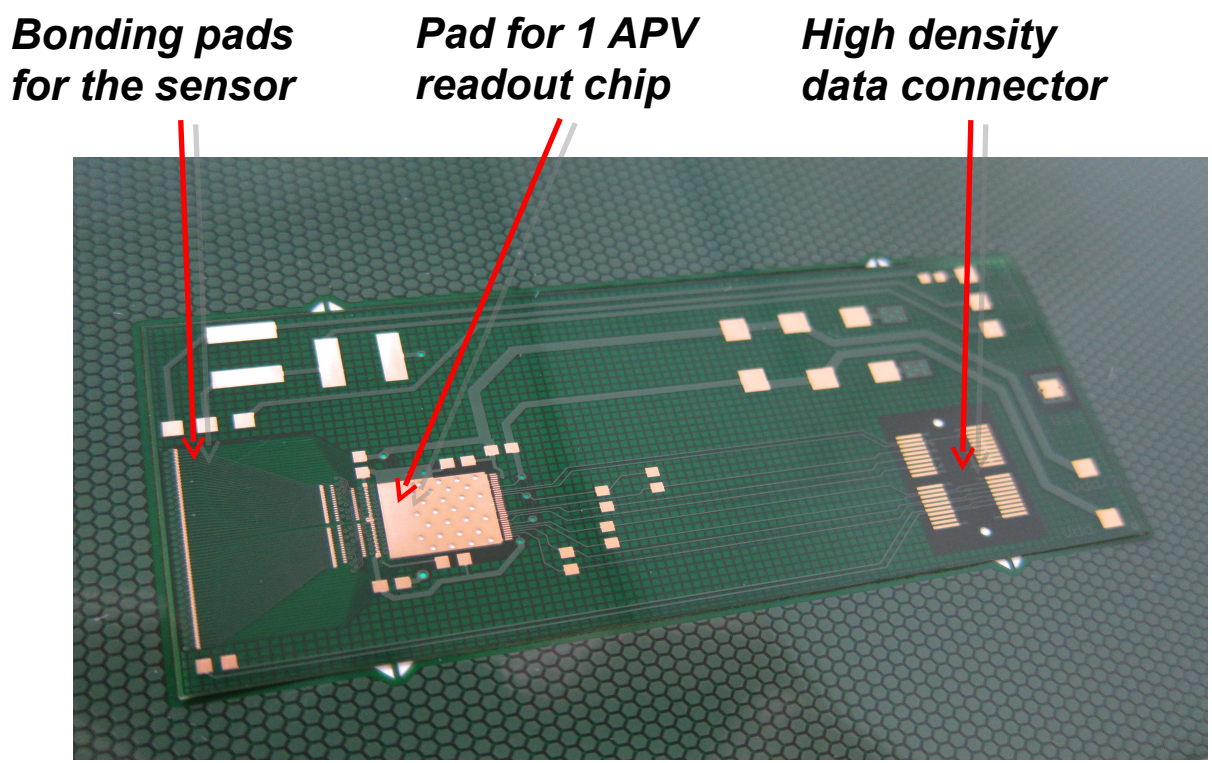
Flex pitch-adapter and squared sensor assembled on a test board and successfully tested at SPS, CERN (September 2012)



Flex PCBs

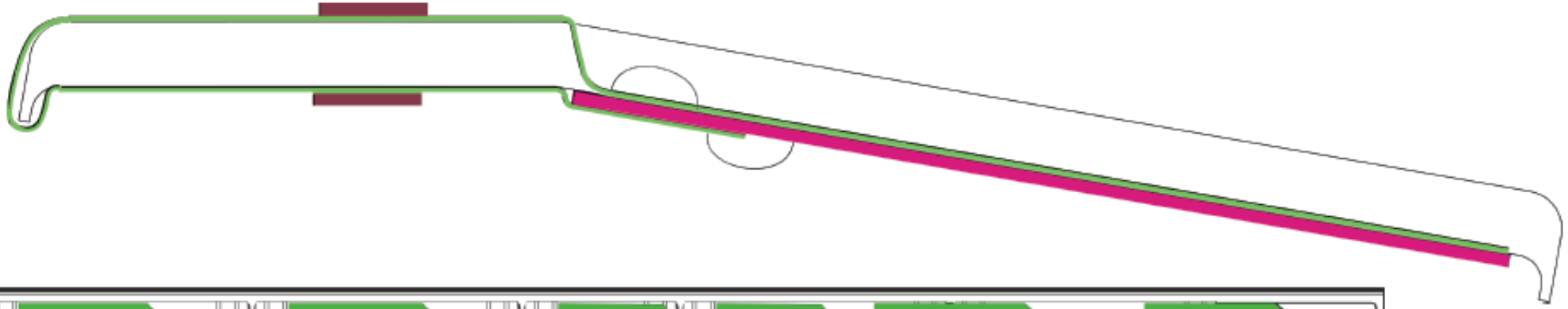

Laser-drilled microvias
diam. 200-650 µm
Varnish 15 µm
Cu 12 µm
Kapton 50 µm
Cu 12 µm
Thinflex A-2003AD
Cu-Kapton-Cu
laminate 74 µm
Varnish 15 µm

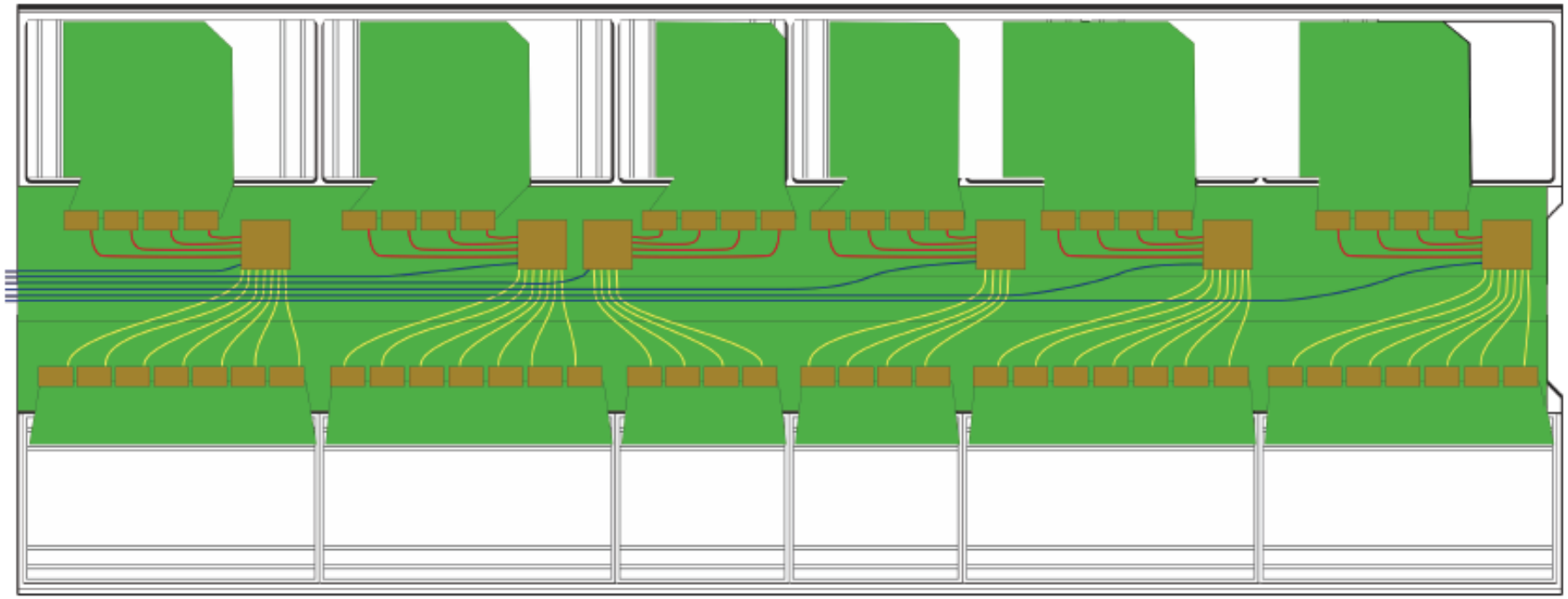

Pads p-side
NTC1


Bonding pads
for the sensor
Pad for 1 APV
readout chip
High density
data connector

Flex PCBs

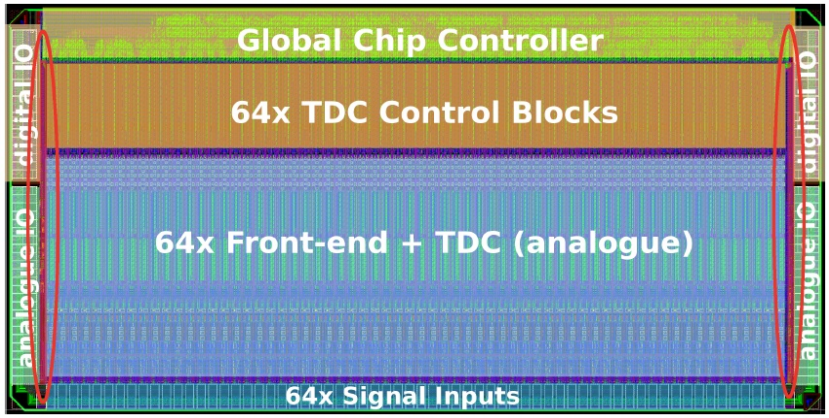
Possibility for barrel stave flex PCB:
Large flex PCB folded around the stave to permit a connection from p-side front-ends to n-side where the module controller chip is placed



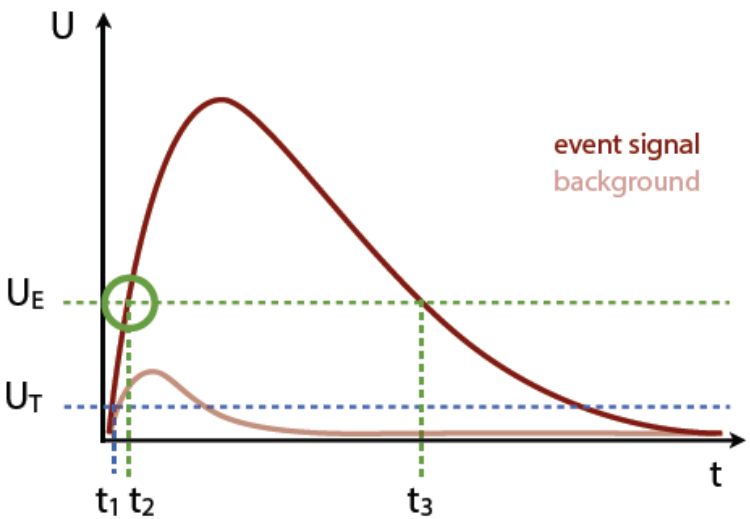


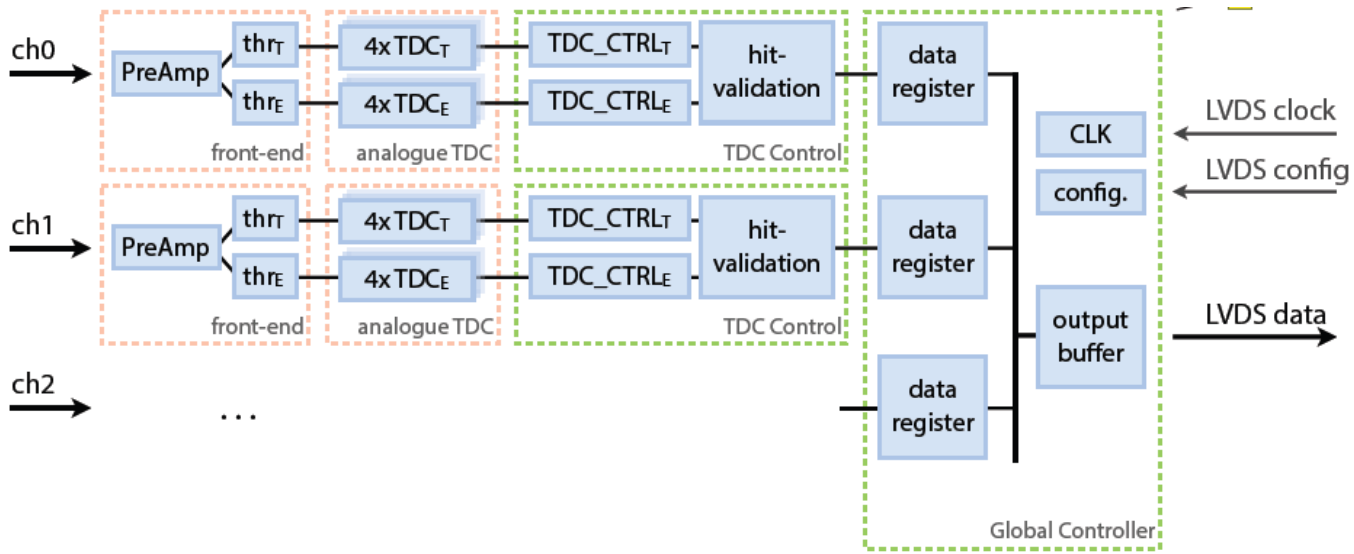
Strip Front-end

- Design of new self-triggering front-end based on TOFPEF chip started in 2012
- TOFPET: ASIC for SiPM readout of ENDO TOFPET US collaboration
- Complete redesign of the analog stage for dynamic range and capacitance of strip detectors
- 2 TDCs per channel: time and energy branch
- ToT from TDCs using analog interpolation
- Multiple TDCs for pile-up rejection
- Technology chosen: UMC 0.11µm

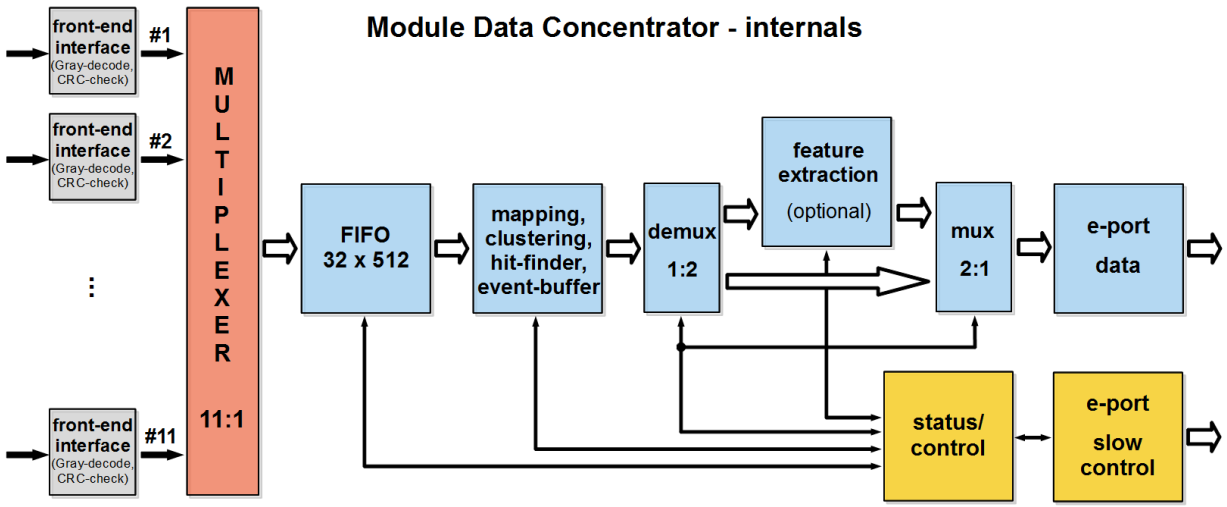


INFN Torino, JLU Giessen, IKP Jülich



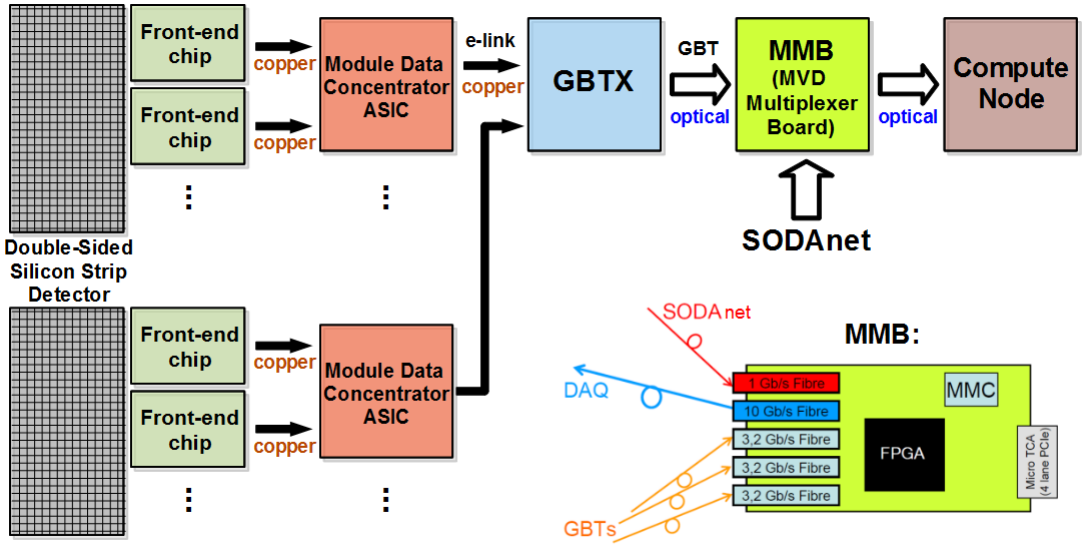


Module Data Concentrator



- On-module ASIC
- Multiplexes all front-ends of one sensor
- Feature extraction: cluster finding, cluster correlation
- Manages slow-control + calibration of attached front-ends
- Fast GBT e-link for data out + configuration data in

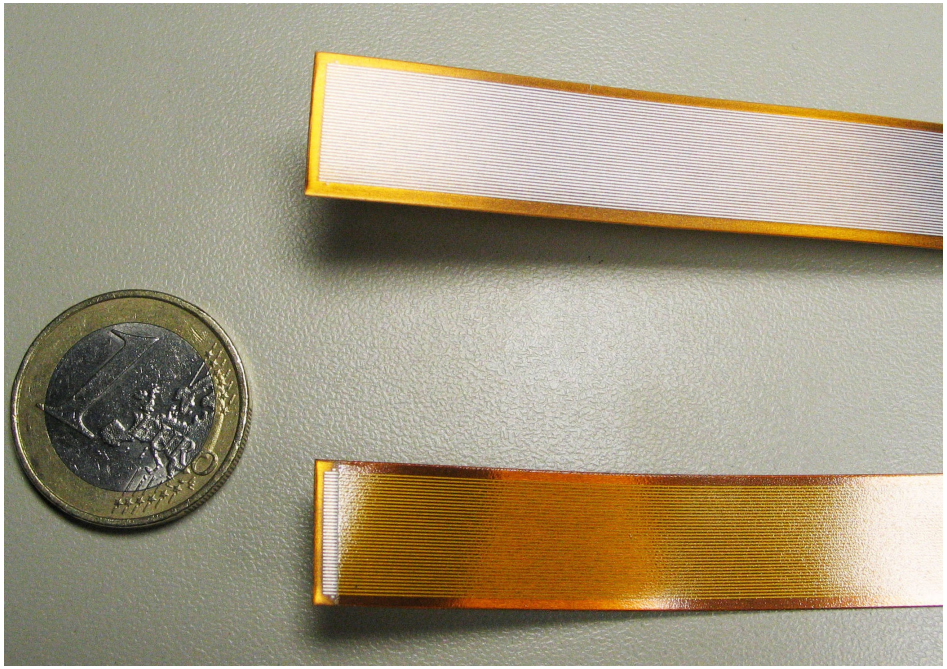
FH Südwestfalen Iserlohn



Infrastructure - Readout

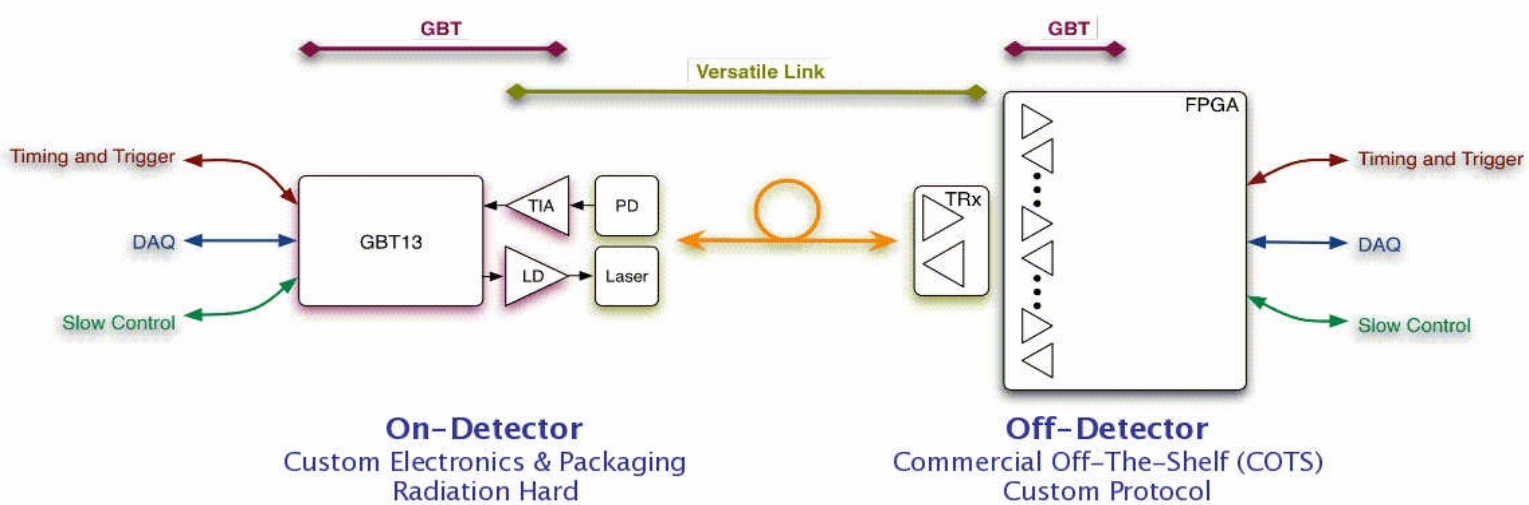
Thin Al-cables

- Thin Kapton carrier
- Aluminum strips, 18 diff. pairs
- For data transmission out of the MVD
- Connect FEs/MDC to GBT receiver
- Tested to operate beyond 320 Mbit/s



GBT Project

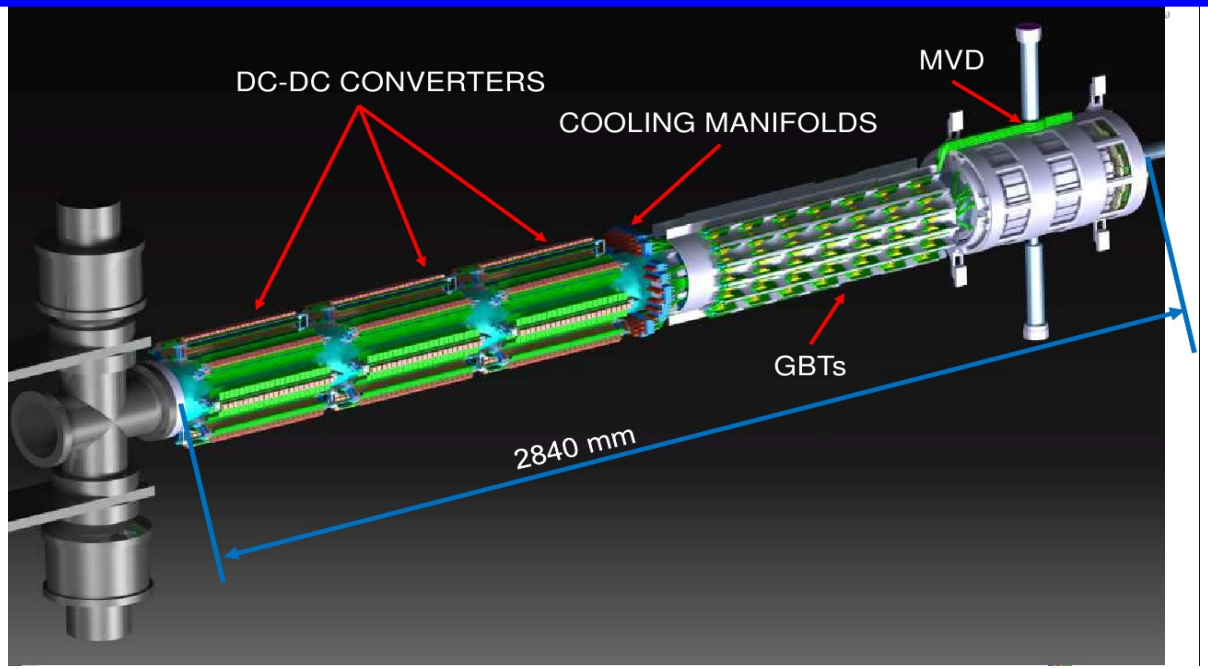
- E-link interface to on-detector node
- Optical link to the off-detector side



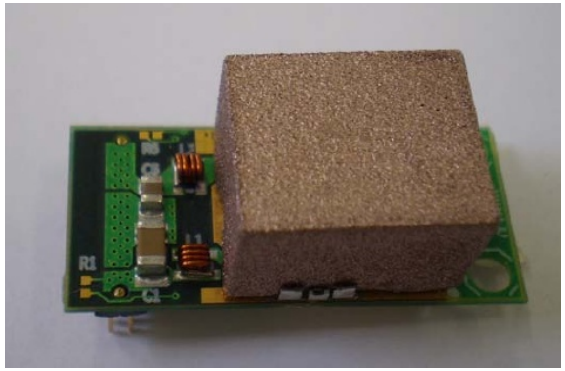
Infrastructure - Powering

DC-DC powering concept

- Switching DC-DC converters close by favored
- Air-coil converters able to operate inside strong magnetic fields as developed for sLHC
- Front-end voltages 1.2 V
- Placed along the beam-pipe
- Water-cooled

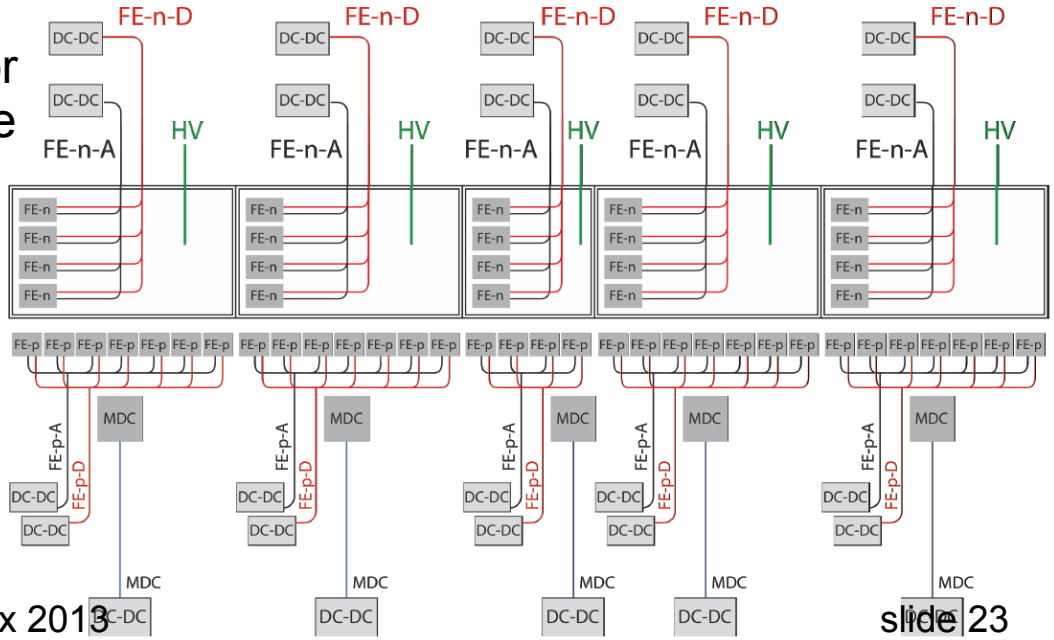


N.B. each line in this schematic has two wires!



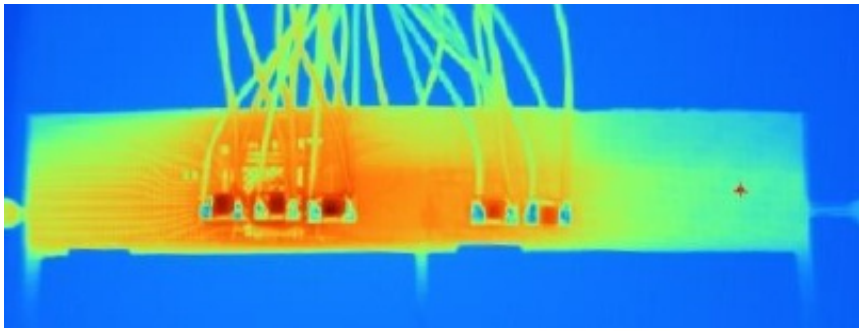
SM01C DC/DC converter

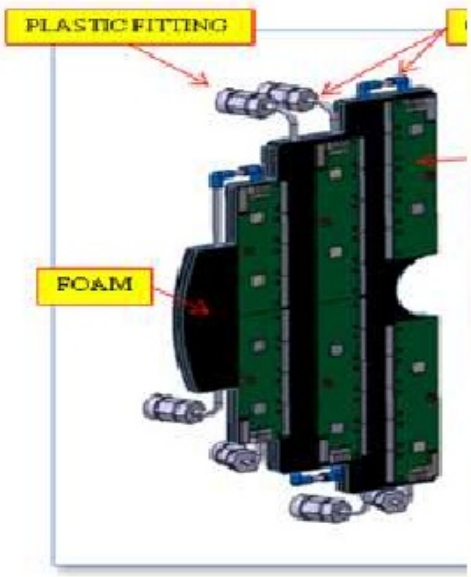
Strip sub-detector powering scheme

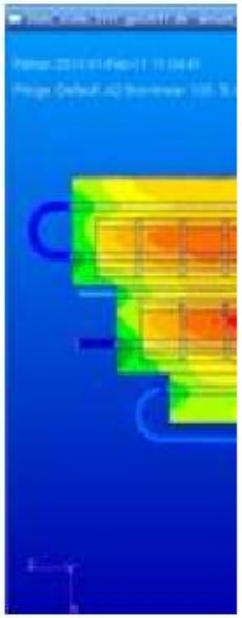


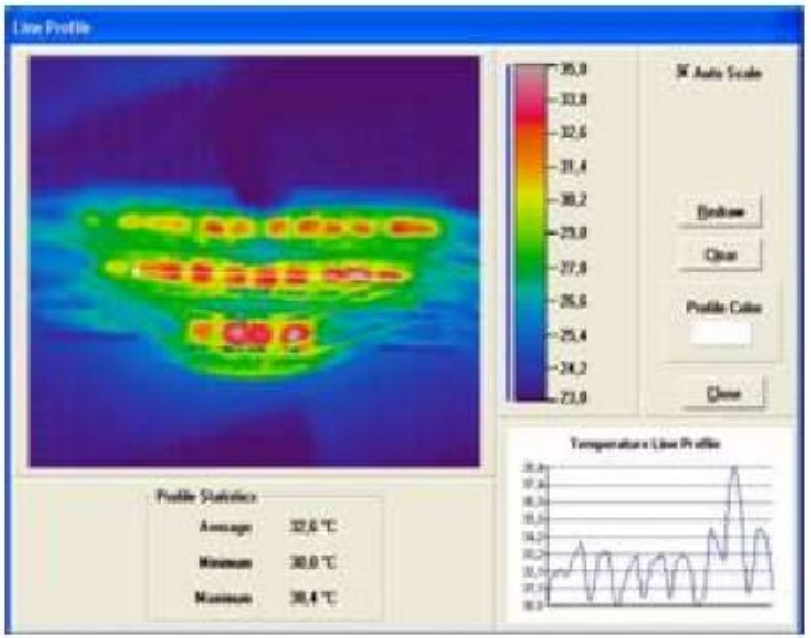
Infrastructure - Cooling

- Water cooling system in depression mode
- Operated close to room temperature (coolant approx. 16°C)
- Carbon foam embedded in staves: high thermal conductivity
- Dummy staves with thermal loads built up and scrutinized









Summary

- Design and implementation of the PANDA MVD well advanced
- Development and tests for pixel and strip sensors completed
- Methods for large-scale sensor qualification developed
- Radiation hardness studies performed
- Several successful beam tests
  - Pixel front-end prototypes together with prototype sensors
  - PANDA-size strip detectors
  - Time-stamp synchronized DAQ
- Strip front-end development well advanced
- Next step: bring all components together for full-size detector module test
- And of course: build the full detector

Thank you for your attention

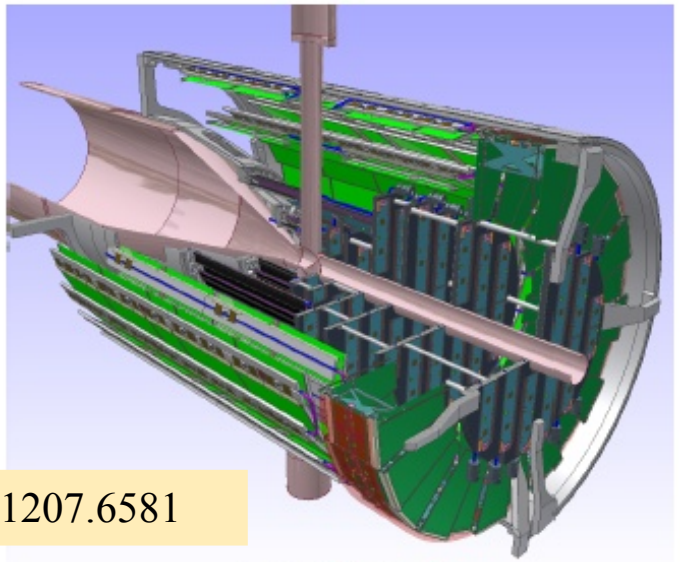
Technical Design Report for the:

$\overline{\text{P}}$ANDA
Micro Vertex Detector

(AntiProton Annihilations at Darmstadt)

Strong Interaction Studies with Antiprotons

$\overline{\text{P}}$ANDA Collaboration



arXiv:1207.6581

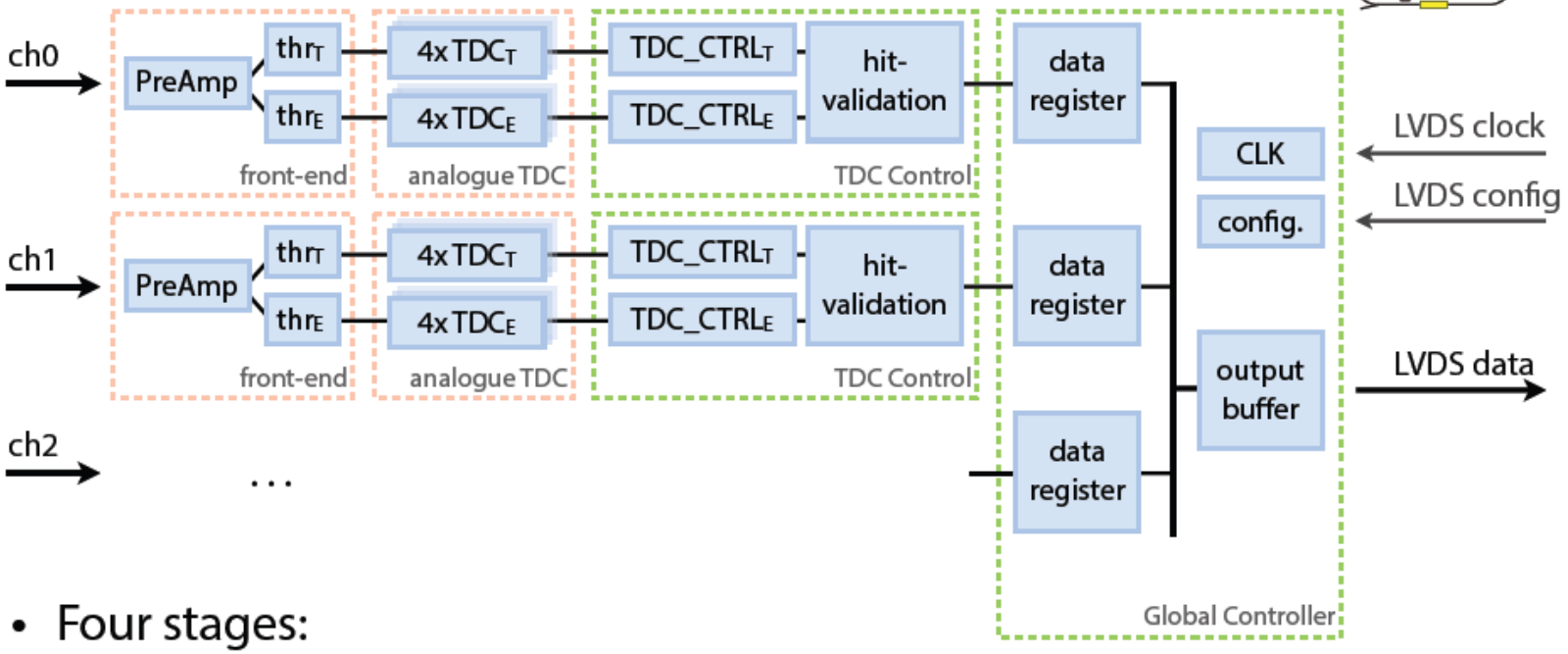
Bundesministerium
für Bildung
und Forschung

II. Physikalisches
Institut

JUSTUS-LIEBIG-
UNIVERSITÄT
GIESSEN

Backup

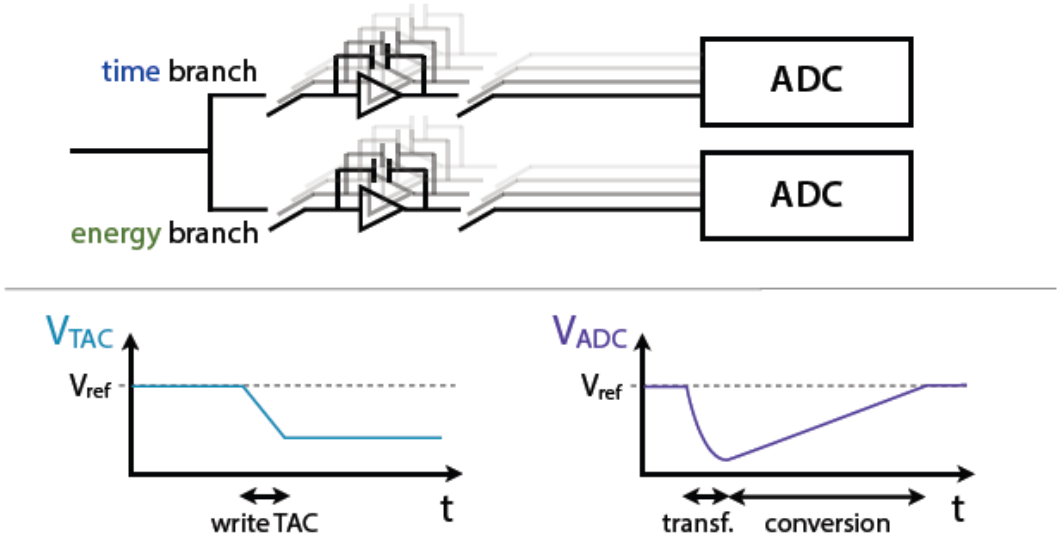
Concept of the ASIC



- Four stages:
  - **Front-end** (analogue)
  - **TDC** (analogue)
  - **TDC Control** (digital)
  - **Global Controller** (digital)

Backup

Analogue Time-to-Digital Converter



stage 1
front-end
stage 2
analogue TDC
stage 3
TDC CTRL
stage 4
global CTRL

- Two stages: buffer and convert signal
  - Buffering: discharge a capacitor (TAC)
    - Start: threshold; End: rising edge of clock*
  - Transfer to 4x larger capacitor, linearly recharge with 32/64x smaller current (Wilkinson ADC)
- Increase time resolution by 128/256x (50/25 ps @ 160 MHz)
  - Conversion takes ~ 3 µs (@128x) → buffer multiplicity of 4

ADC: Analogue to Digital Converter
TAC: Time to Analogue Converter

*: Dynamic range 1-3 clock cycles