The Readout Chain for the P̄ANDA MVD Strip Detector

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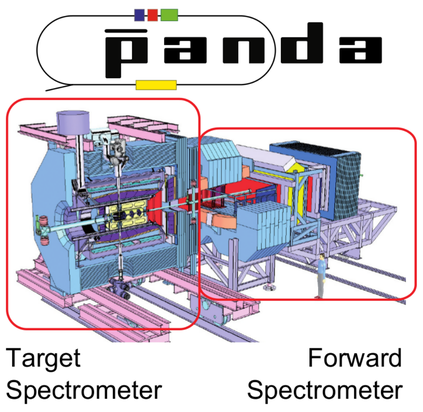
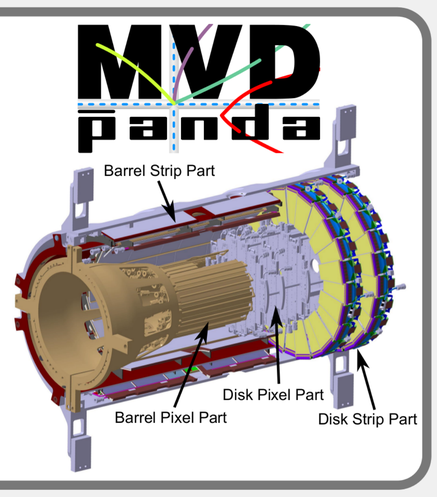
The P̄ANDA Detector

- Fixed-target experiment
- Almost 4π acceptance
- Cooled antiproton beam using
  - Electron cooling
  - Stochastic cooling
- Proton or heavy nuclear target
- Momentum from 1.5 to 15 GeV/c
- Peak luminosity of $2 \cdot 10^{32}$ $cm^{-2}s^{-1}$
- Unique self-triggering data acquisition concept



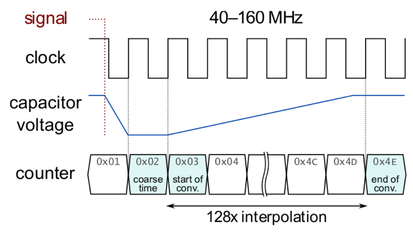
The Micro-Vertex-Detector

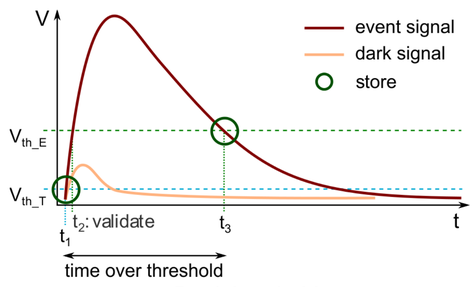
- 4 concentric barrels and 6 forward disks
- Hybrid pixel detectors
- Double-sided silicon strip detectors
- Vertex reconstruction for primary and secondary vertices
- Improvement of momentum resolution and PID
- Requirements:
  - Trigger-less readout with high rate capability
  - Good time resolution and low material budget
  - High radiation tolerance



P̄ANDA Strip ASIC (PASTA)

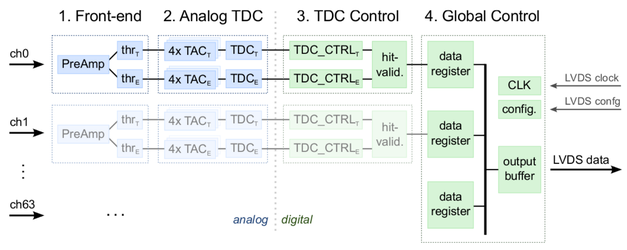
- Measurement concept inspired by TOFPET architecture
- Self-triggering, fully digital architecture
- Complete redesign of the analog stage for dynamic range and capacitance of strip detectors
- Time-over-threshold (ToT) using analog interpolators
- Multiple ToT-stages to reduce pile-up probability
- Low power consumption (goal: < 4 mW/ch)
- Precise time resolution $\mathcal{O}$(100 ps)

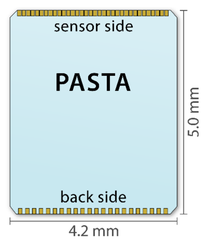




Dual threshold concept

- Submission planned for end of this year
- Employ commercial 110nm CMOS technology



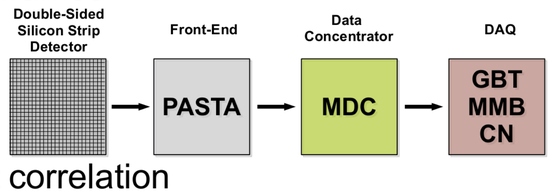


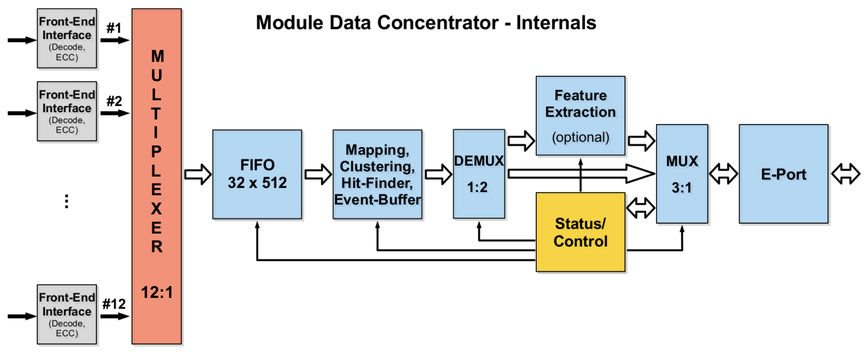
Planned geometry of the 64 channel chip

- Joint development of:
  - University Gießen
  - Forschungszentrum Jülich
  - INFN Torino

Module Data Concentrator (MDC)

- Data Concentrator ASIC at the stave level
- Multiplexes all front-ends of one sensor
- Decoding of front-end data frames
- Time-ordering of data
- Feature extraction:
  - Mapping
  - Cluster finding
  - Optional 2-dimensional hit correlation
- Slow control interface to front-end chips
- Interfacing DAQ via serial GBT E-links
- Will be produced in the same commercial 110nm CMOS technology as PASTA
- Triple redundancy for all critical components
- Tests/device simulations in progress
- ASIC design carried out at FH-SWF, Iserlohn

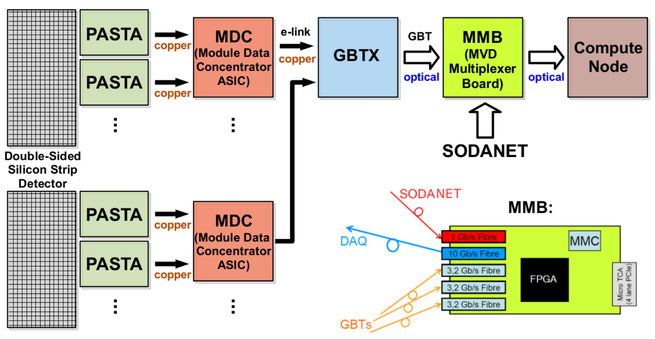




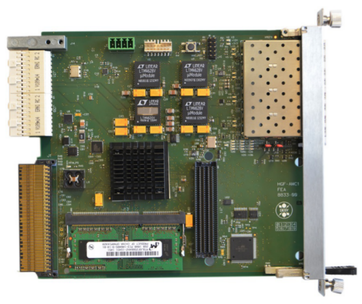
Block diagram of the Module Data Concentrator

Data Acquisition

- Up to $2 \cdot 10^7$ events/s requires fast and effective DAQ
- Objective: reduce length and amount of copper lines
  → Use fast optical data links: GBT (CERN)
- GBT multiplexes MDC to off-detector electronics
- MVD Multiplexer Board (MMB)
  - Off-detector electronic of the MVD
  - MTCA.4 compatible AMC module
  - Based on Kintex 7
  - Receives 3 GBT links
  - Implements link to time distribution system (SODANET)
  - Links to Compute Nodes with up to 10 Gbit/s
- Development of GBT protocol implementation for prototype test systems started
  - To be tested with GBT board, soon



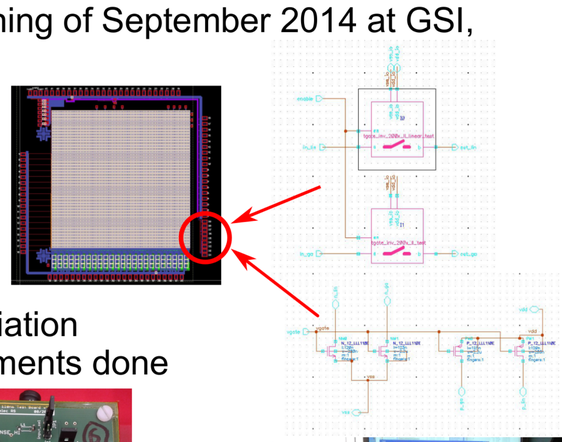
Scheme of the readout chain from the detector level to the event builder farm

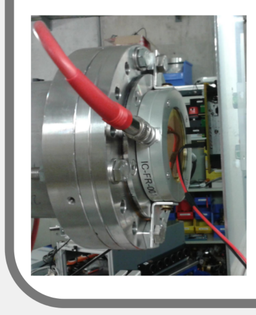


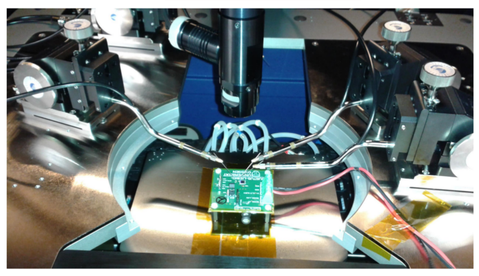
HGF-AMC (DESY/KIT)

Irradiation of 110nm CMOS Technology

- Test chip from PSI, Switzerland with 6 test structures:
  - NMOS linear and enclosed-layout transistor,
  - PMOS linear and enclosed-layout transistor,
  - Transmission gate array with linear transistors and with enclosed-layout transistors
- 10 chips irradiated beginning of September 2014 at GSI, Darmstadt with ^{132}Xe ions
- Doses applied:
  - 0.3 MRad
  - 1.0 MRad
  - 4.0 MRad
  - 10.0 MRad
  - 20.0 MRad
- Chips biased during irradiation
- Post-irradiation measurements done
- Analysis ongoing







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FAIR

HIC for FAIR Helmholtz International Center

Bundesministerium für Bildung und Forschung

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