Sezione di Torino

ToPiX : a CMOS 0.13 μm Silicon Pixel Readout ASIC for the PANDA Experiment

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Outline

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- The PANDA Micro Vertex Detector
- Readout architecture
- The ToPiX ASIC
- ToPiX prototype
- Test results
- Conclusions

The PANDA experiment

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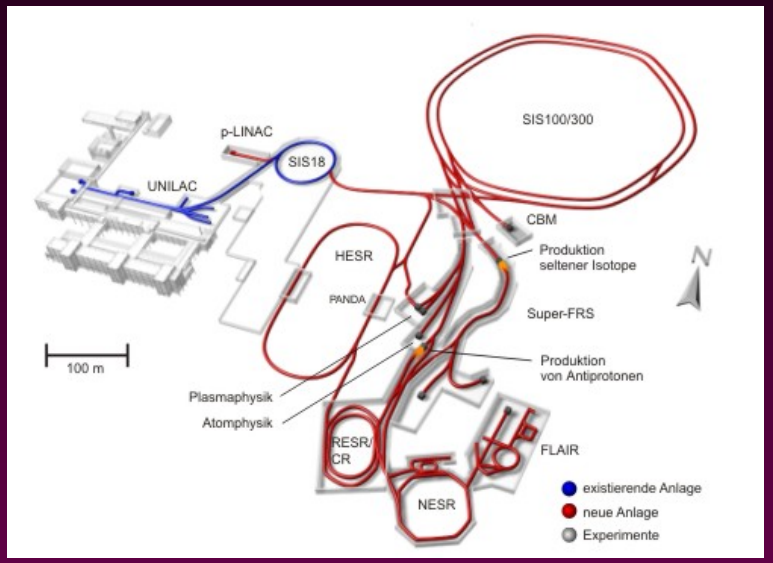

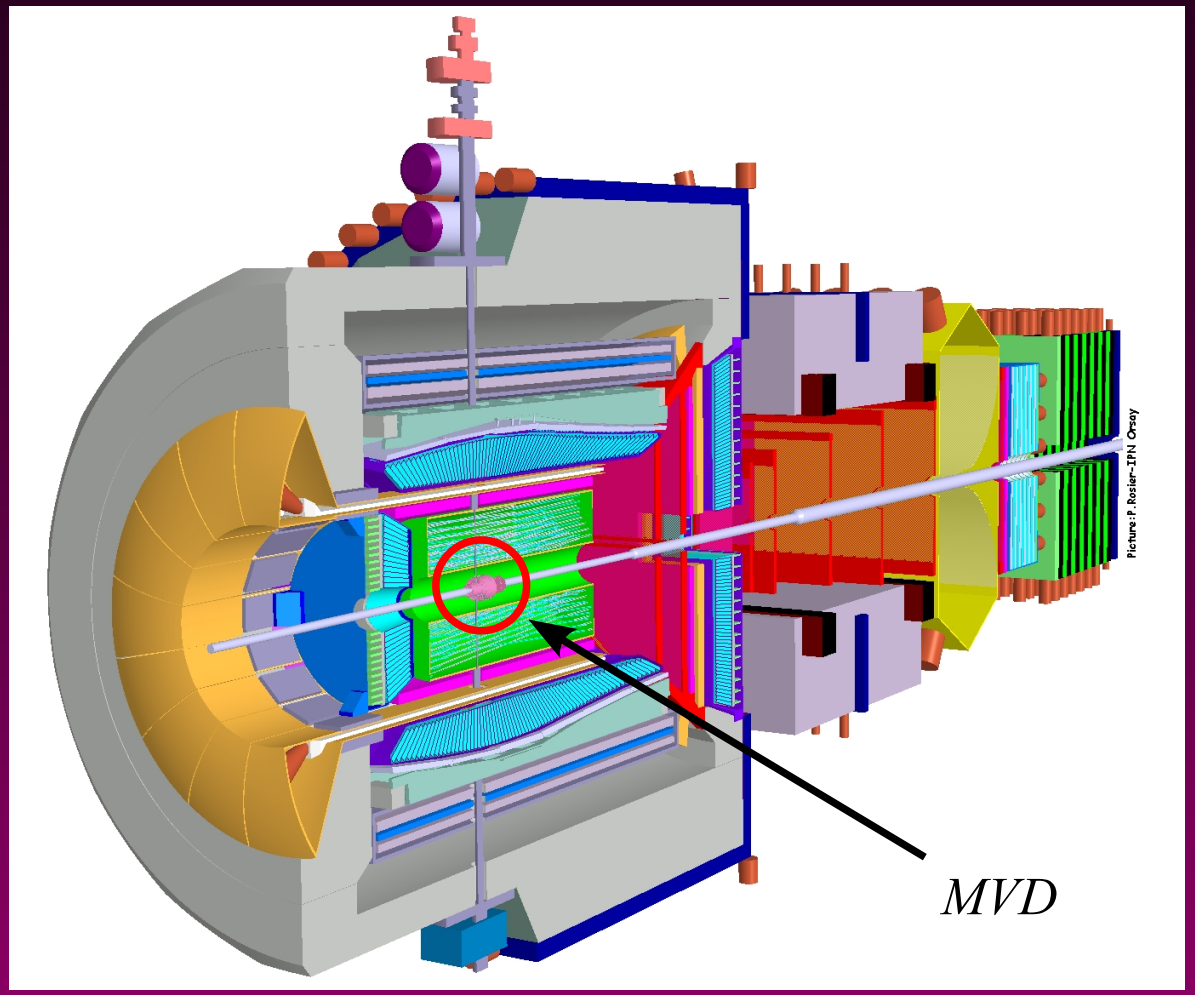

Located at the new FAIR facility
p-p and p-nucleous annihilation reaction
Beam and target pipe
No trigger

PANDA MVD

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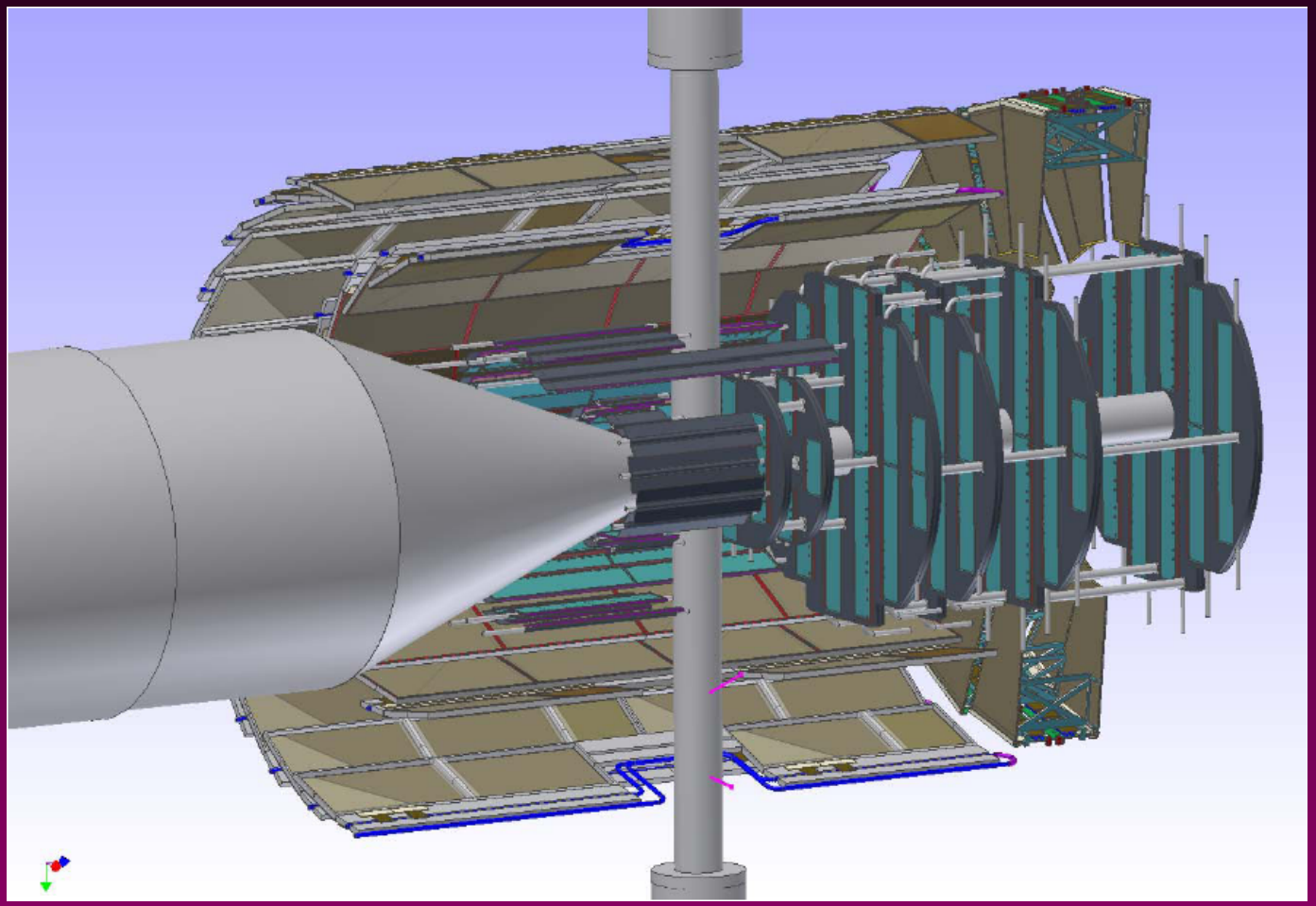

- Barrel :

Layer 1 : radius 28 mm, SPDs

Layer 2 : radius 53 mm, SPDs

Layer 3 : radius 92 mm, SSDs

Layer 4 : radius 120 mm, SSDs

- Forward :

Disks 1-2 : radius 37.5 mm, SPDs

Disks 3-4 : radius 75 mm, SPDs

Disks 5-6 : radius 130 mm, SPDs + SSDs

Pixel specs

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Pixel size	$100 \times 100\ \mu m^2$
Chip active area	$11.4 \times 11.6\ mm^2$ (116 rows, 110 cols)
dE/dx measurement	ToT, 12 bits dynamic range
Max input charge	50 fC
Noise floor	<32 aC (200 e^-)
Clock frequency	155.52 MHz
Time resolution	6.45 ns (1.9 ns *r.m.s.*)
Power consumption	< 750 mW/cm^2
Max event rate	$6 \cdot 10^6$ *events/s*
Total ionizing dose	< 100 kGy

ToPiX ASIC

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- Custom development for the PANDA MVD
- Provides spatial and time coordinates plus energy resolution measurement (via ToT)
- Compatible either with p-type or n-type detectors
- Self triggered architecture
- Each event has a 12 bits time reference
- Double rate serial readout
- Radiation tolerant
- Data corresponding to a 12 bits counter cycle (26.21 μs) are packed in a frame, with an 8 bits frame counter (6.71 ms cycle)

Pixel cell

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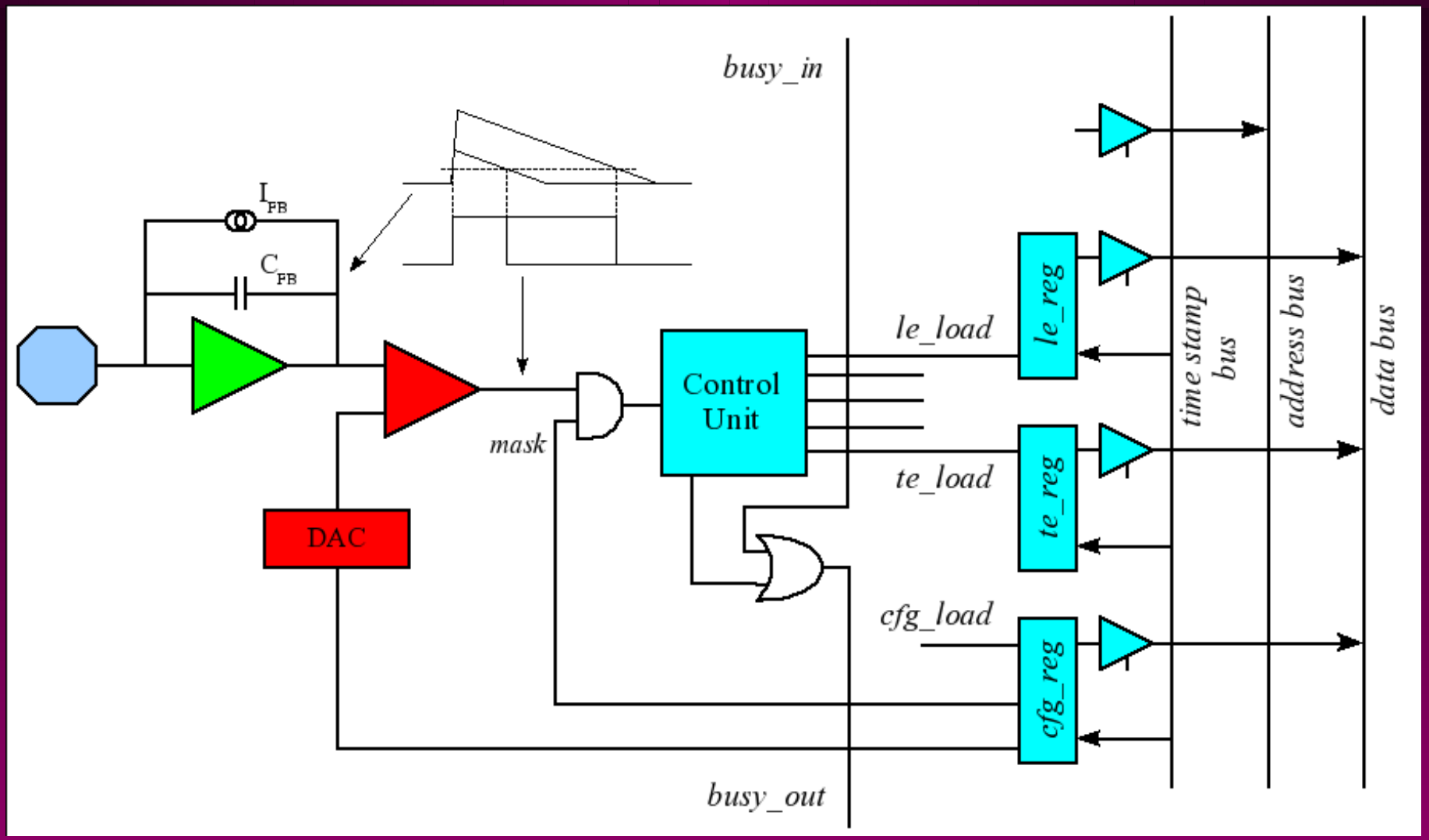
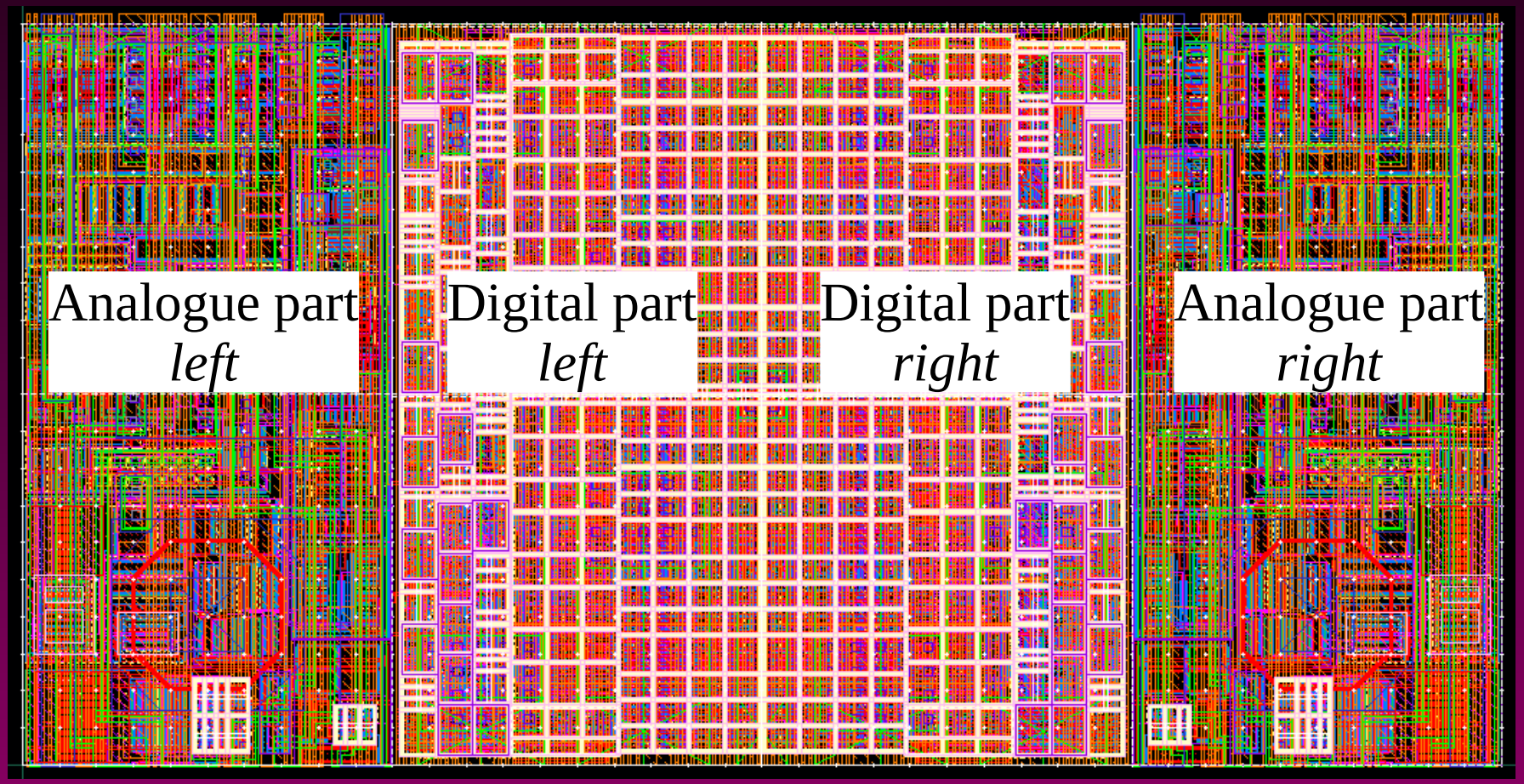


Double cell



Common bus

EoC readout

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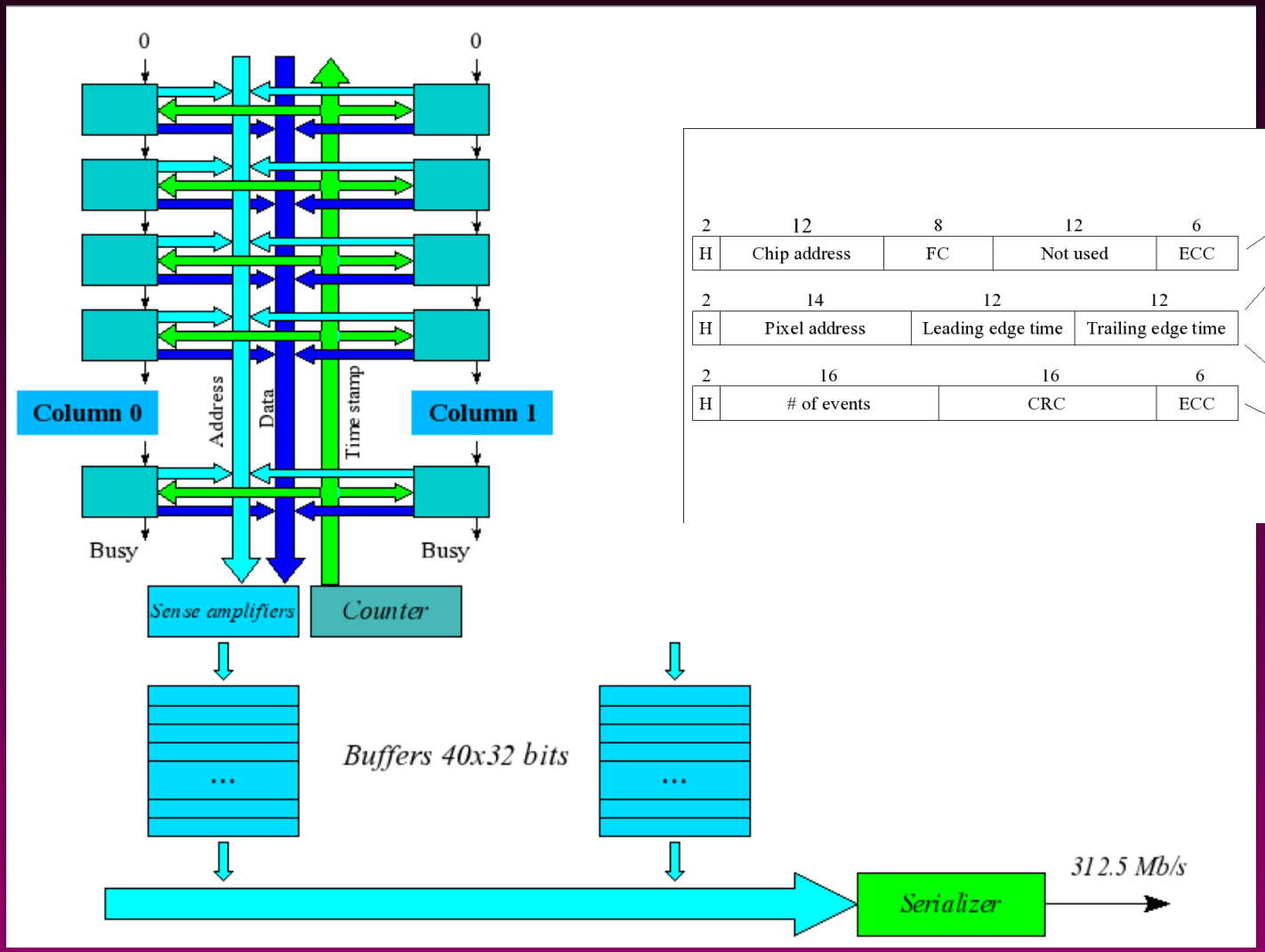

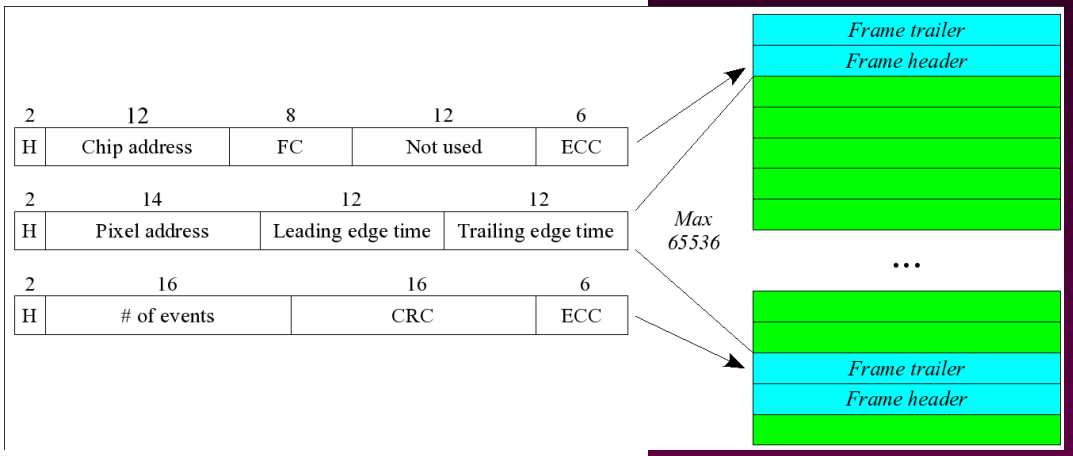

SEU protection

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- Pixel data register : triple redundancy (area : 75 μm^2/bit)
- Pixel config register : triple redundancy with asynchronous self correction (area : 145 μm^2/bit)
- EoC control logic : Hamming encoding with synchronous self correction
- EoC FIFO Hamming encoding with output decoding and correction only

ToPiX v3 layout

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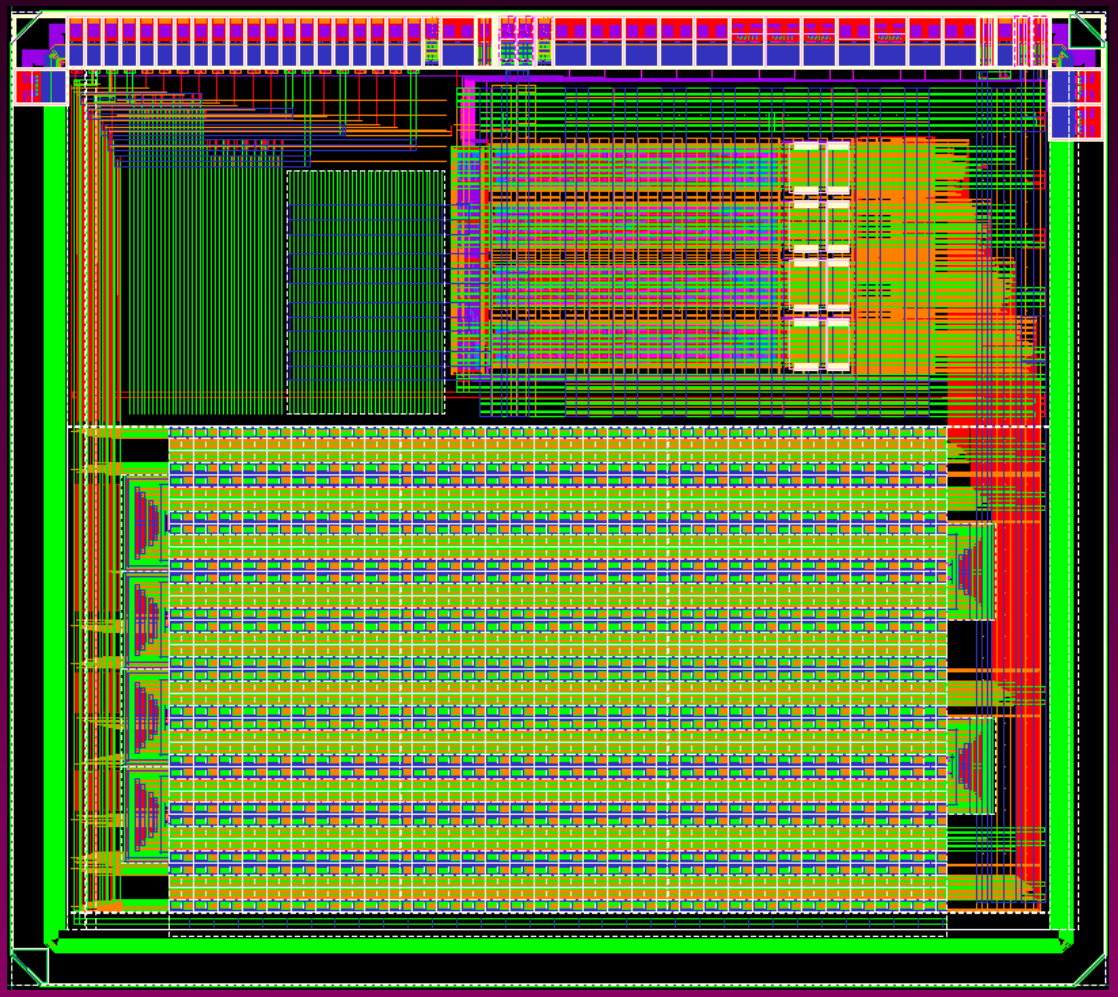

- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

Test system

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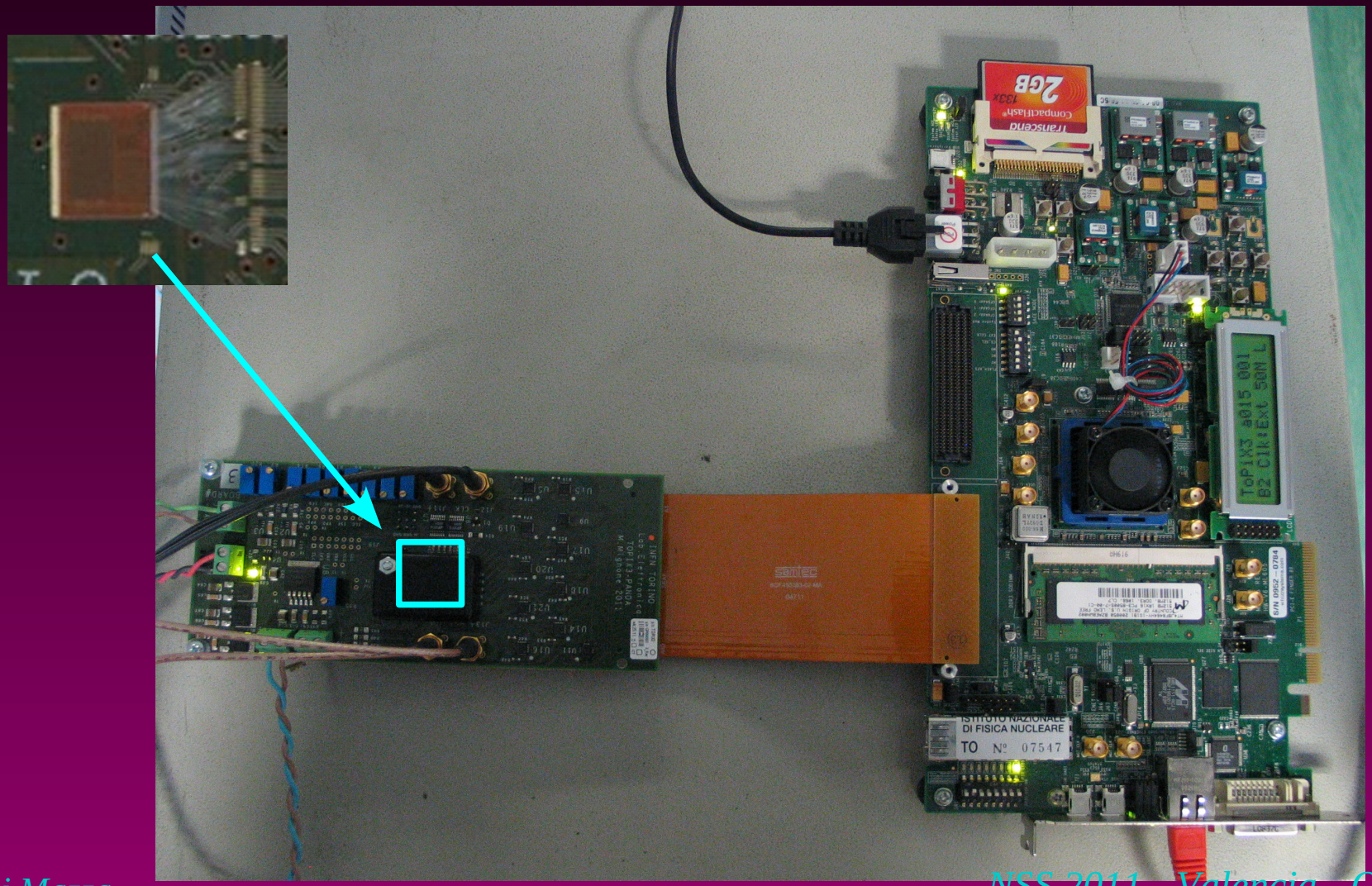

Pixel map

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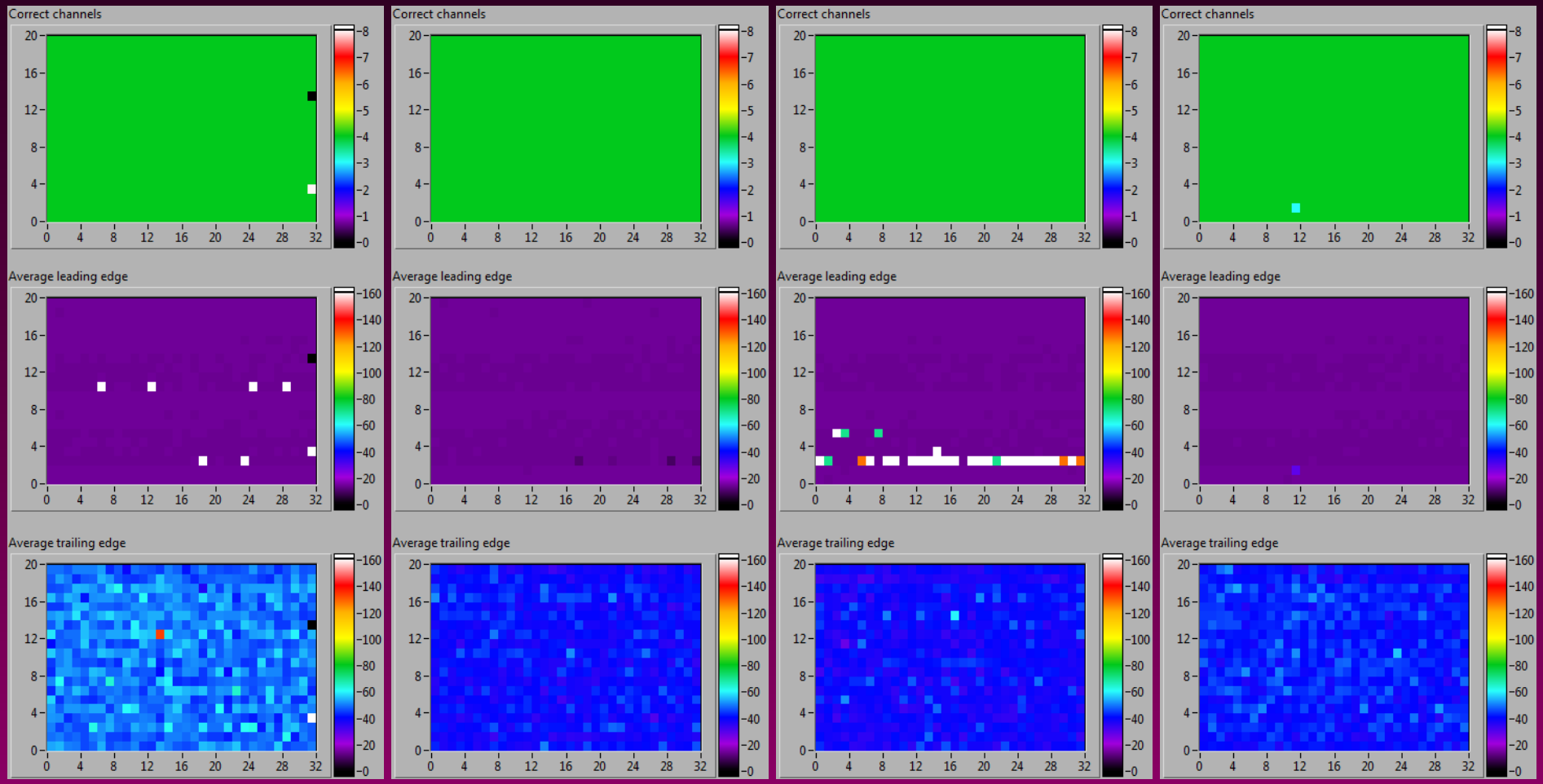
Chip 1 *Chip 2* *Chip 3* *Chip 4*



Baseline

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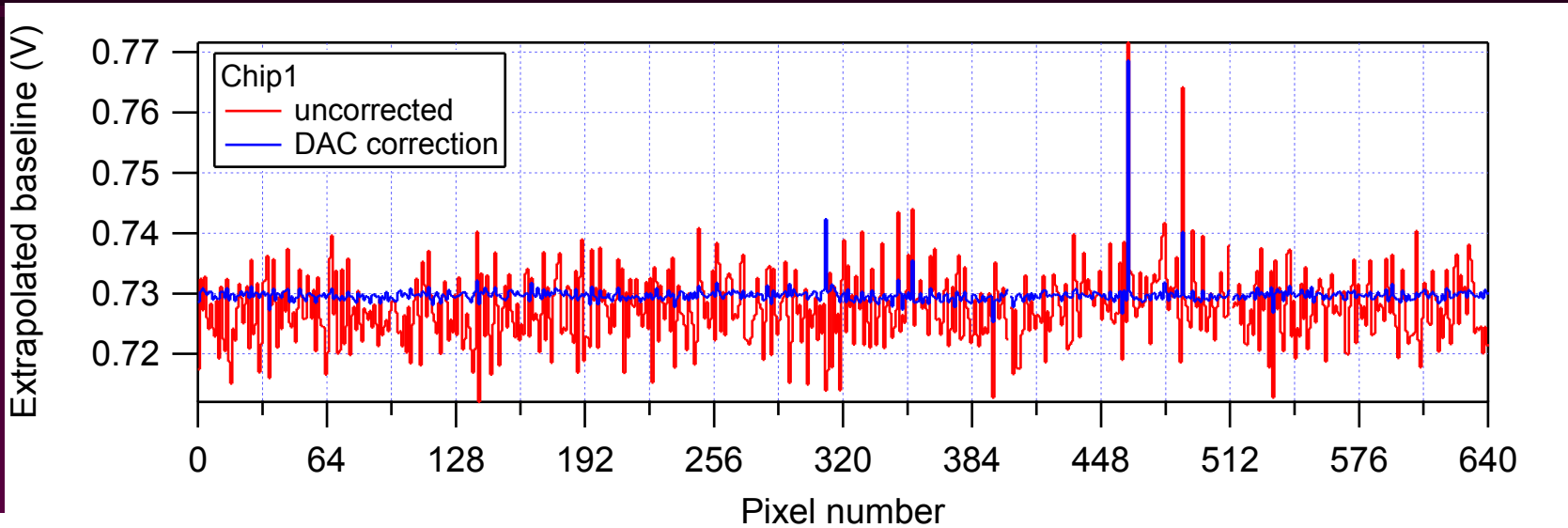
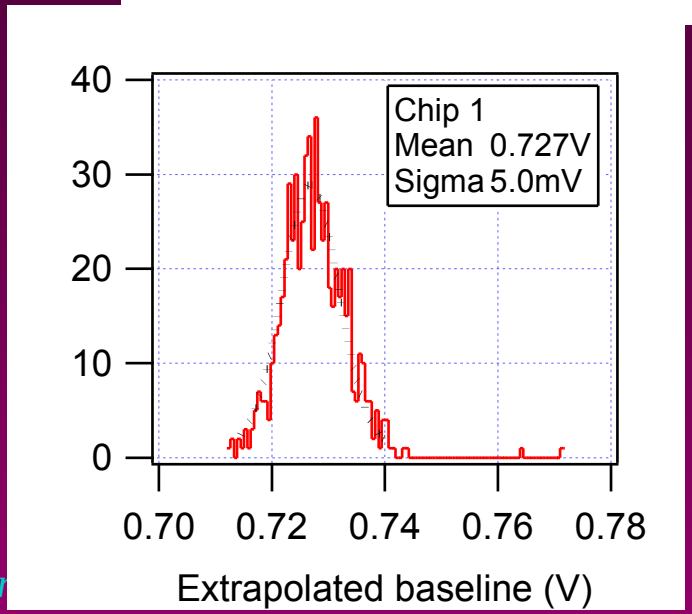
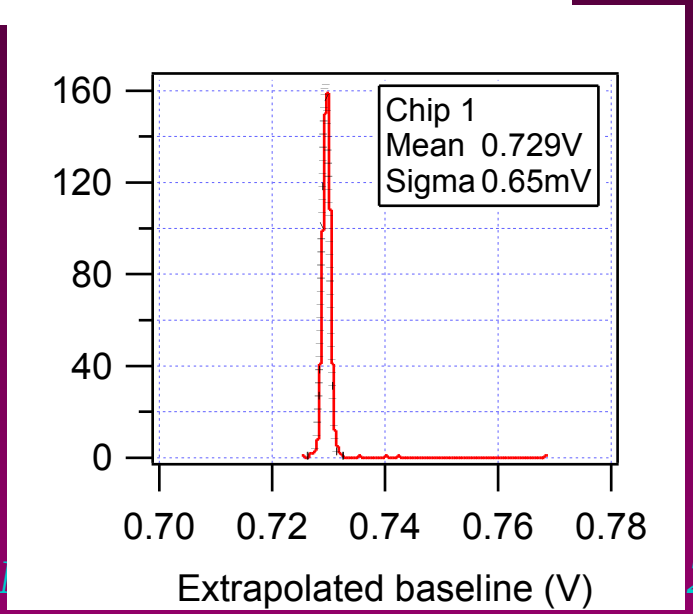
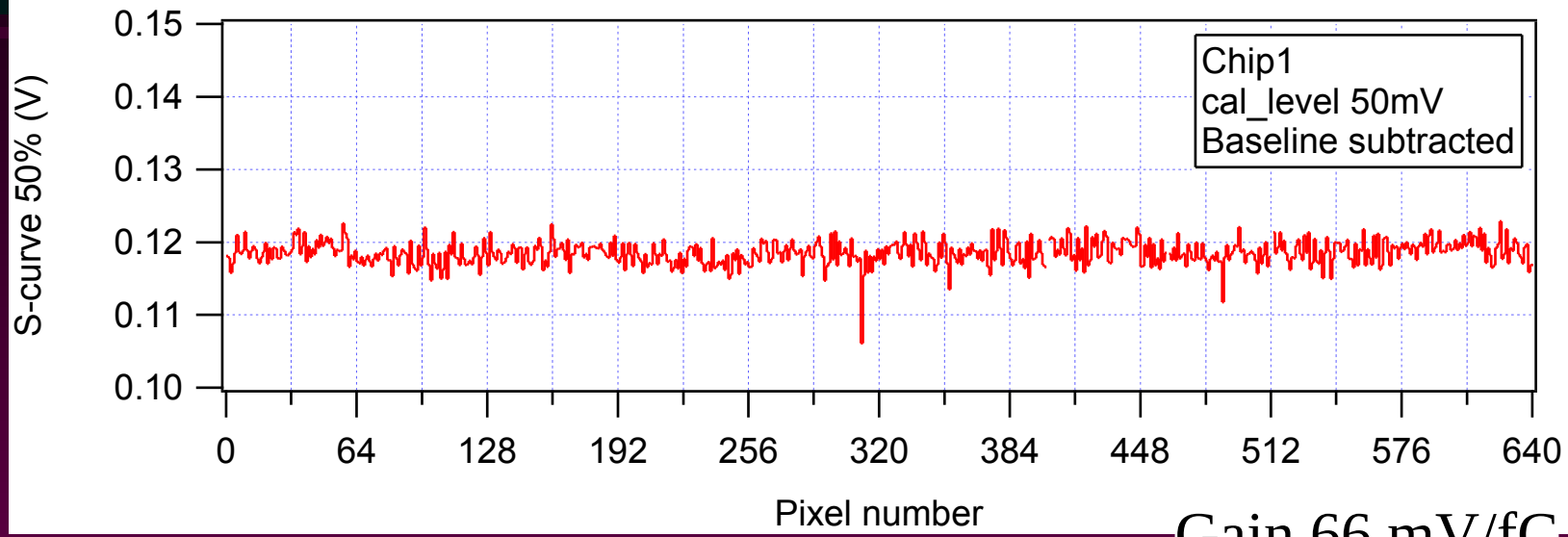




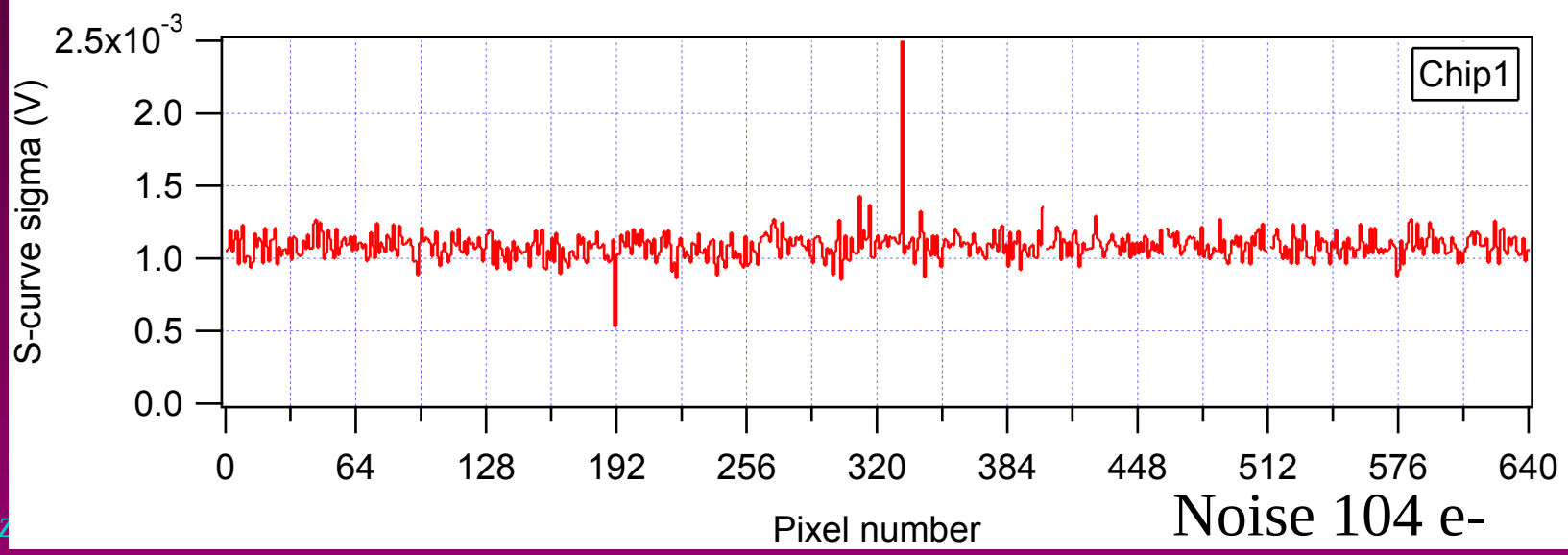
DAC correction



Gain and noise



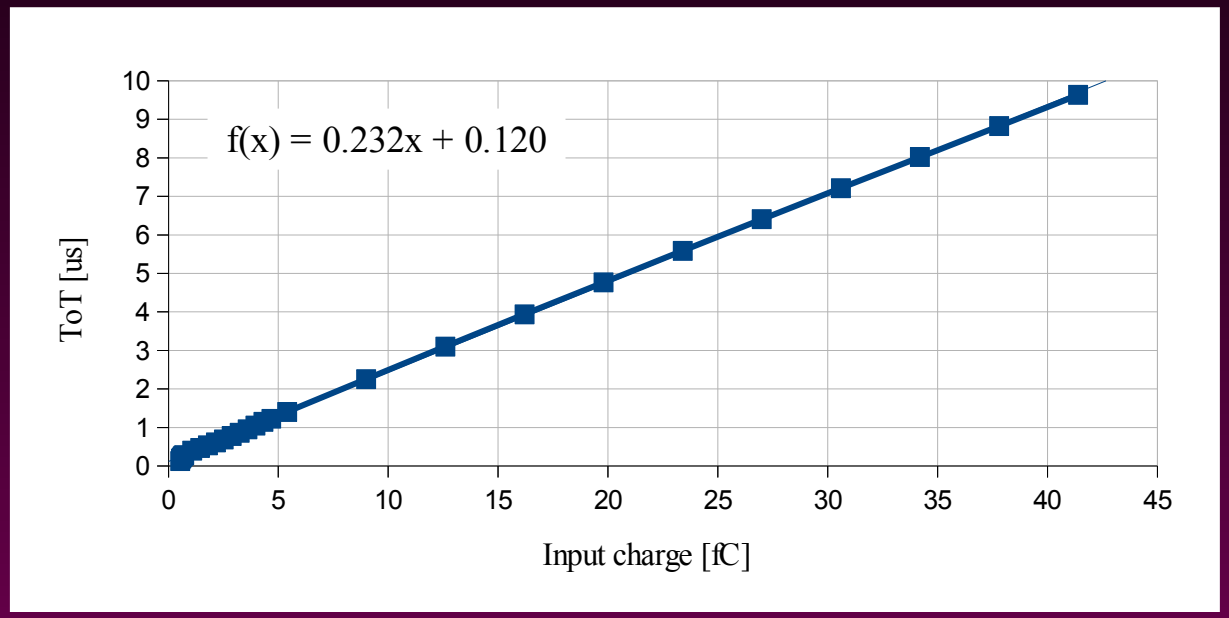
Gain 66 mV/fC

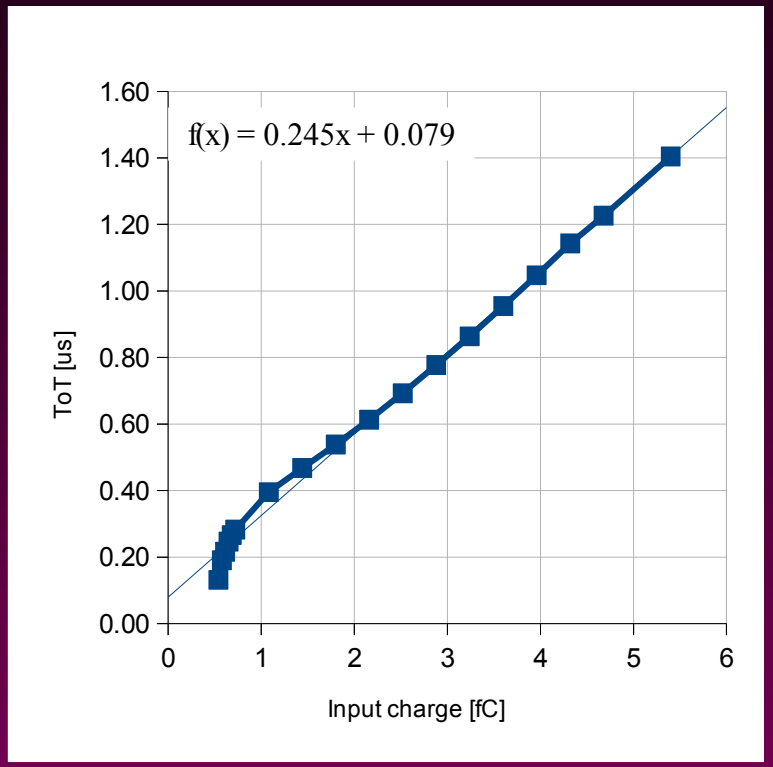


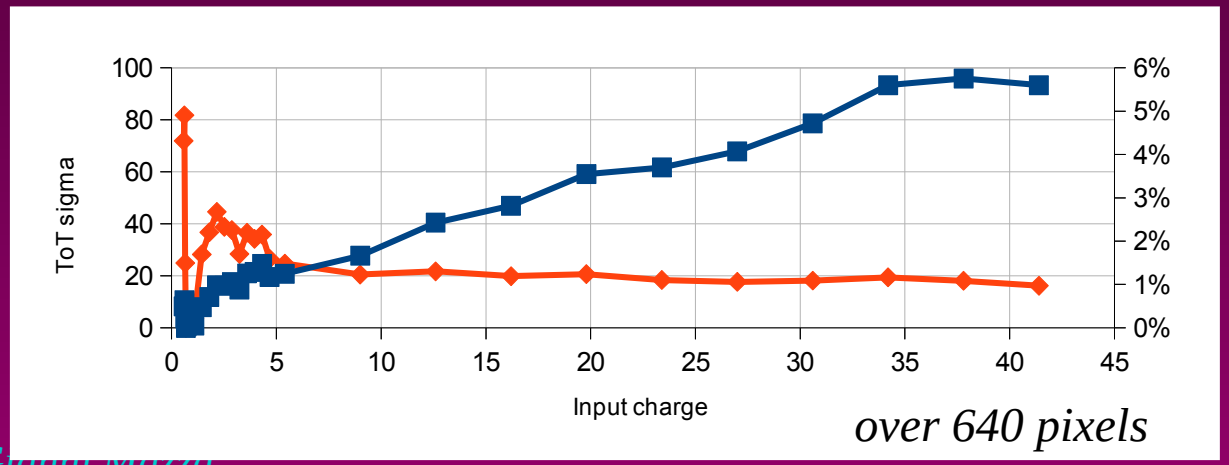
Noise 104 e-

ToT @ 5 nA

Sezione di Torino





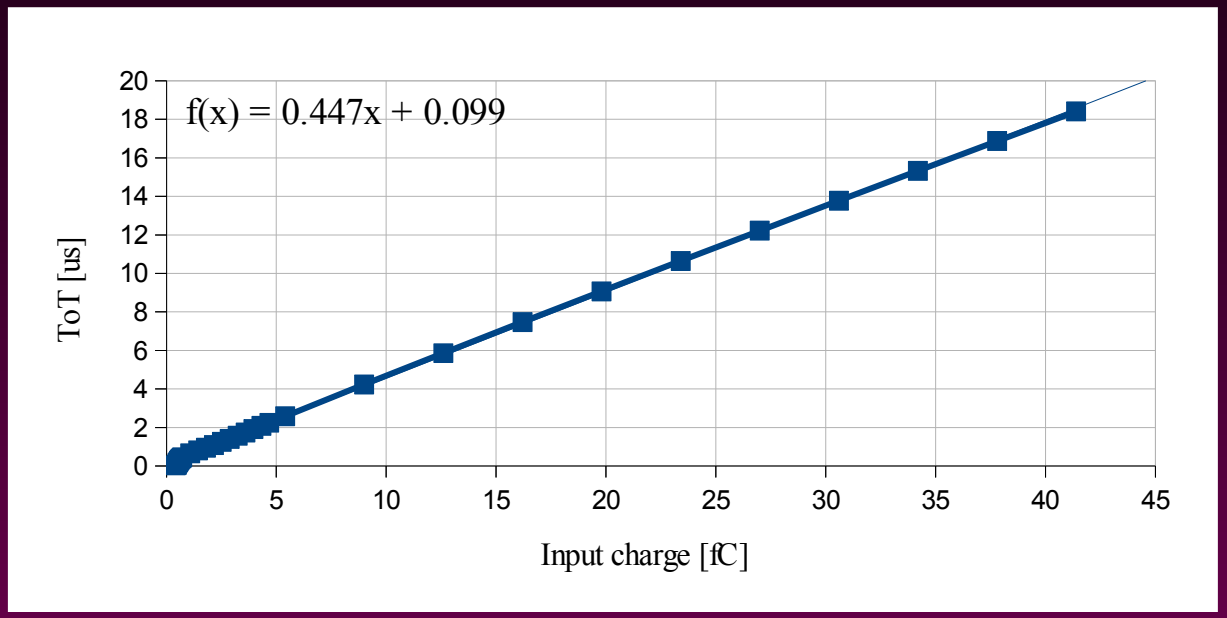


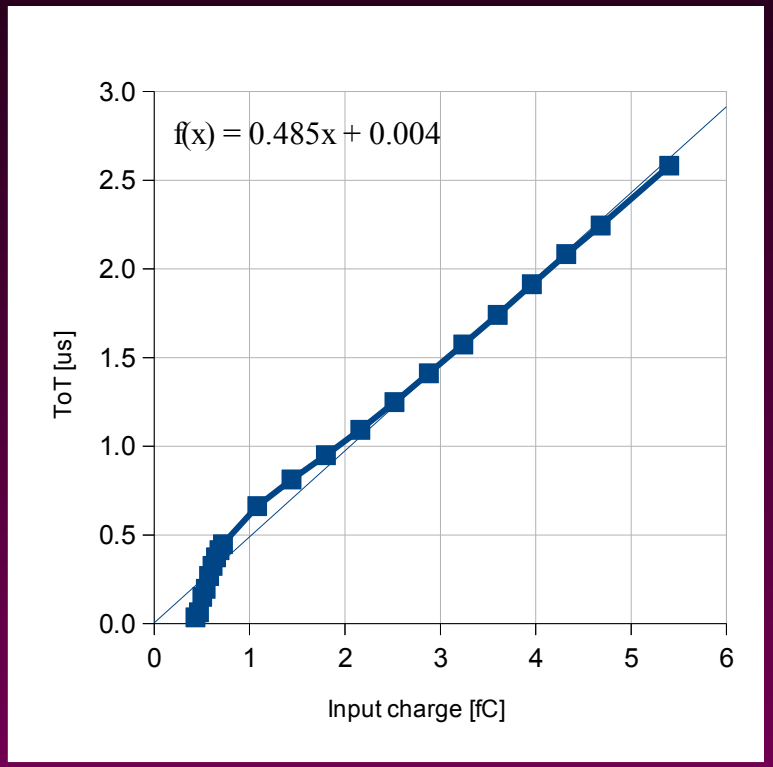
$I_{FB} = 5\ nA$

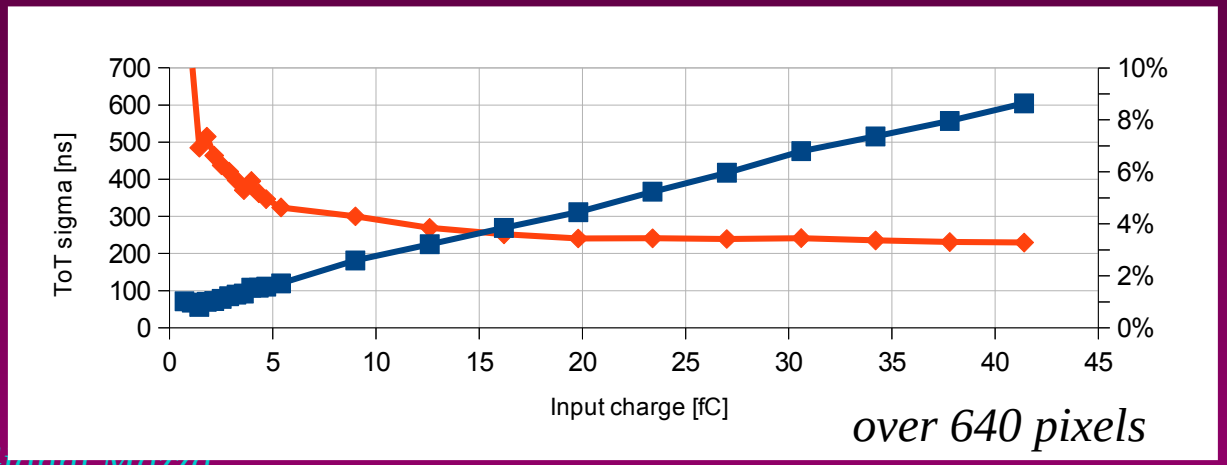
Simulated gain : 202 ns/fC

ToT @ 2.5 nA

Sezione di Torino







$I_{FB} = 2.5\ nA$

Simulated gain : 400 ns/fC

Conclusions

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- The ASIC solution for the triggerless readout of the silicon pixel sensors of the PANDA experiment has been described
- The current reduced-size prototype is fully functional in terms of main performances
- Some issues related to the time resolution to be clarified (trade-off between resolution and power)
- Tests of the prototype bump-bonded to the detector will start in few weeks
- Beam tests and irradiation tests (both TID and SEU) are foreseen for the end of 2011 and beginning of 2012.

Backup slides

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Backup slides

Cable routing

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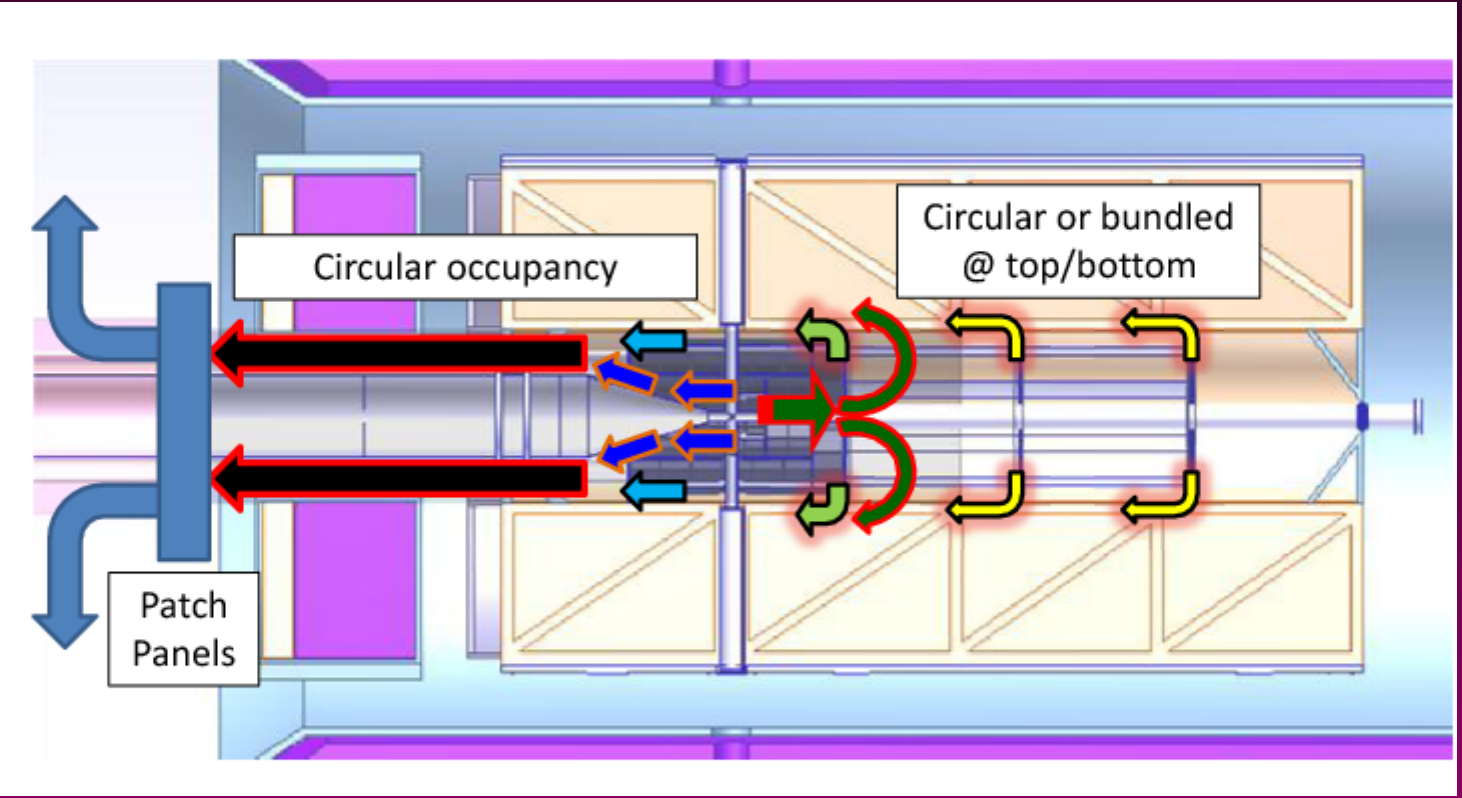
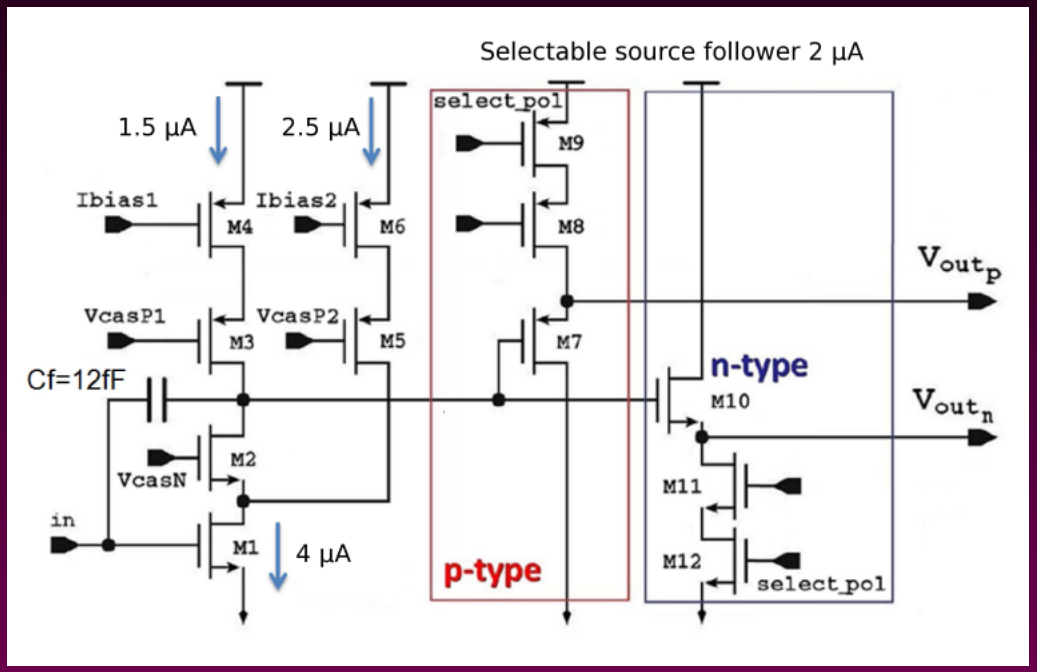
Access possible on the upstream direction
→ possible criticity in cables and service routing



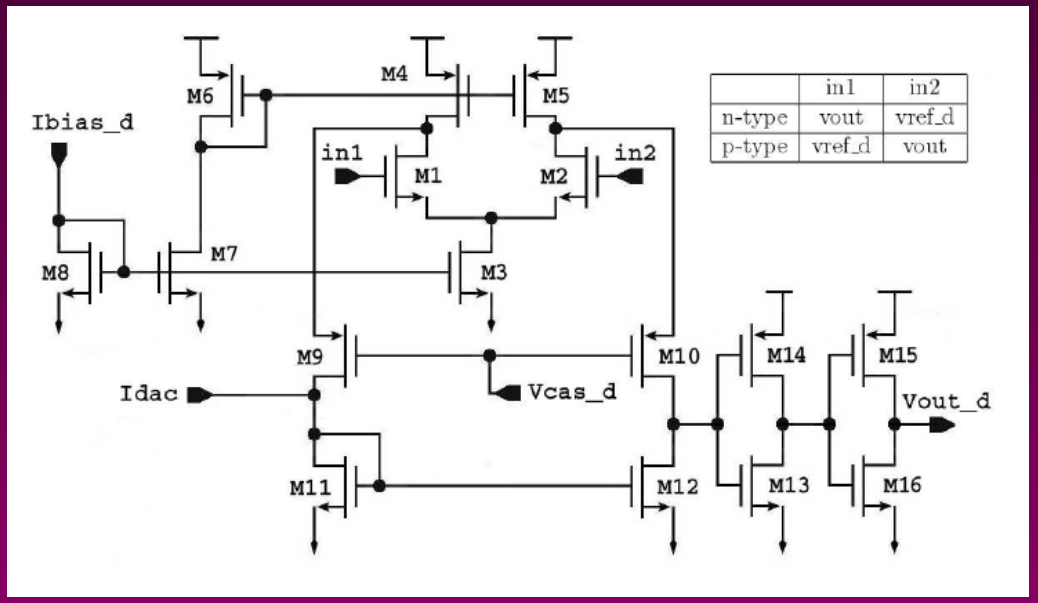
Preamplifier & comparator

Sezione di Torino



Preamplifier

open loop gain	: ~60 dB
f_{-3dB}	: ~ 500 kHz
closed loop gain	: 76 mV/fC



	in1	in2
n-type	vout	vref_d
p-type	vref_d	vout

Comparator

Baseline restorer & feedback current source

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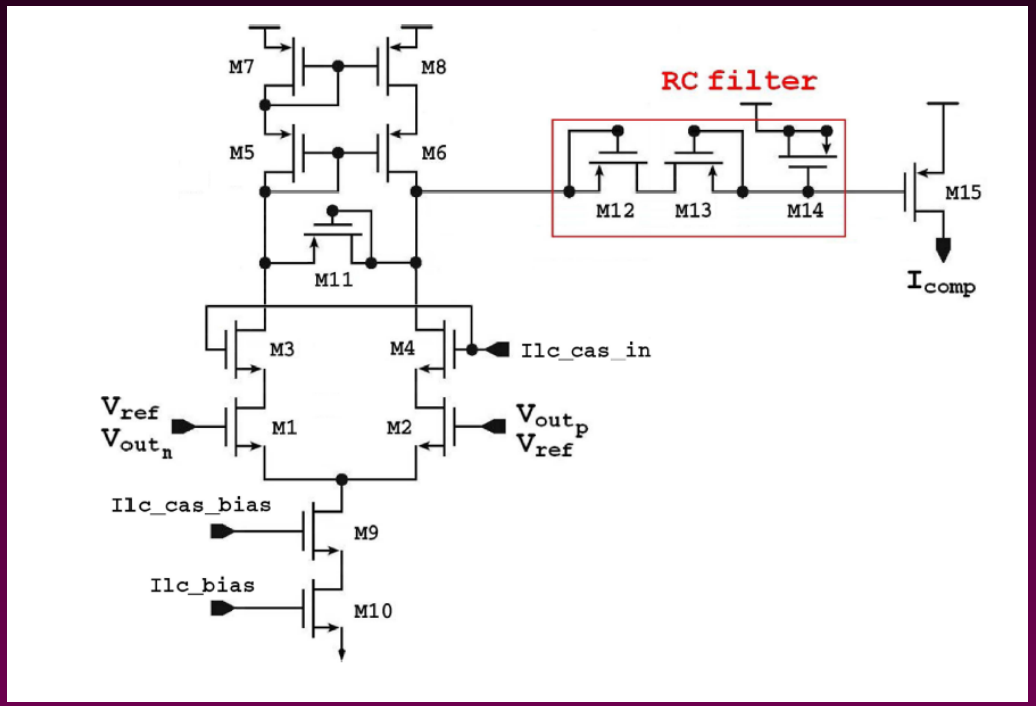
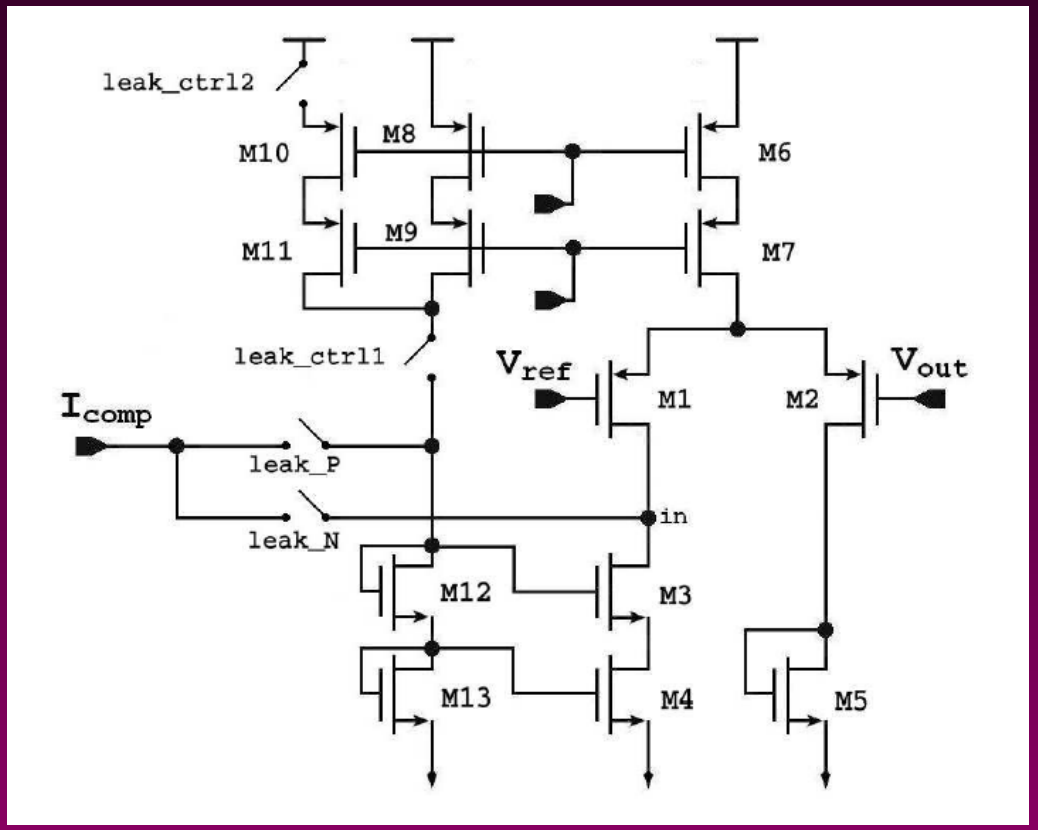


Feedback current source



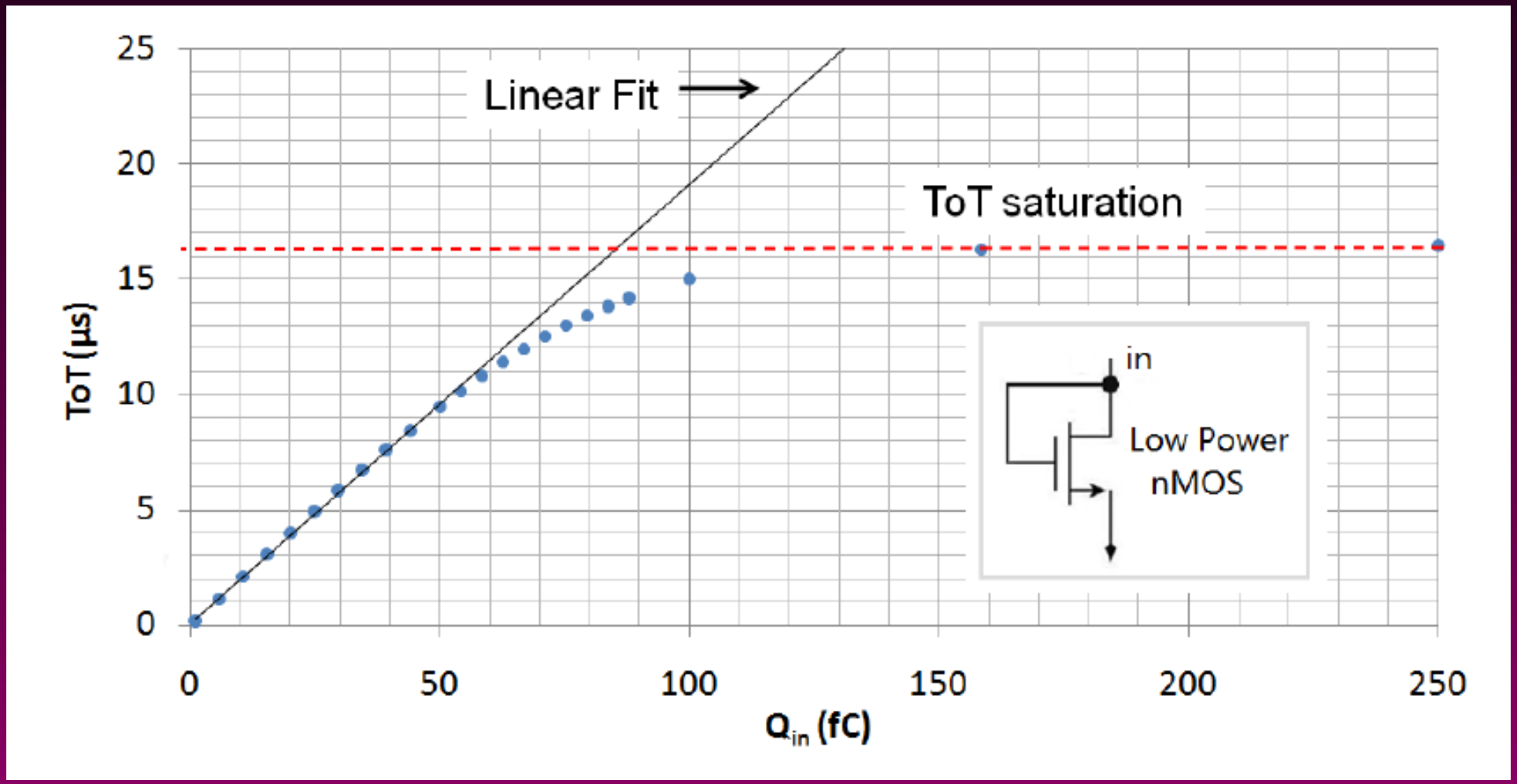
Baseline restorer

R_{EQ} : 500 MΩ÷10 GΩ

C_{EQ} : 5 pF

f_{-3dB} : ~ 500 kHz

Clipping circuit



Irradiation tests - 1

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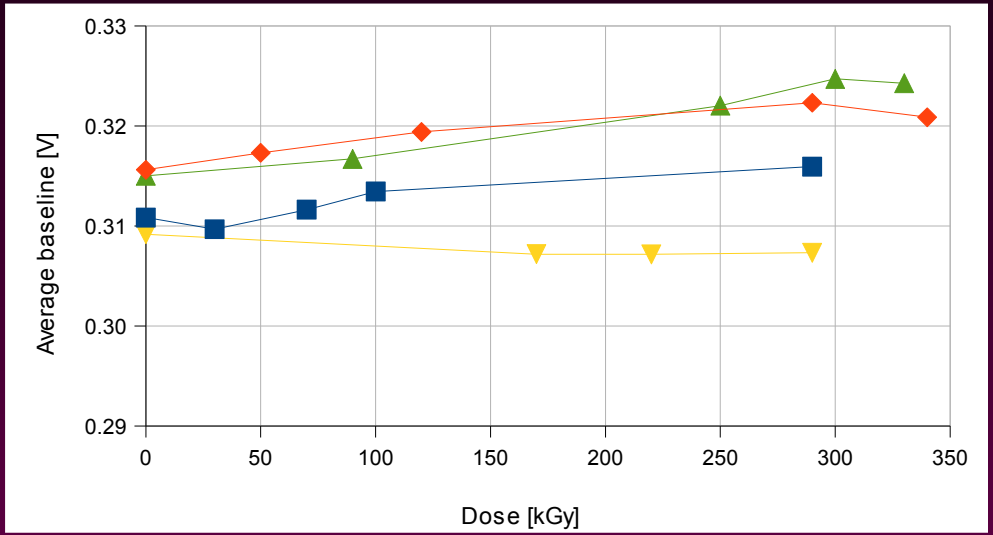
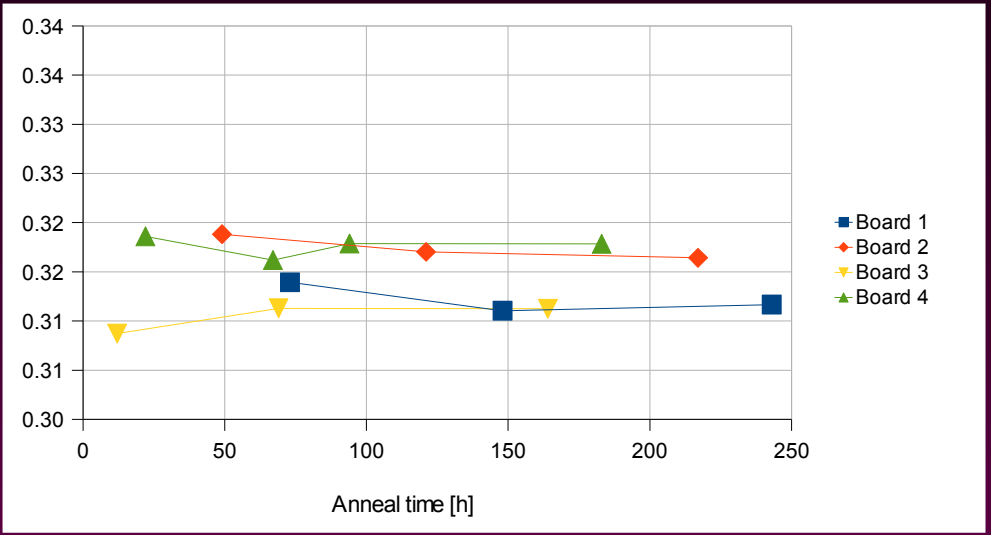
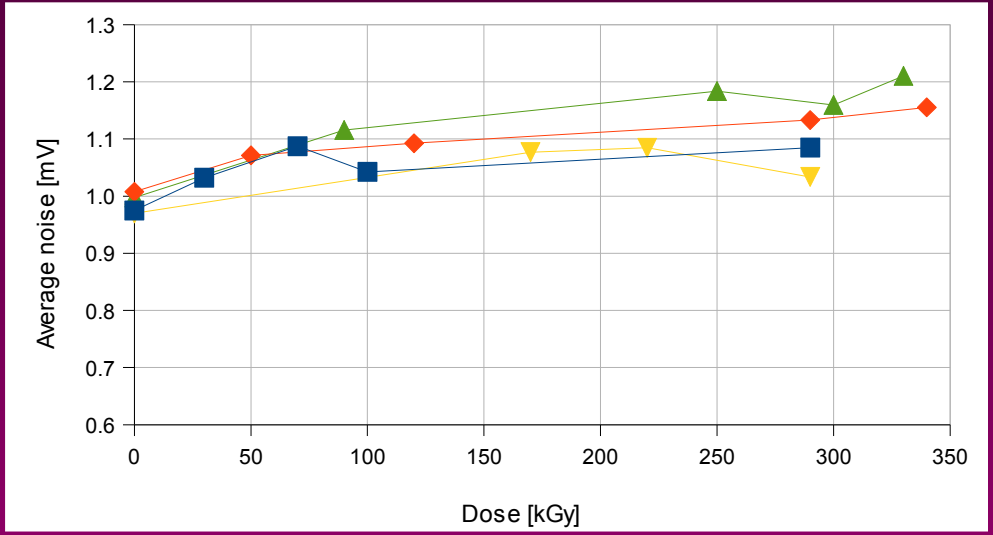
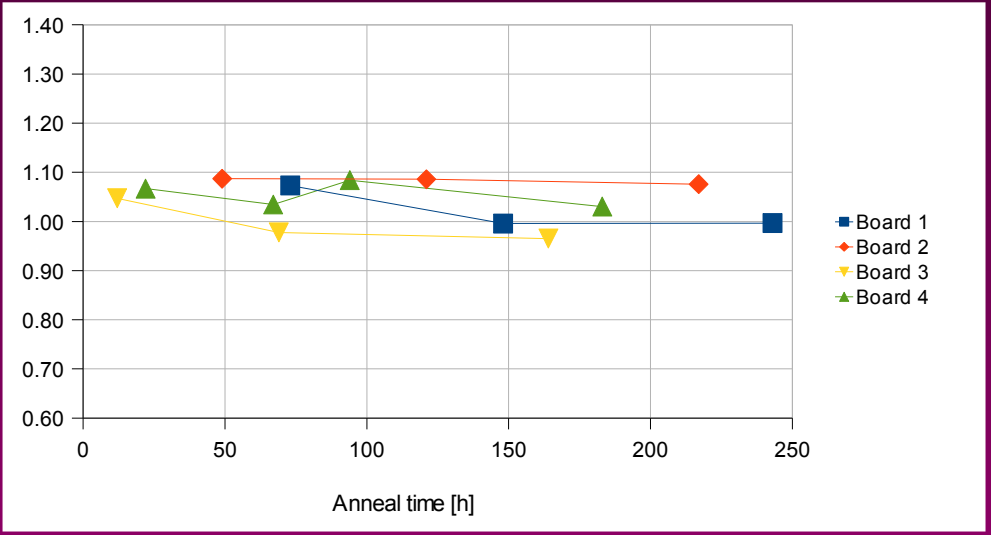


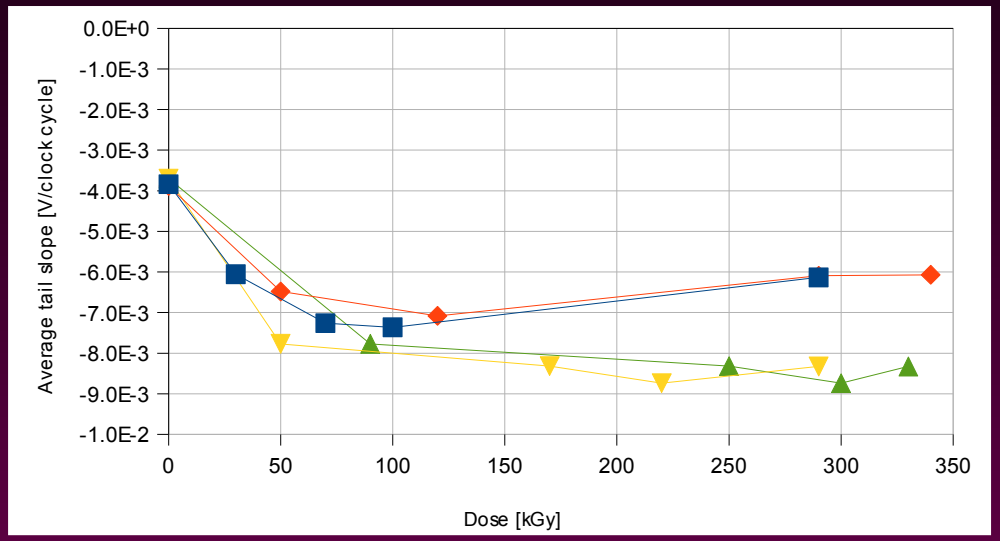


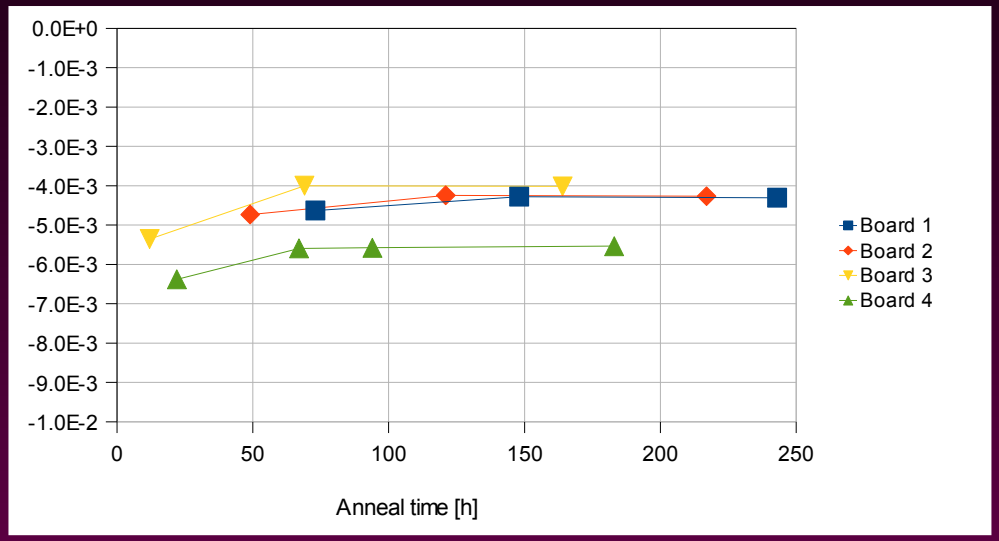


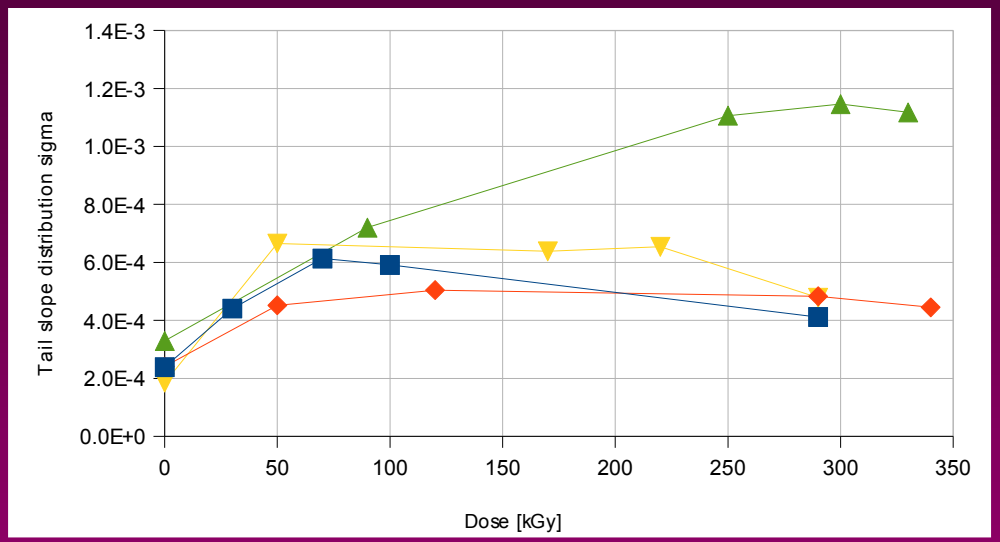


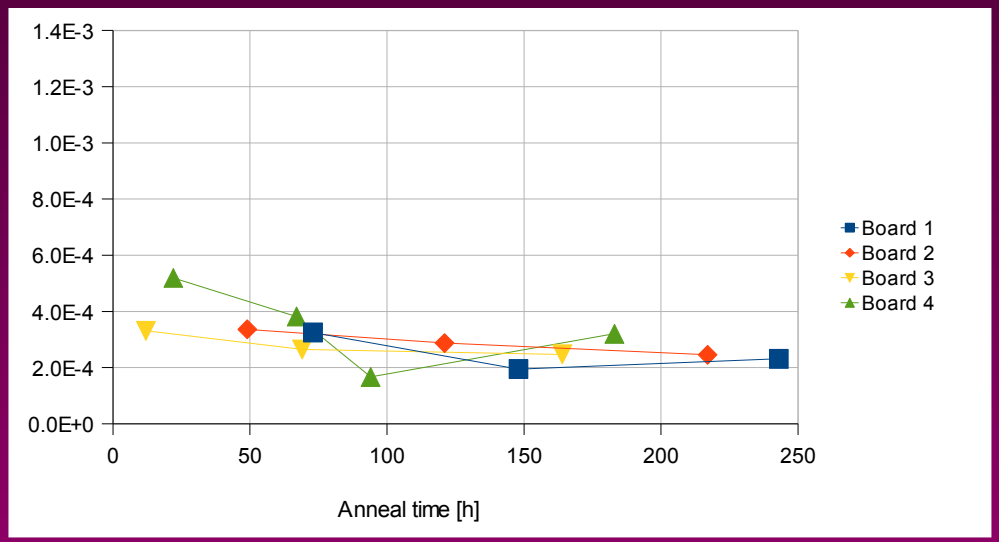
Irradiation tests - 2

Sezione di Torino

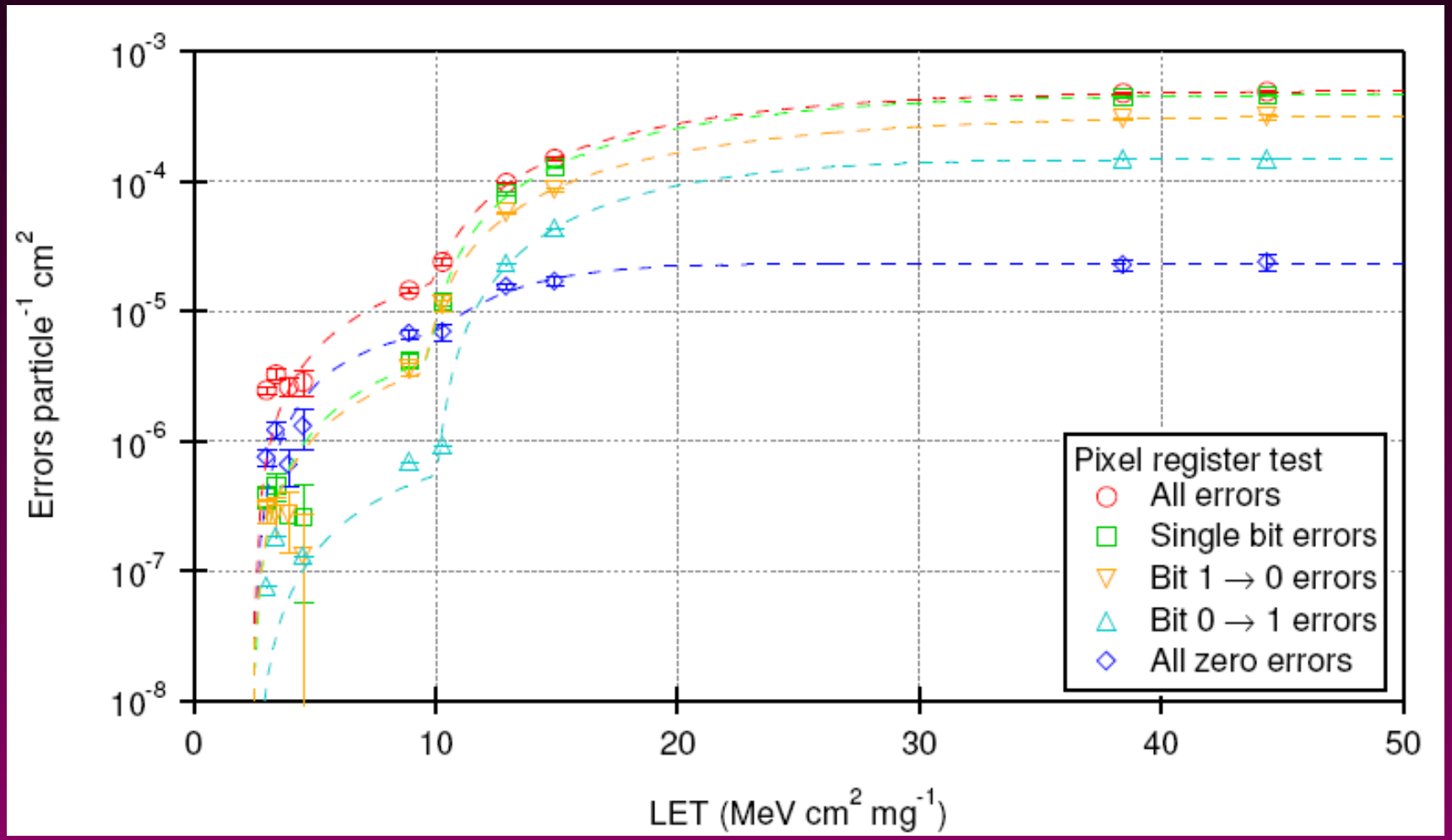








SEU effects


Errors particle^{-1} cm^{2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
0
10
20
30
40
50
LET (MeV cm^{2} mg^{-1})
Pixel register test
All errors
Single bit errors
Bit 1 → 0 errors
Bit 0 → 1 errors
All zero errors