First characterization of the PASTA chip for the microstrip part of the $\bar{P}$ANDA MVD

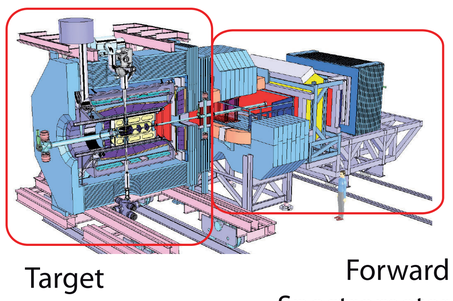
Tommaso Quagli[1], Kai-Thomas Brinkmann[1], Daniela Calvo[2], Valentino Di Pietro[1], Alessandra Lai[3], Alberto Riccardi[1], James Ritman[3], Angelo Rivetti[2], Manuel Rolo[2], Robert Schnell[1], Tobias Stockmanns[3], Richard Wheadon[2], André Zambanini[3], and Hans-Georg Zaunick[1]

[1]II. Physikalisches Institut, Justus-Liebig-Universität Gießen; [2]INFN, Sezione di Torino; [3]Forschungszentrum Jülich GmbH, Jülich, Germany

DPG Frühjahrstagung 2017, Münster

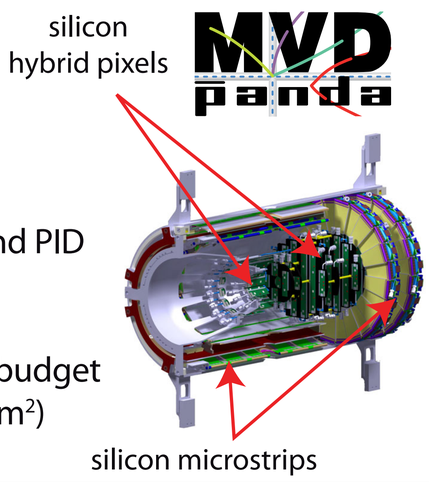
The $\bar{P}$ANDA Experiment

- Fixed target experiment
- Almost 4π acceptance
- Cooled antiproton beam using electron and stochastic cooling
- Proton or heavy nuclear target
- Momentum from 1.5 up to 15 GeV/c
- Trigger-less readout at ~10^7 interactions / s



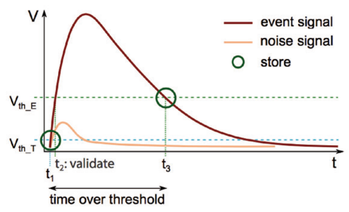
The Micro-Vertex-Detector

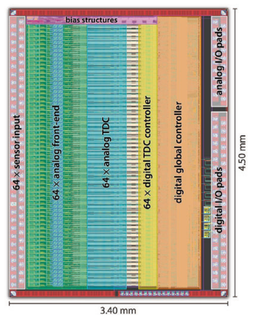
- 4 concentric barrels and 6 forward disks
- Vertex reconstruction for primary and secondary vertices
- Improvement of momentum resolution and PID
- Requirements:
  - spatial resolution (tens of µm)
  - good time resolution and low material budget
  - high radiation tolerance (10^{14} $n_{1MeV\,eq}$ / cm^2)



PANDA STrip ASIC (PASTA)

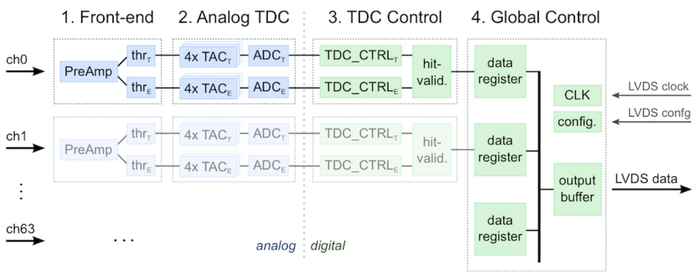
- Front-end readout chip for double-sided silicon strip sensors
- Measurement concept inspired by TOFPET



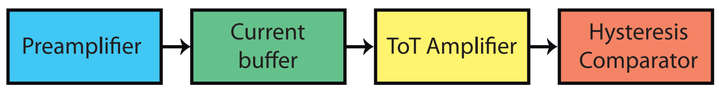


- Number of channels: 64
- Input pitch: 63 µm
- Clock frequency: 160 MHz
- Rate capability: 100 kHz / ch
- Time bin width: 50 - 400 ps
- dE/dx measurement: ToT, 8 bits dynamic range
- Front-end noise: < 600 e^-
- Power consumption: < 4 mW / ch
- Radiation tolerance: 100 kGy (TID)
- Technology: CMOS 110 nm

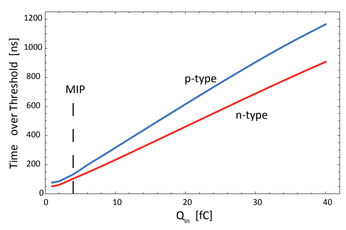
Chip Architecture



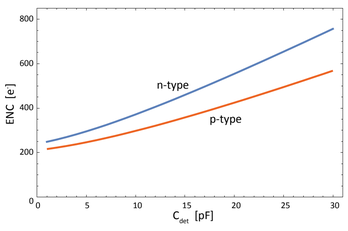
Front-End Architecture



Chip Simulations



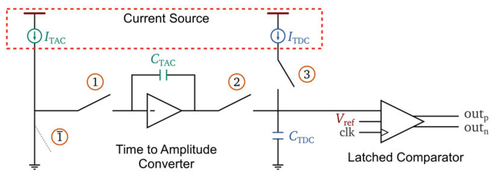
ToT linearity in the input charge range from 1 fC to 40 fC



Electronic noise with an input charge of 4 fC, for a capacitance from 1 pF to 30 pF

Analog TDC

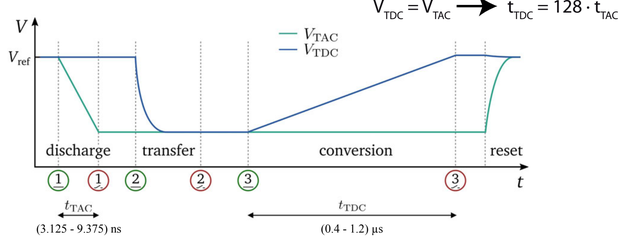
Time-to-Digital Converter (TDC) architecture



TDC working principle

$C_{TDC} = 4 \cdot C_{TAC}$; $I_{TDC} = 1/32\, I_{TAC}$

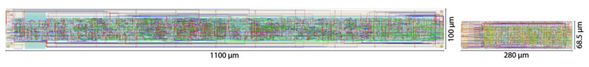
$V_{TDC} = V_{TAC} \rightarrow t_{TDC} = 128 \cdot t_{TAC}$



Digital Blocks

Significant optimization of TDC control with respect to TOFPET:

- Size reduced by ~80%
- Overall power consumption halved

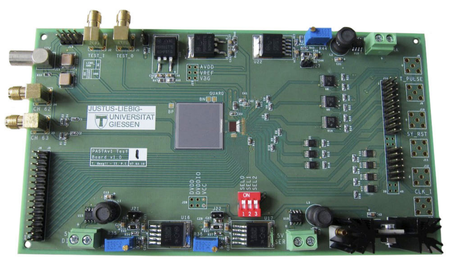


Radiation-hard logic for Single Event Upset (SEU) protection:

- 1 bit: Triple Modular Redundancy
- n bits: Hamming encoding

PASTA Readout Systems

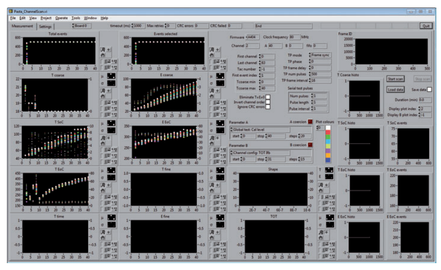
- PASTA chips fabricated in UMC CMOS 110nm technology and assembled on dedicated test boards



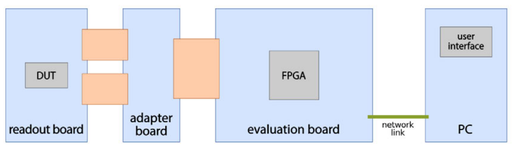
PASTA chip assembled on a test board and connected to a 2x2 cm^2 silicon strip sensor (strip pitch 50 µm)

Two readout systems:

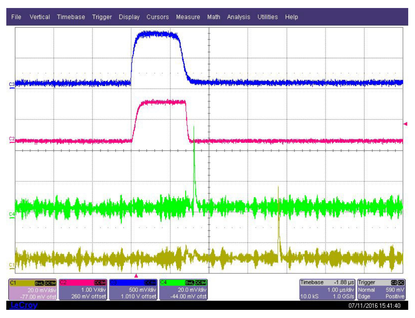
- Labview-based Torino system
  - Optimized for parameter scans and chip testing
  - Acquisition of signal from a radioactive source



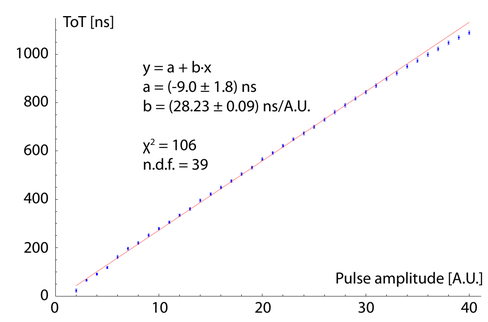
- Jülich Digital Readout System (JDRS)
  - Modular, flexible system
  - Higher rate capability suitable for use during beam tests
  - See A. Lai et al., HK 63.8



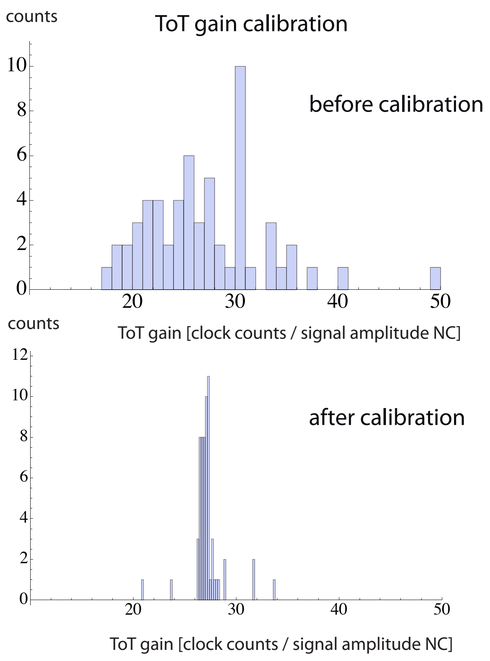
First PASTA Characterizations



Example of chip test signals for an injected pulse

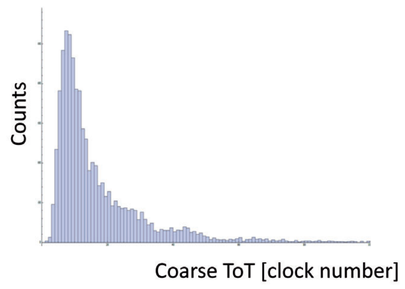


ToT linearity with ToT = t_{coarse_E} - t_{coarse_T}



First characterizations of the ASIC:

- measurement of the ToT linearity (using only the coarse timing information);
- acquisition of signal from alpha an beta radioactive sources on the strip sensor;
- calibration of the ToT gain on all channels on a chip by adjusting the ToT feedback current.



Spectrum of a ^{90}Sr β^- source

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN
JÜLICH FORSCHUNGSZENTRUM
INFN
GEFÖRDERT VOM Bundesministerium für Bildung und Forschung
HIC for FAIR Helmholtz International Center

Tommaso Quagli
II. Physikalisches Institut, JLU
Heinrich-Buff-Ring 16
D-35392 Gießen
Tommaso.Quagli@exp2.physik.uni-giessen.de