JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

The PASTA chip for the silicon micro strip sensor of the PANDA **MVD**

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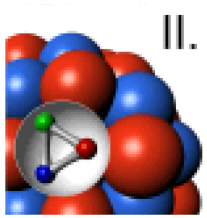
3) INFN Sezione di Torino



II. Physikalisches Institut

DPG Spring Meeting 2016

Contents

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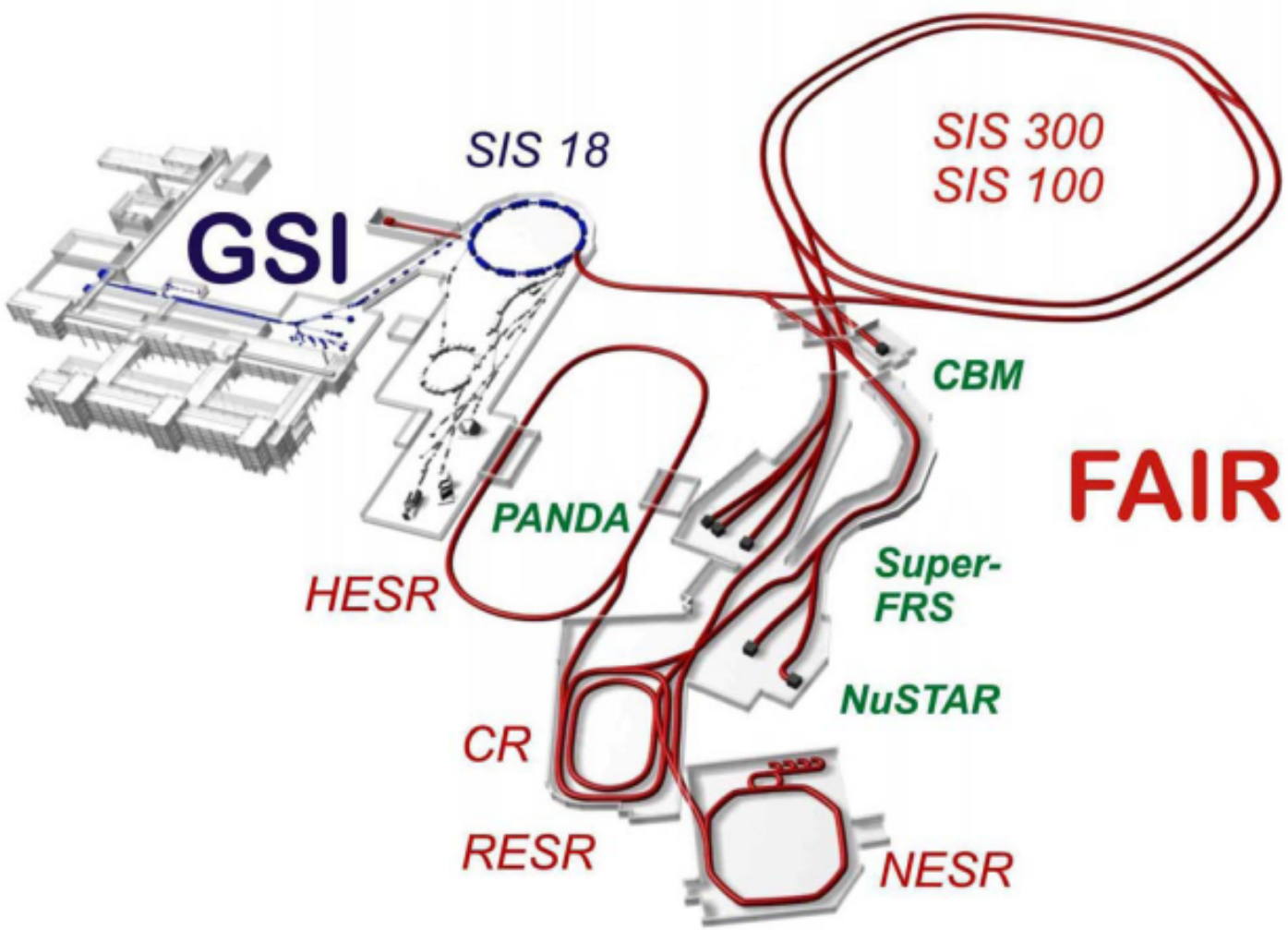
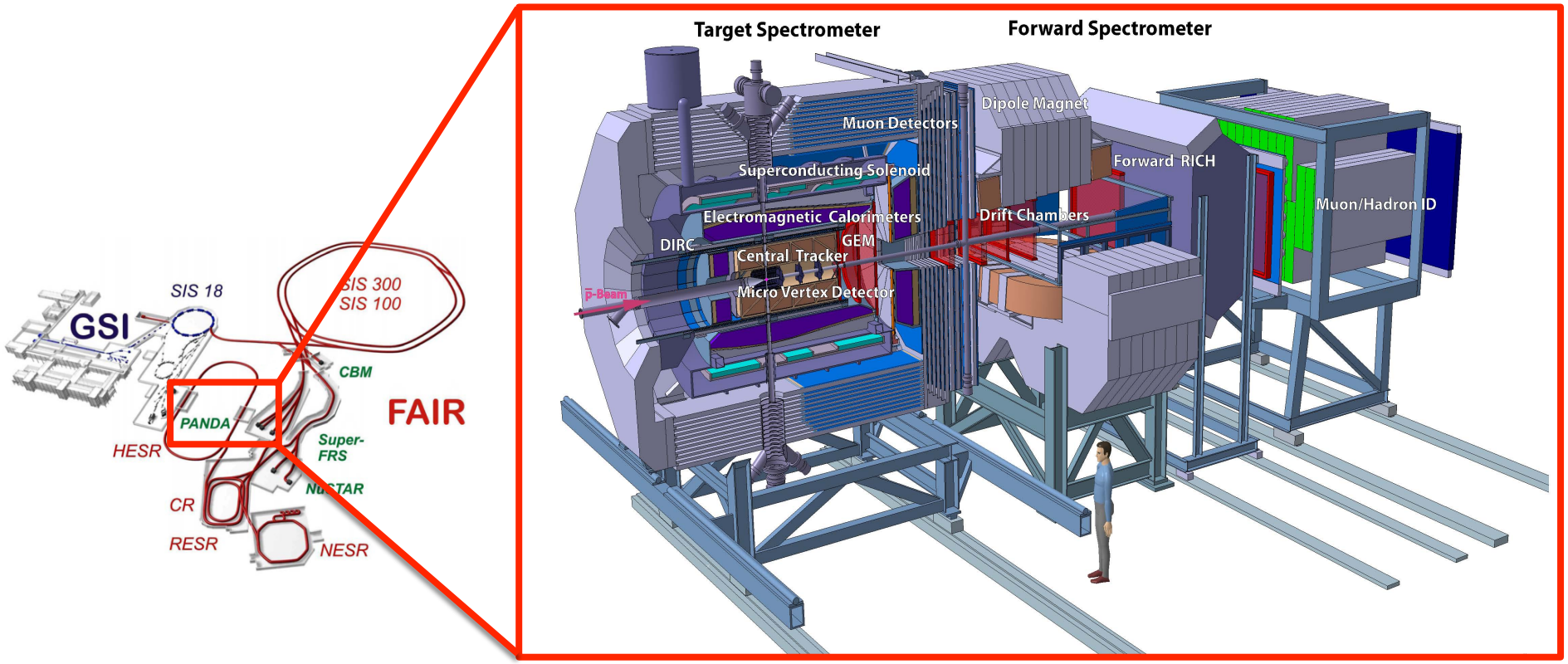

SIS 18
SIS 300
SIS 100
GSI
CBM
FAIR
PANDA
HESR
Super-
FRS
NuSTAR
CR
RESR
NESR

PANDA


GSI
SIS 18
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FAIR
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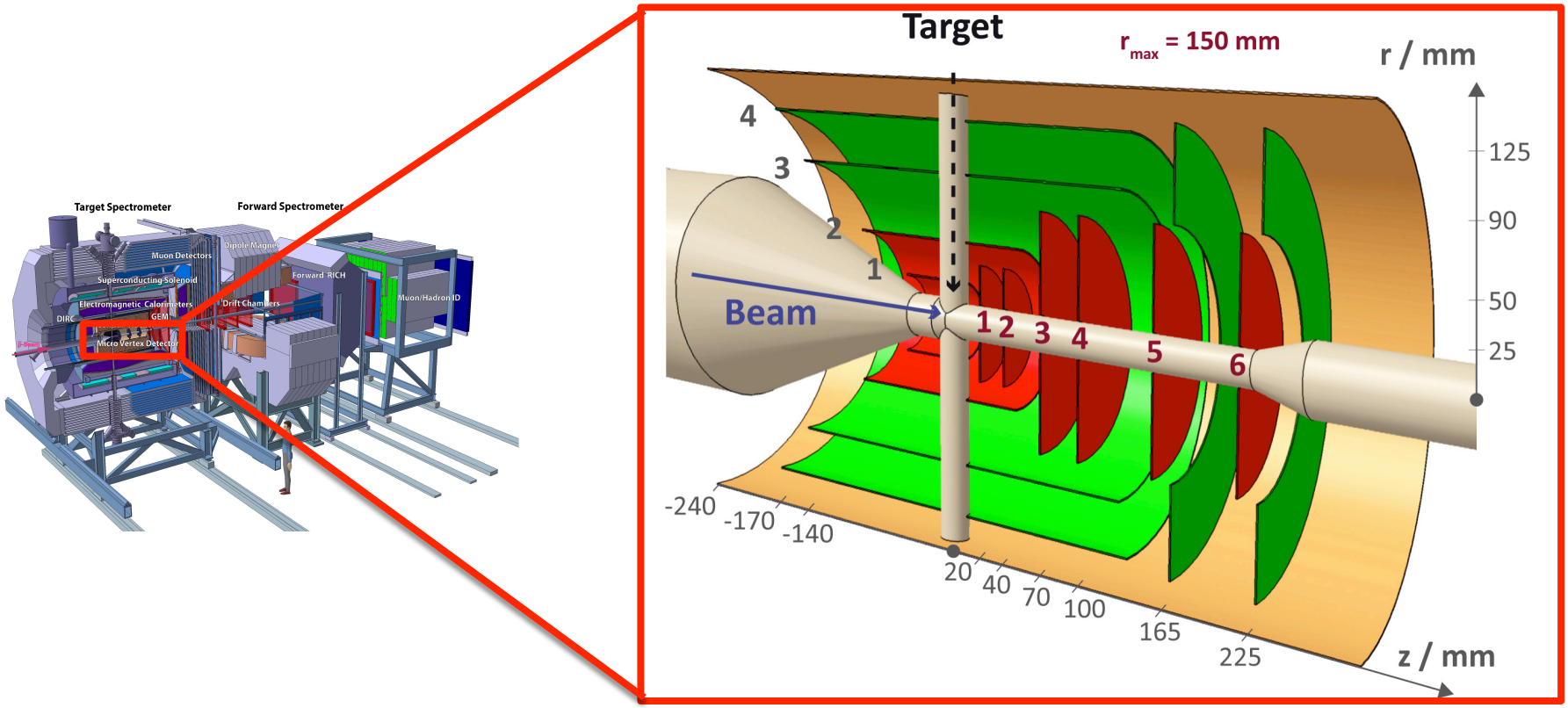
Super-
FRS
HESR
CR
RESR
NESR
Target Spectrometer
Forward Spectrometer
Muon Detectors
Dipole Magnet
Superconducting Solenoid
Forward RICH
Electromagnetic Calorimeters
Drift Chambers
Muon/Hadron ID
DIRC
GEM
Central Tracker
Micro Vertex Detector
p̄-Beam

MicroVertex Detector



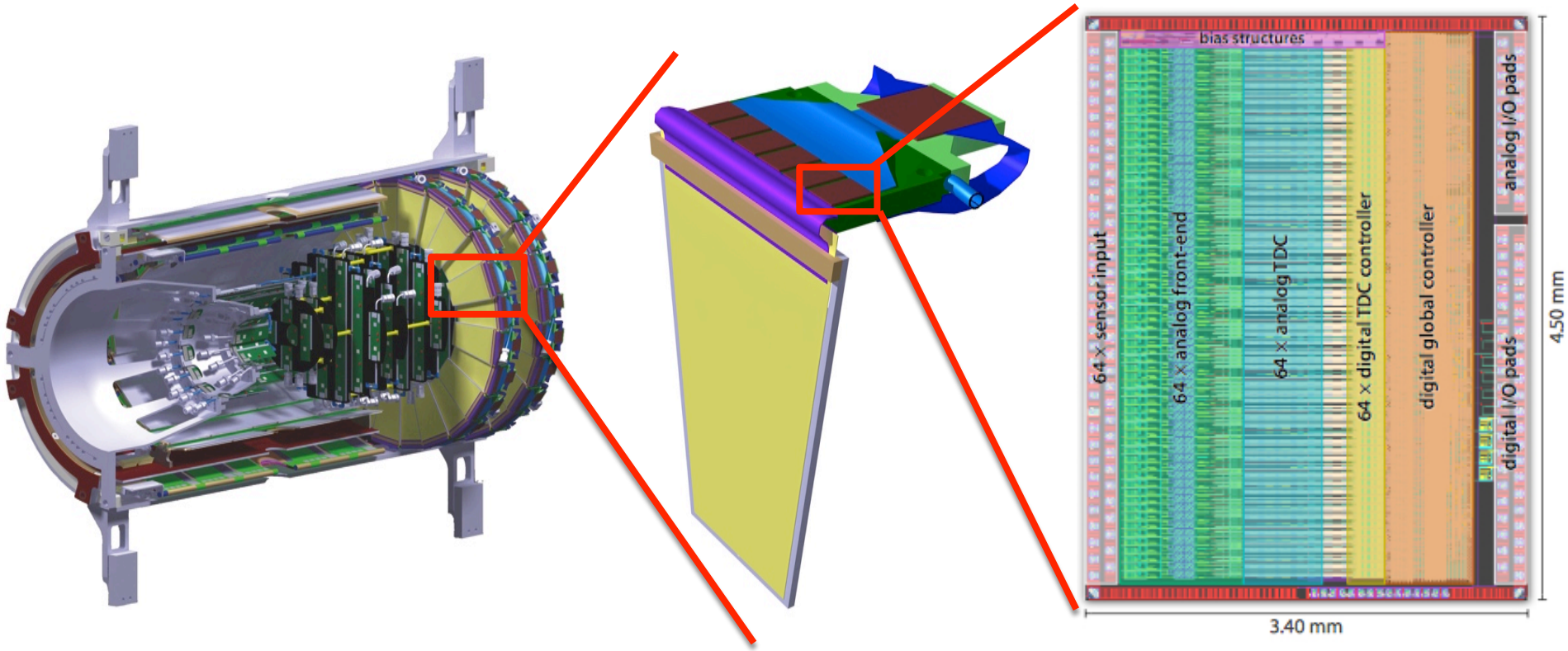
Red zone covered by pixels and green one by strips

PAnda STrip Asic (PASTA)

Micro Vertex Detector

Sensor Module

Readout ASIC

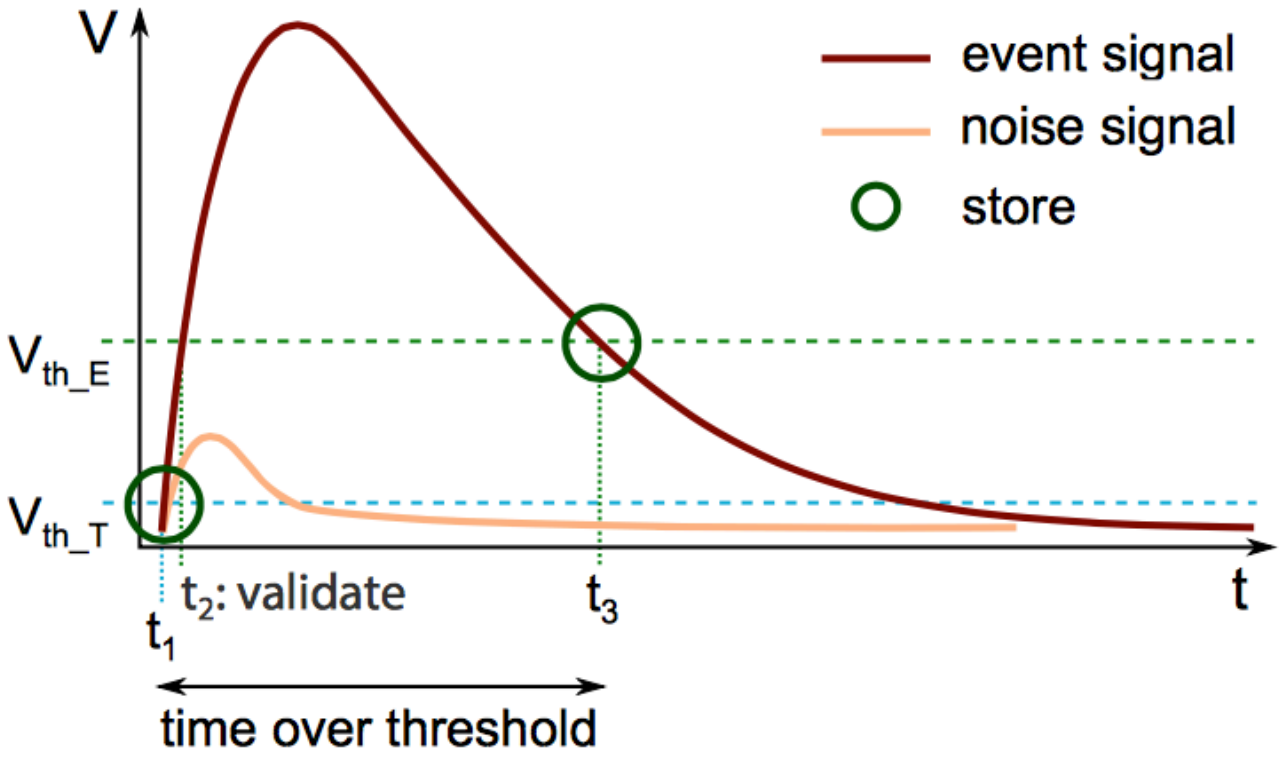


PASTA Features

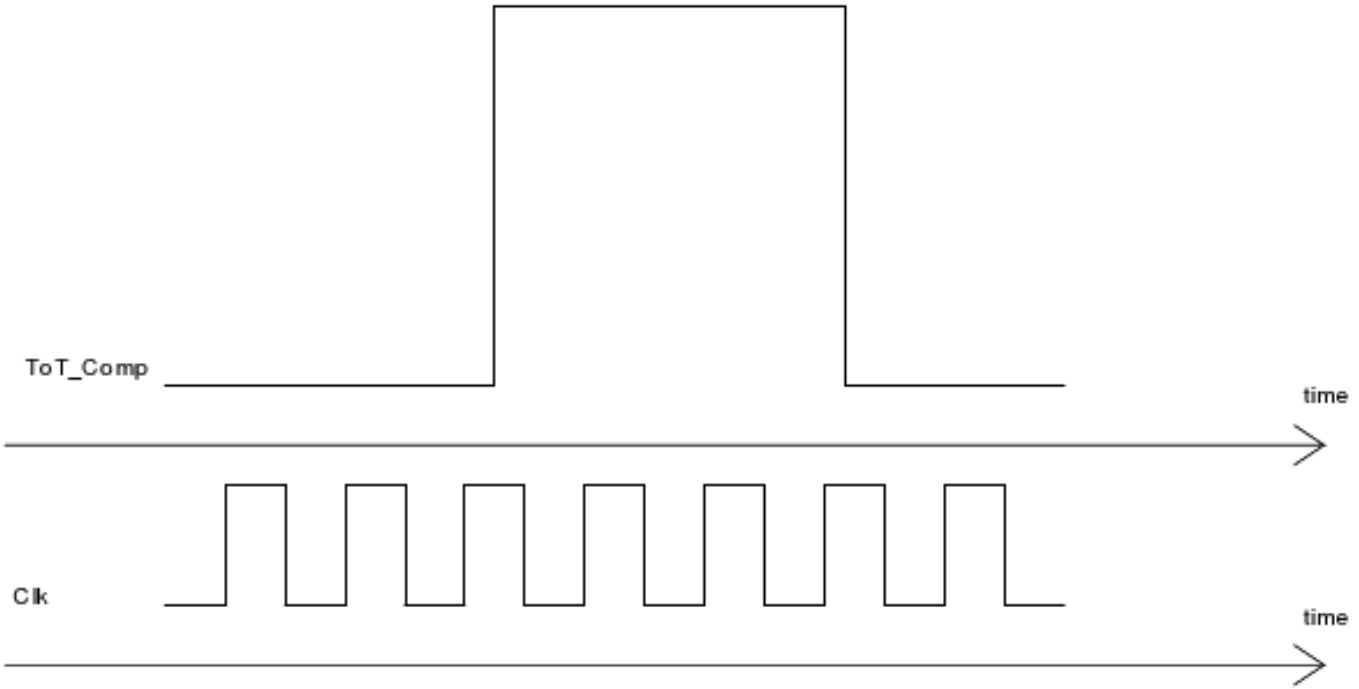
- 64 Channels
- 63 μm input pitch
- 100 kHz Rate/channel
- Less then 4 mW per channel
- Triggerless
- Radiation tolerance 100 kGy

Measurement Concept

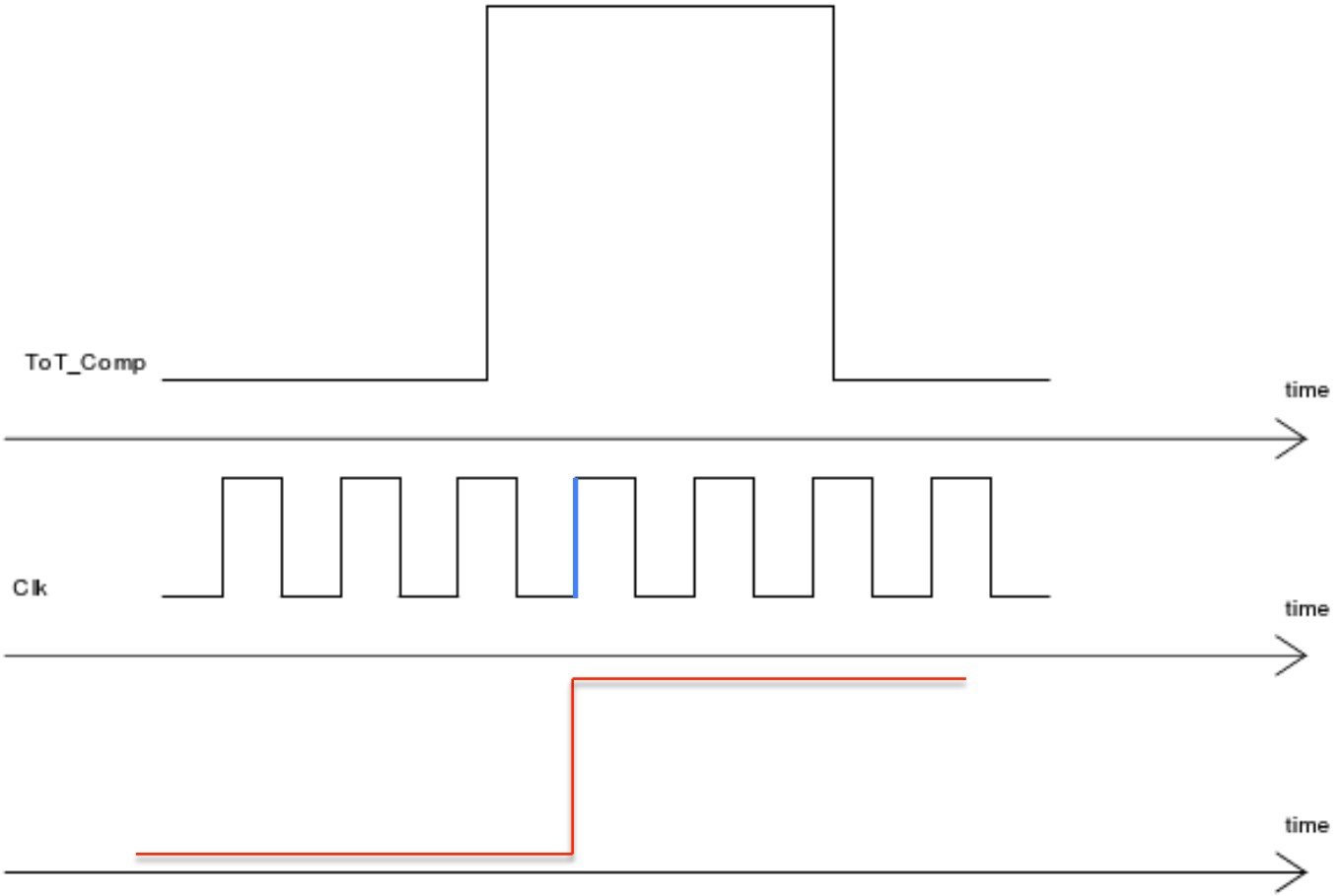
- Low threshold: better time stamp resolution
- High threshold: better jitter performance



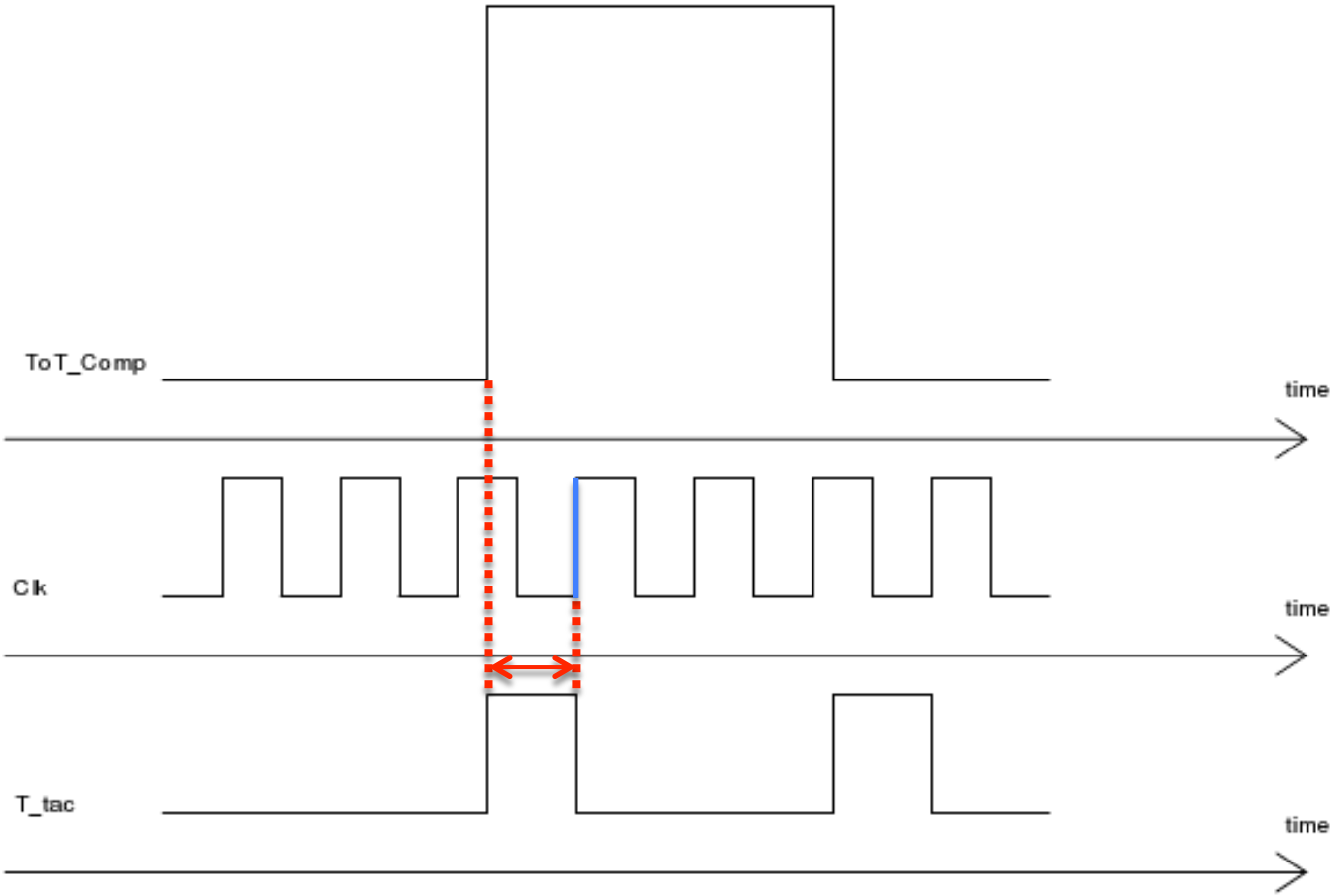
Timing



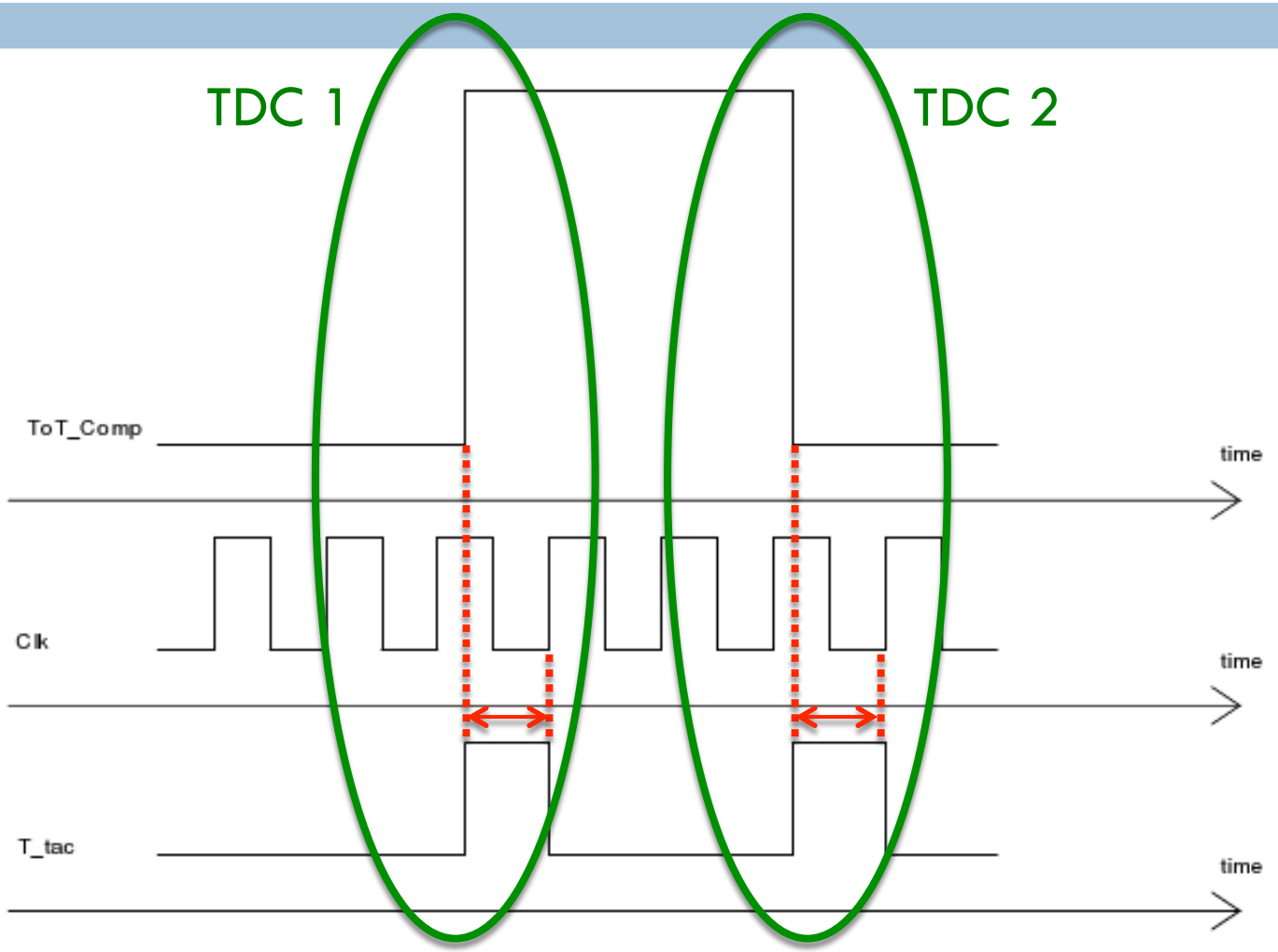
Timing



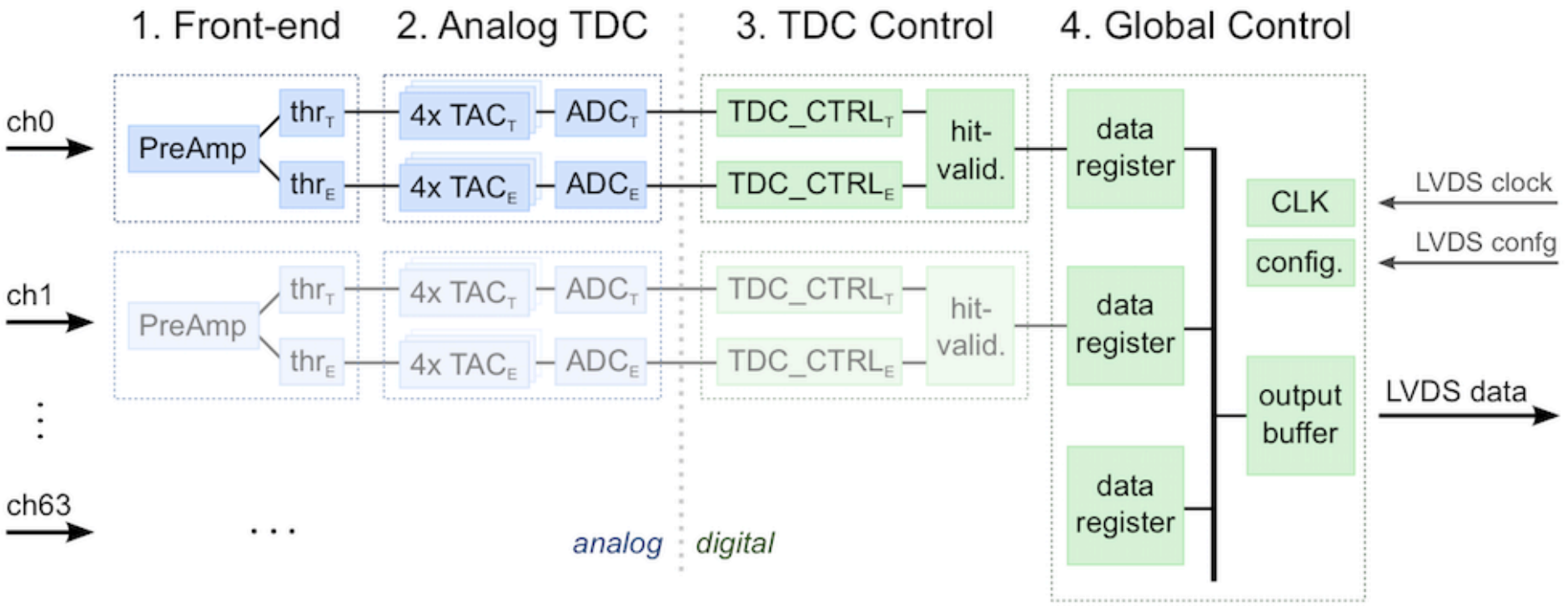
Timing



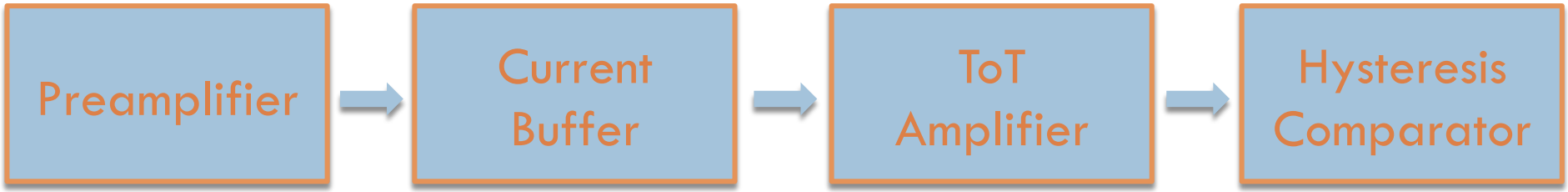
Timing



PASTA Architecture

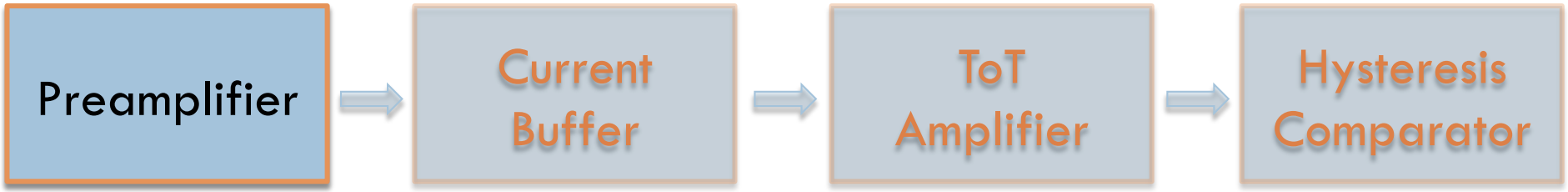


Front-End Implementation



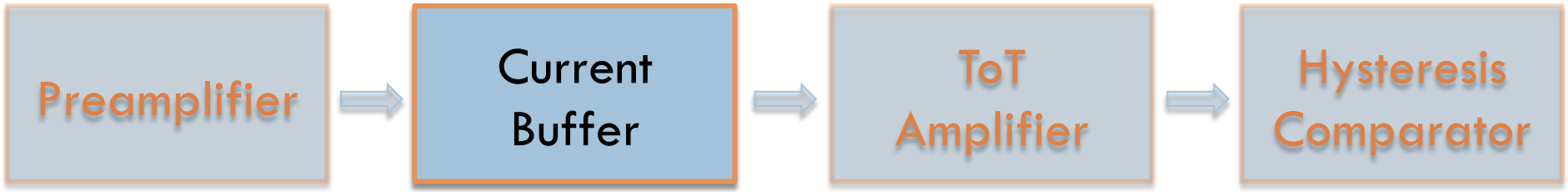
Front-End Implementation

- First preamplification
- Two input polarities, same output polarity



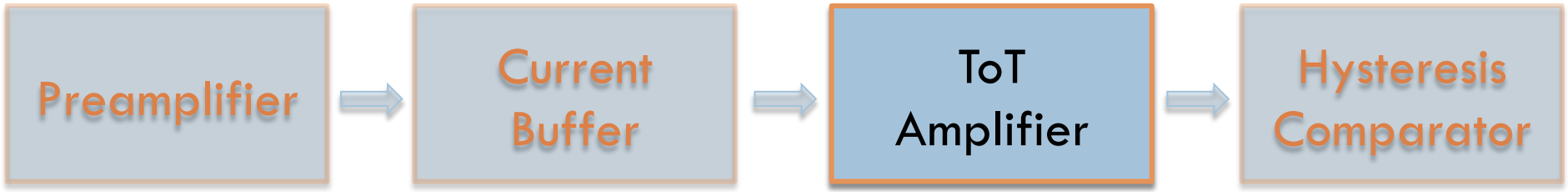
Front-End Implementation

- Current amplification
- Impedance adapter



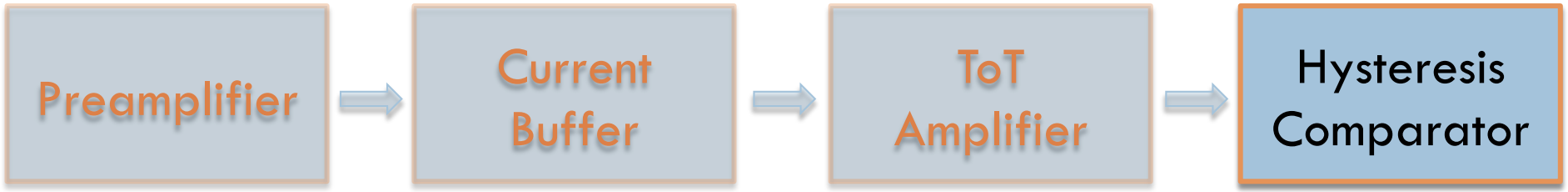
Front-End Implementation

- Last amplification
- Constant current discharge of feedback capacitance

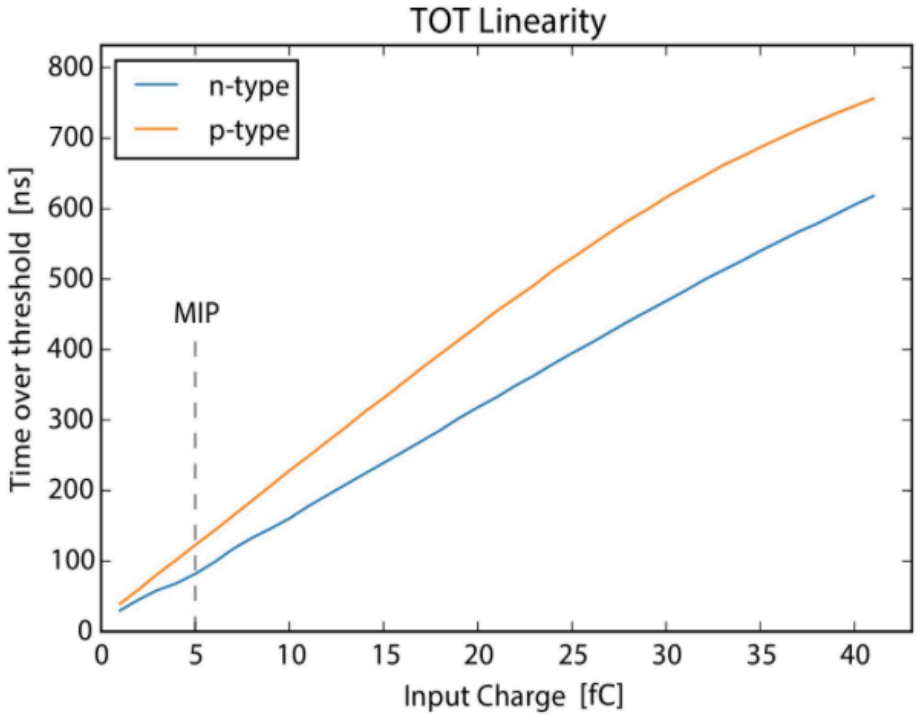


Front-End Implementation

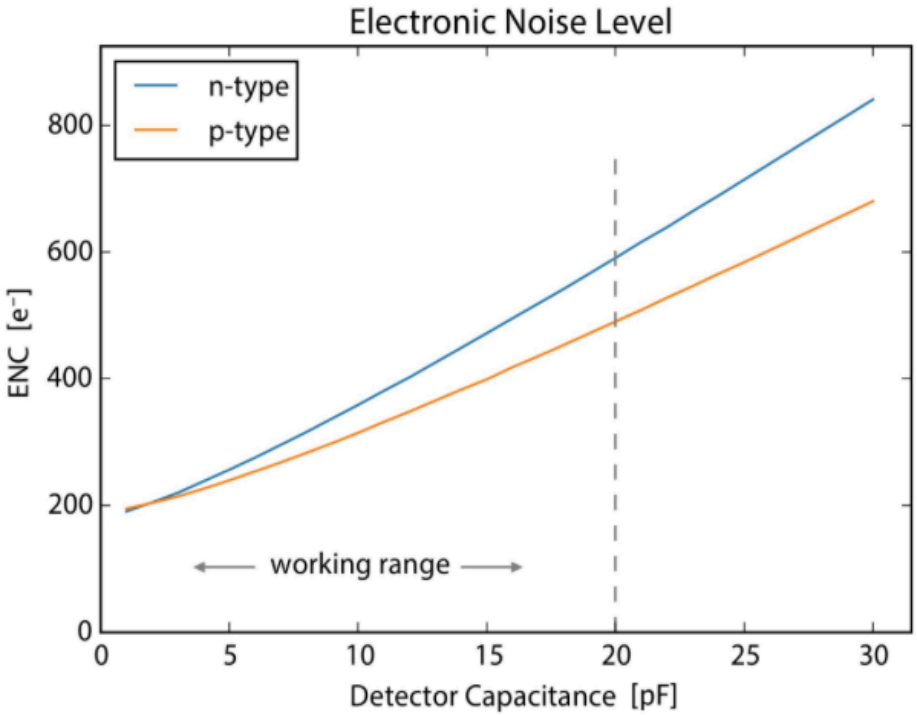
- Low noise sensitivity
- Two for each channel : energy and time branches



Front-End Simulations

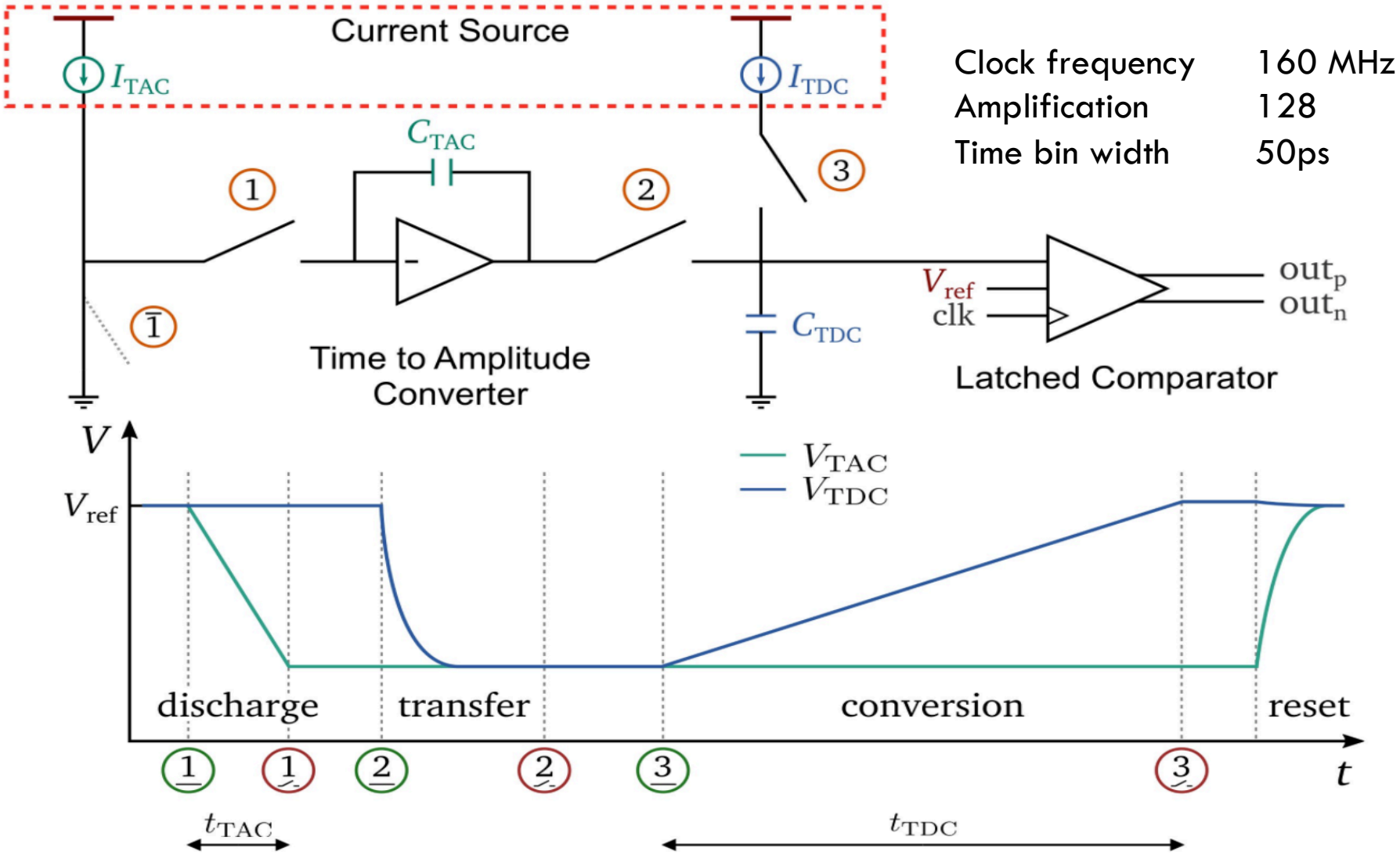


ToT linearity in the input charge range of 1fC to 40 fC with a capacitance of 25 pF



Electronic noise considering an input capacitance in the range 1pF to 30 pF with an input charge of 4fC

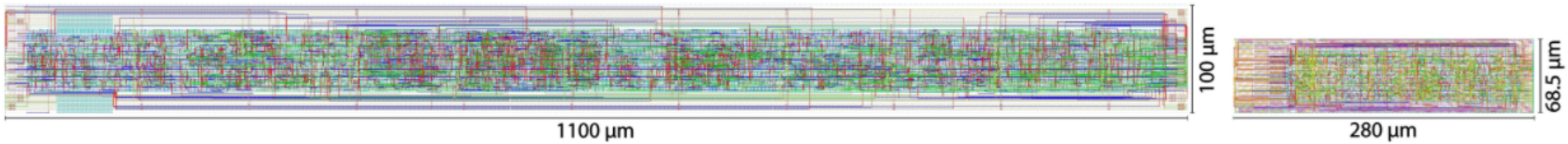
Analog TDC Performance



Clock frequency	160 MHz
Amplification	128
Time bin width	50ps

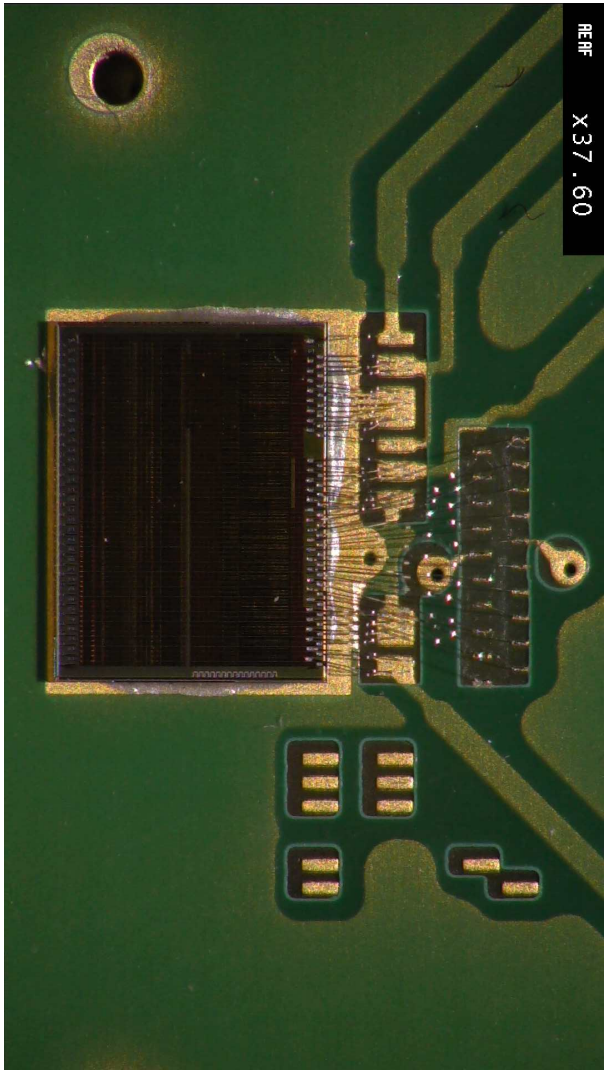
Digital Controllers

- Optimization of the TDC Controller
  - Size reduced by 80%
  - Overall power consumption halved
  - Radiation-hard logic implemented



- Single Event Upset protection
  - 1bit : TripleModular redundancy
  - n bits : Hamming encoding

Current Status



- Chip bonded to the power board
- Power supplies tested
- Readout system under test

Outlook

- Board in production
- First tests scheduled
- Beam test with sensor planned in the middle of the year

HIC for FAIR
Helmholtz International Center

panda

FAIR

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Thank you for your attention

GEFÖRDERT VOM

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und Forschung

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