



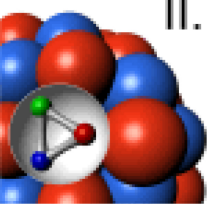
A time digitizer for the microstrip detectors of the PANDA MVD

Alberto Riccardi¹

Kai Thomas Brinkmann¹, Valentino Di Pietro¹, Sara Garbolino², Angelo
Rivetti², Manuel Rolo²

1) II. Physikalisches Institut Justus-Liebig-Universität Gießen

2) INFN Sezione di Torino



II. Physikalisches
Institut

DPG Spring Meeting 2015

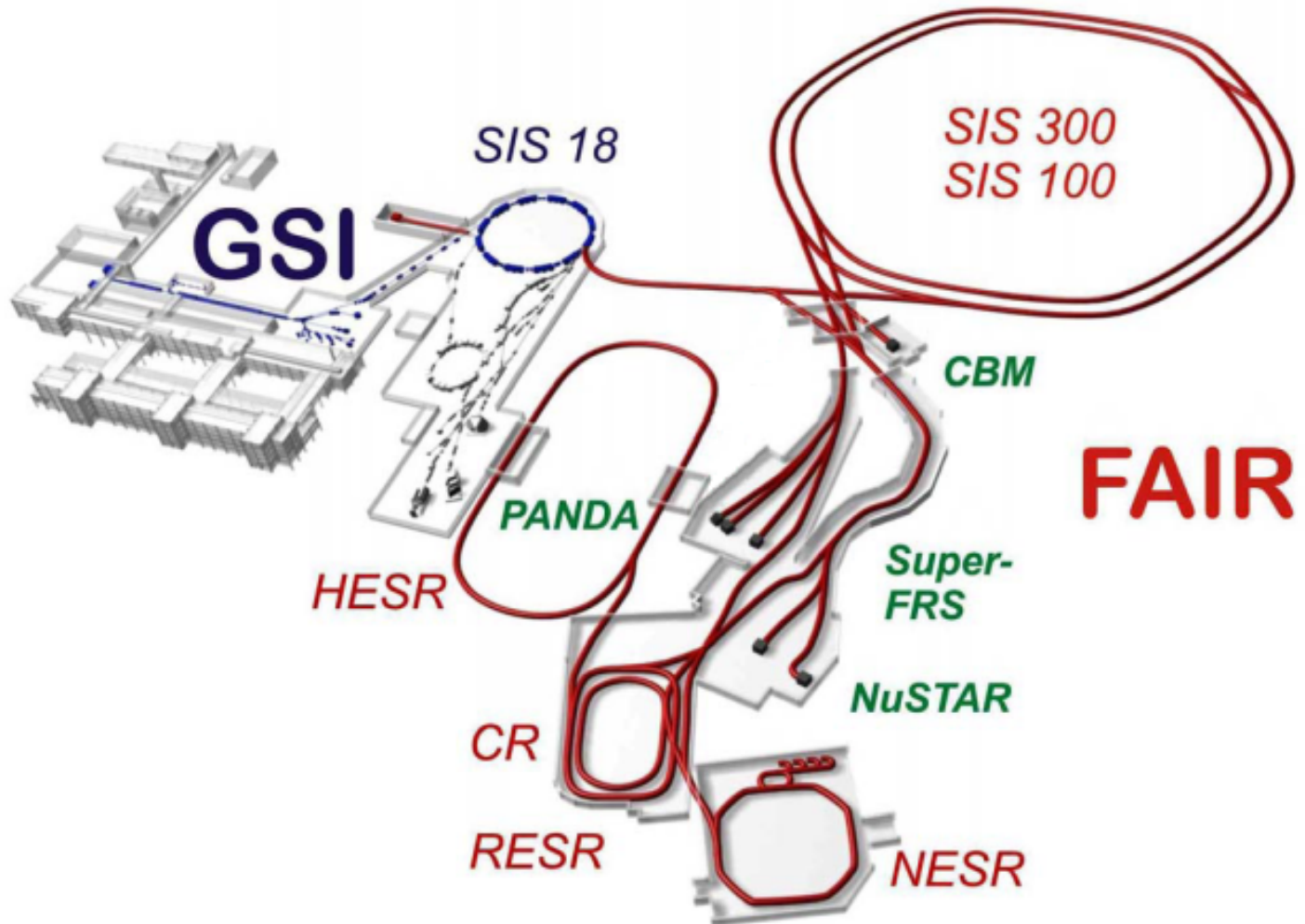


Contents

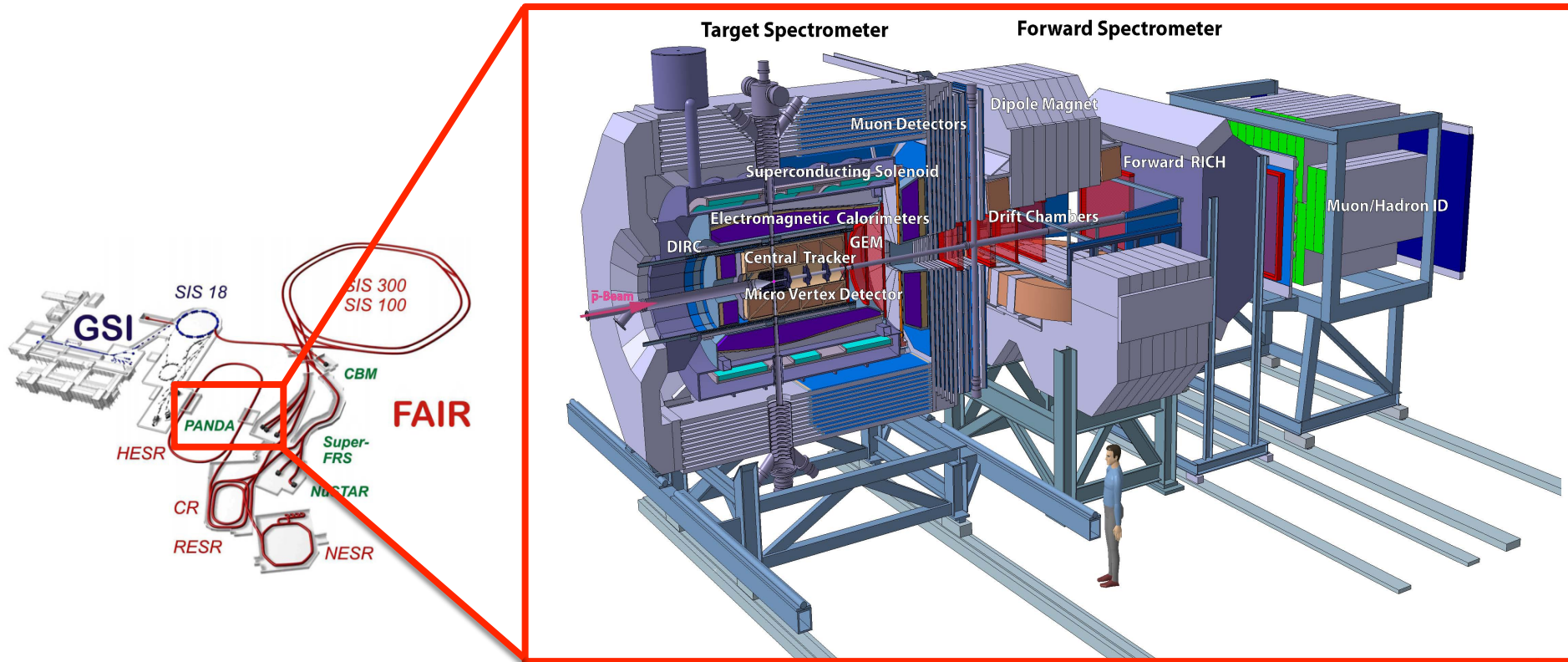


1. Context
2. Analog Time to Digital Converter
3. Layout and Post-Layout simulations
4. Outlooks

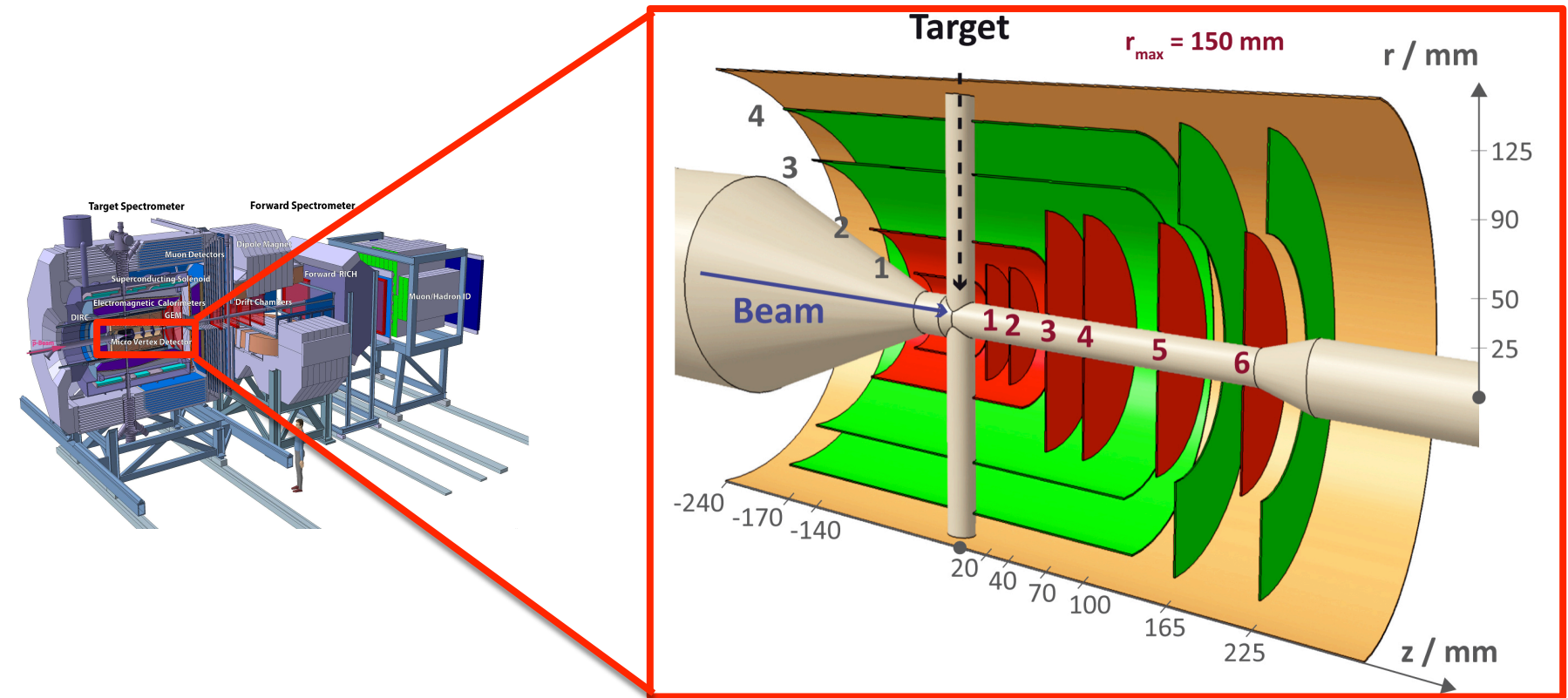
FAIR



PANDA

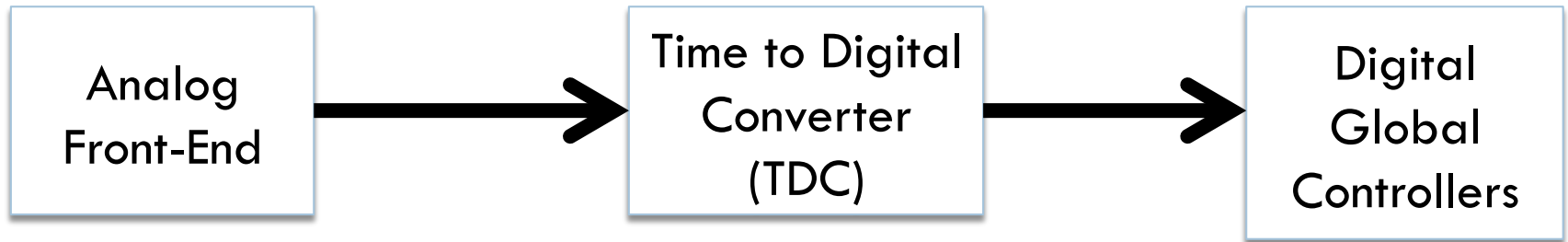


MicroVertex Detector

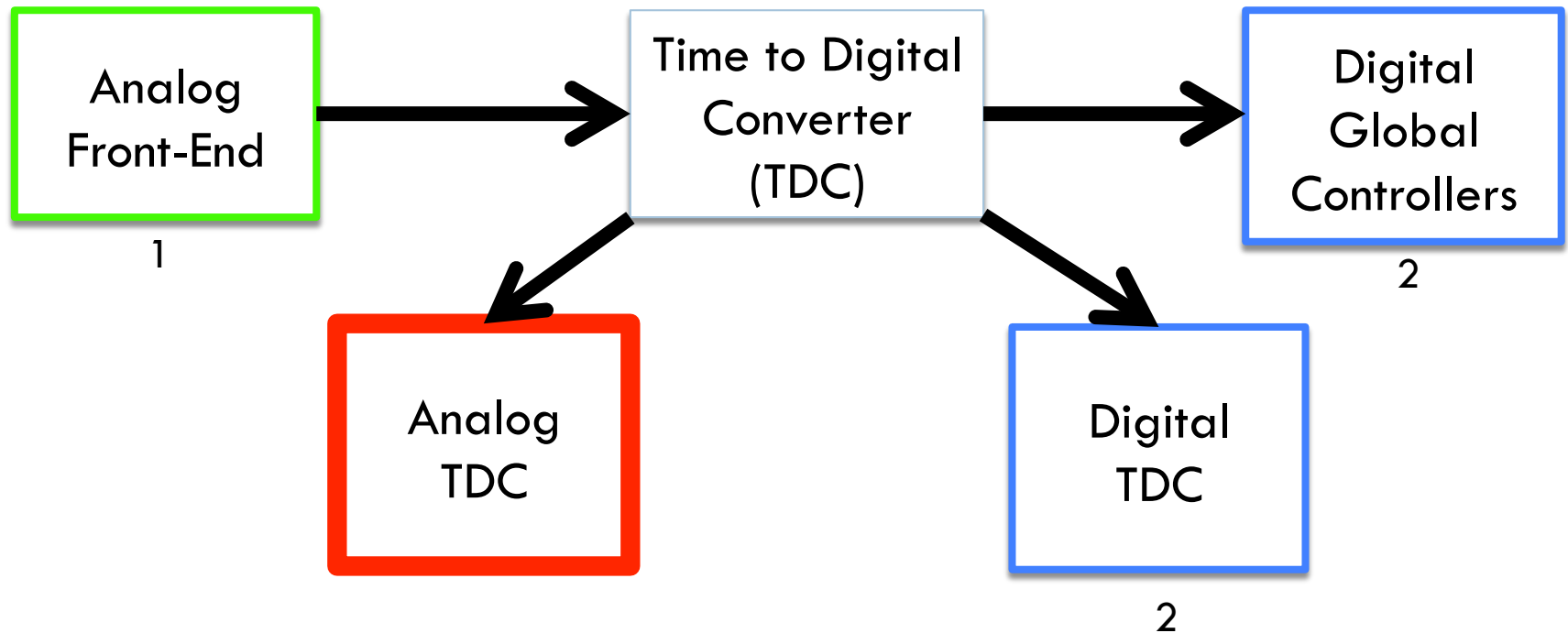


Red zone covered by pixels and green one by strips

PAnda STrip Asic (PASTA)



PAnda STrip Asic (PASTA)



1) Valentino Di Pietro, HK 30.3

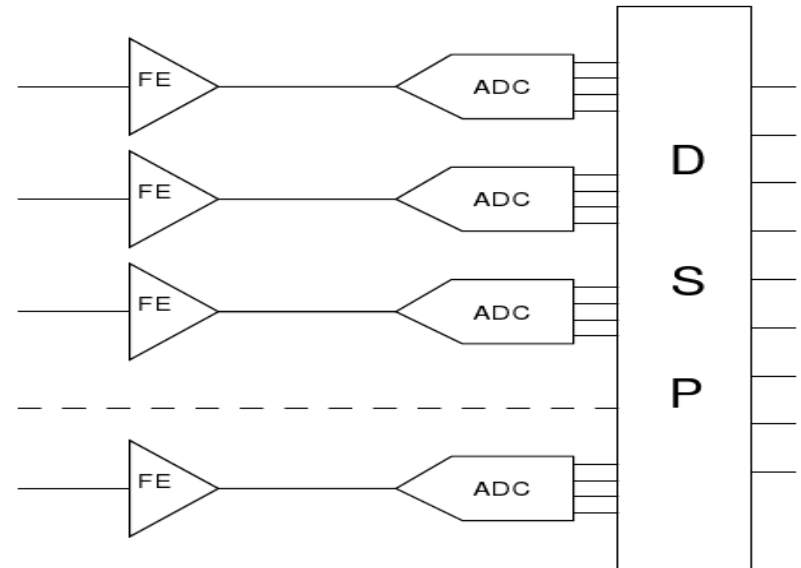
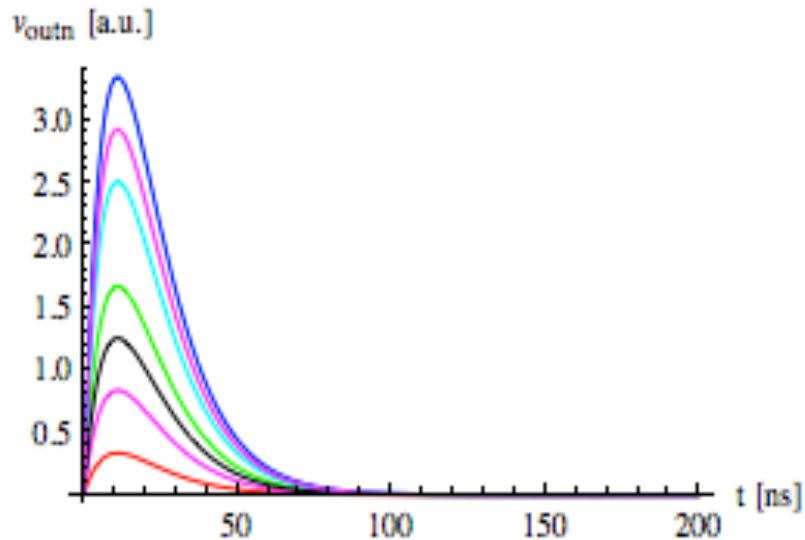
2) André Goerres, HK 50.2

Requirements



- Rate/channel ~ 40 kHz
- ~ 4 mW per channel
- **Triggerless**
- **Preserve the charge information**
- **Only digital outputs**

Standard Approach

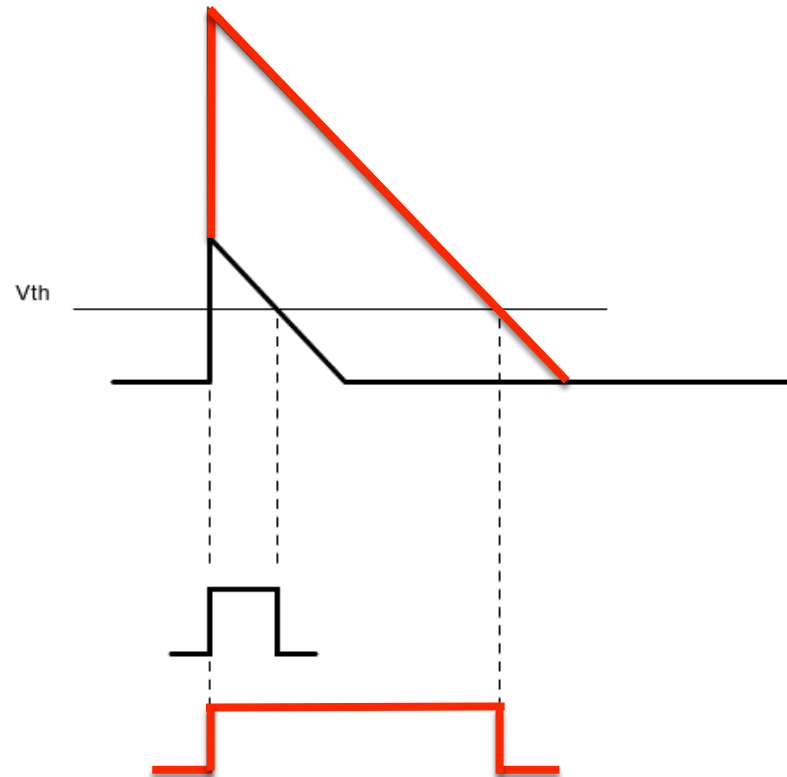


Usually to obtain the charge information the front-end signal amplitude is measured. To obtain this information the classic structure is that is reported in figure.

✓ All signals have the same durations

X Complex to implement
X Limited range

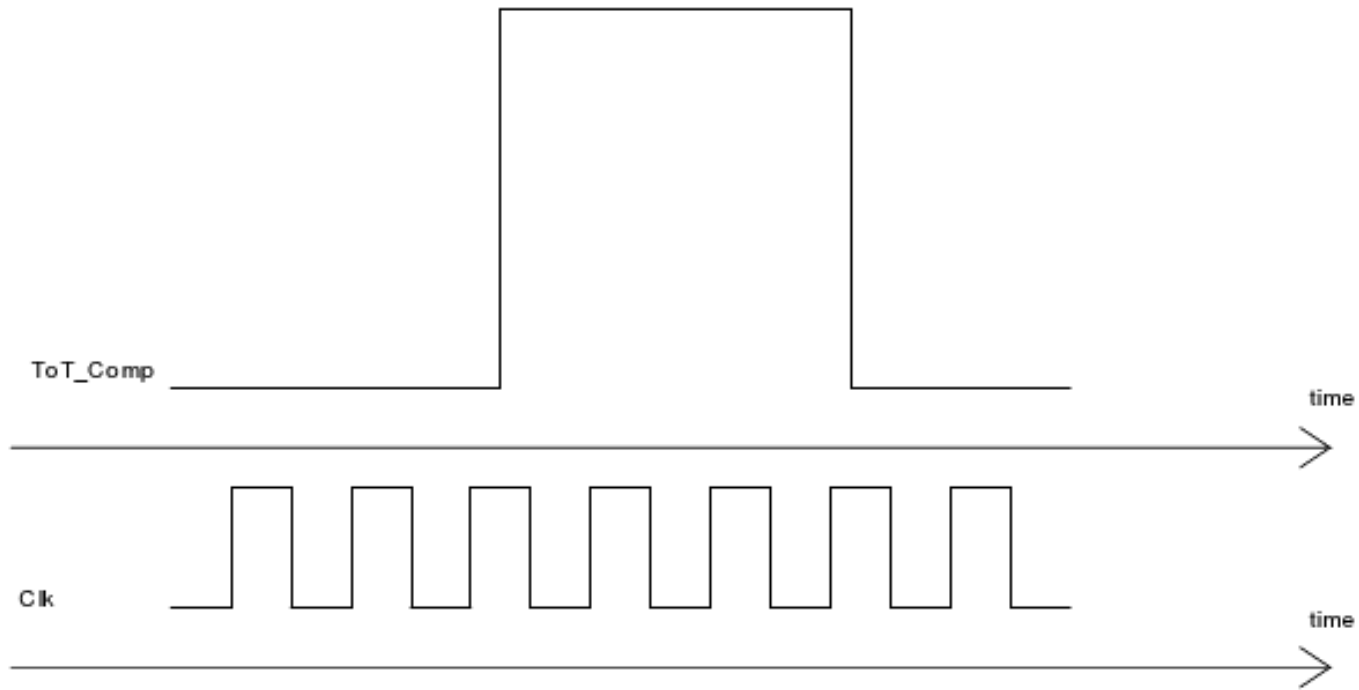
Time Over Threshold Technique



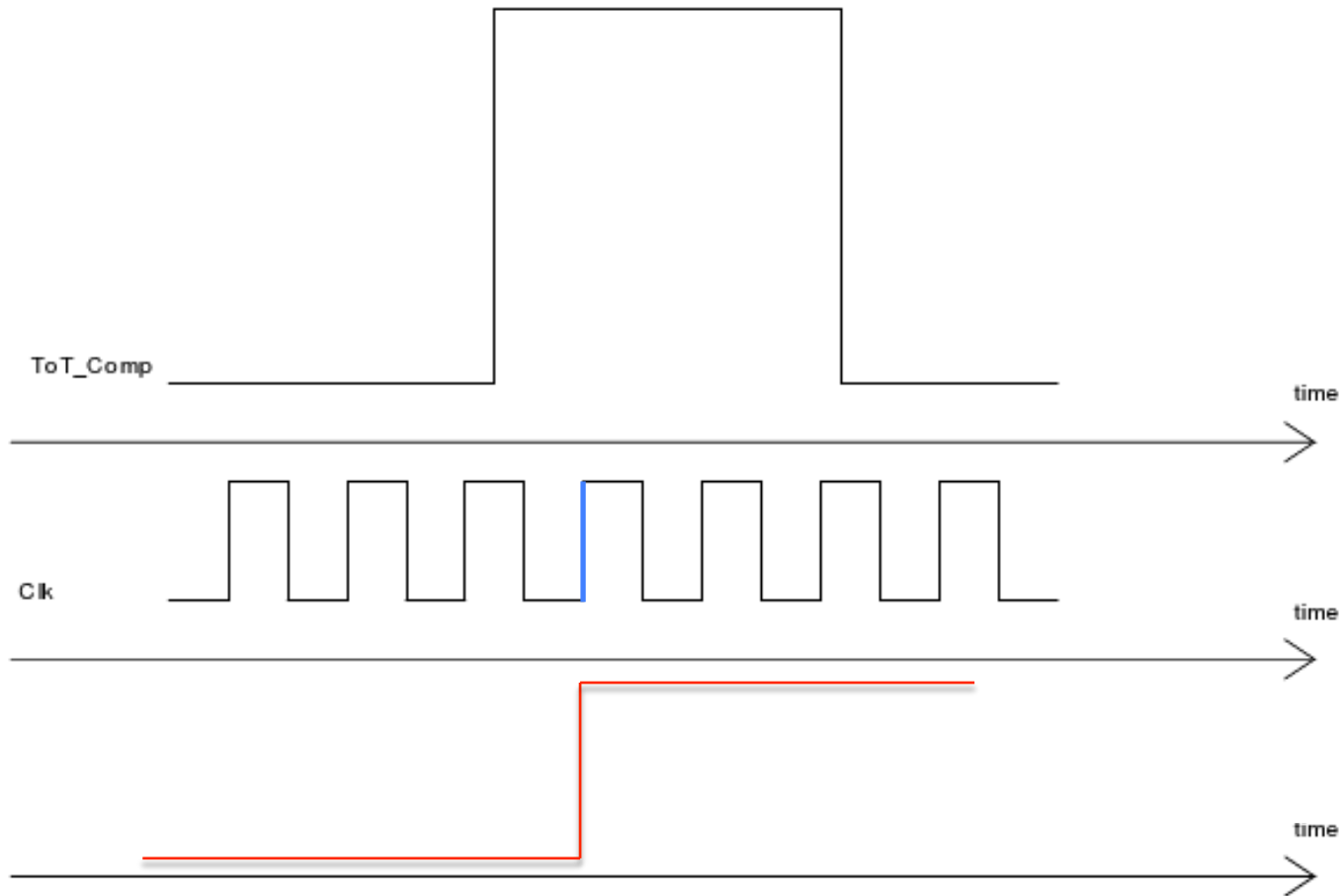
- ✓ Easier to implement
- ✓ Larger dynamic range
- ✓ Measure charge and time stamp

x Pile-up problems

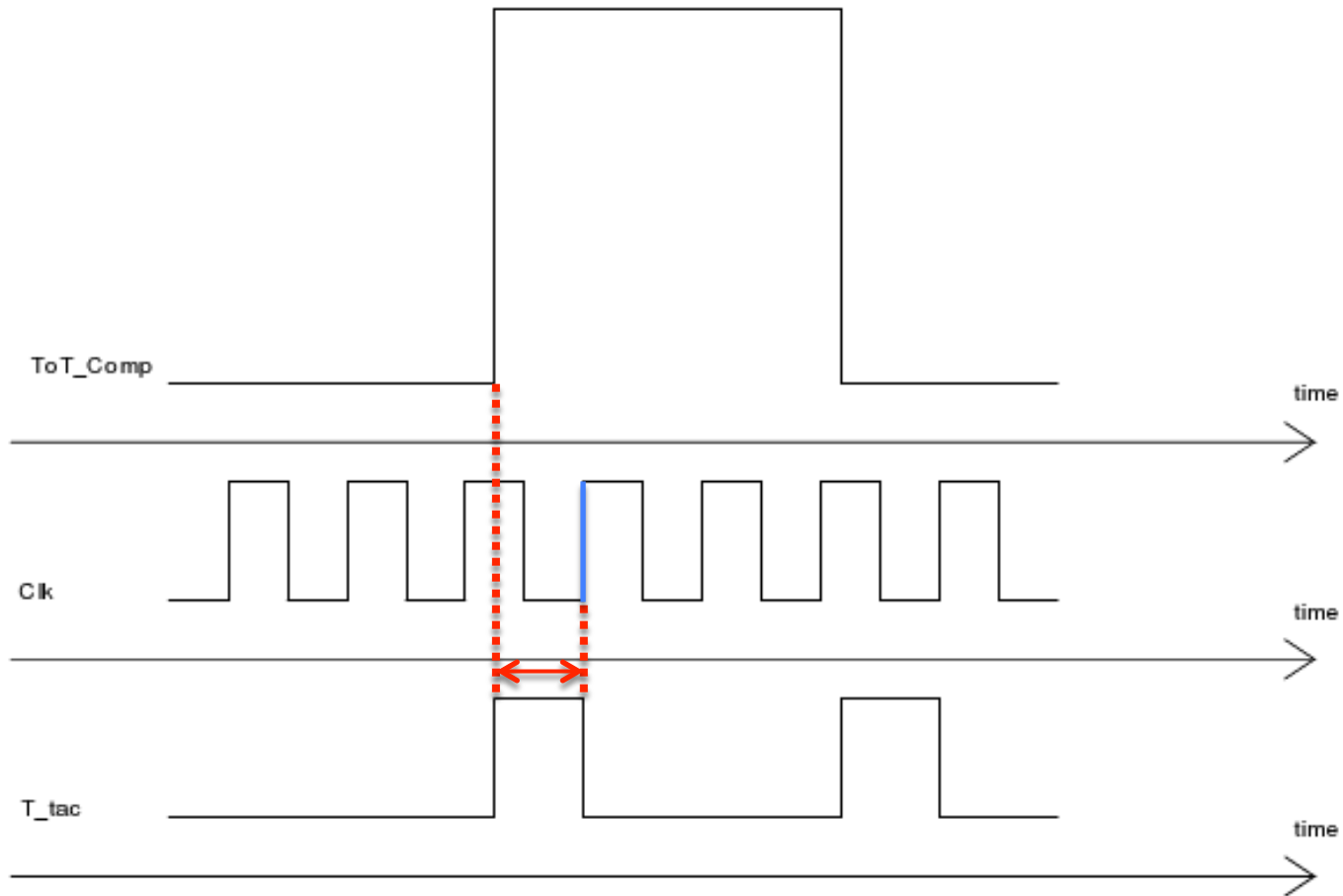
Timing



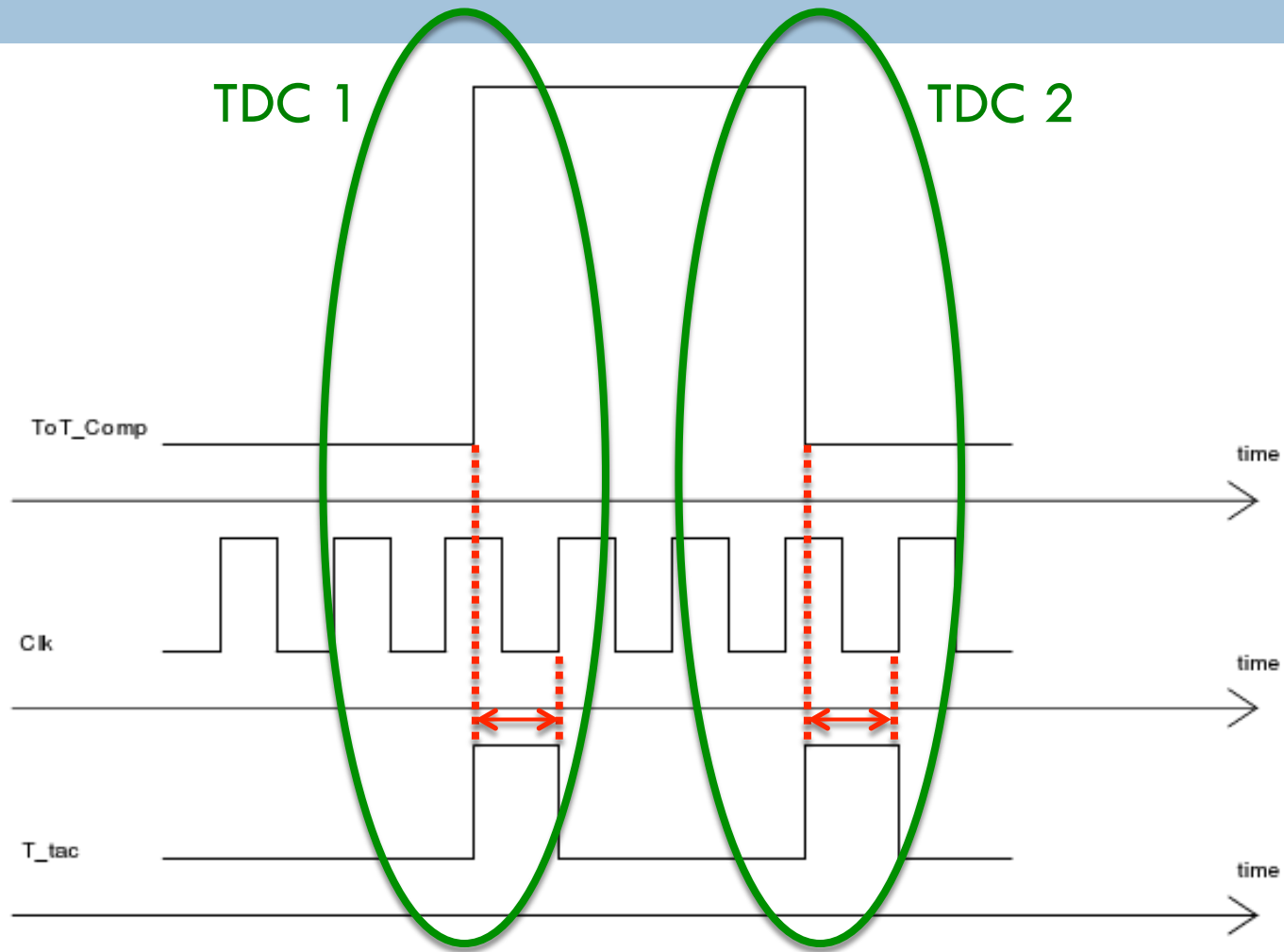
Timing



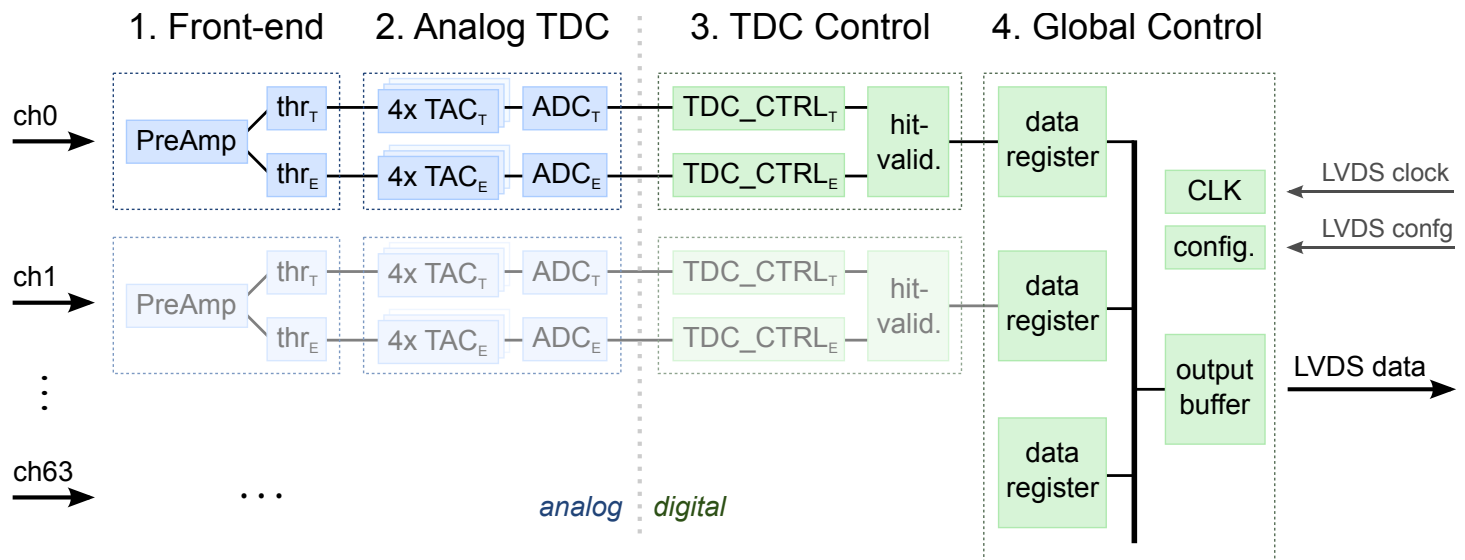
Timing



Timing



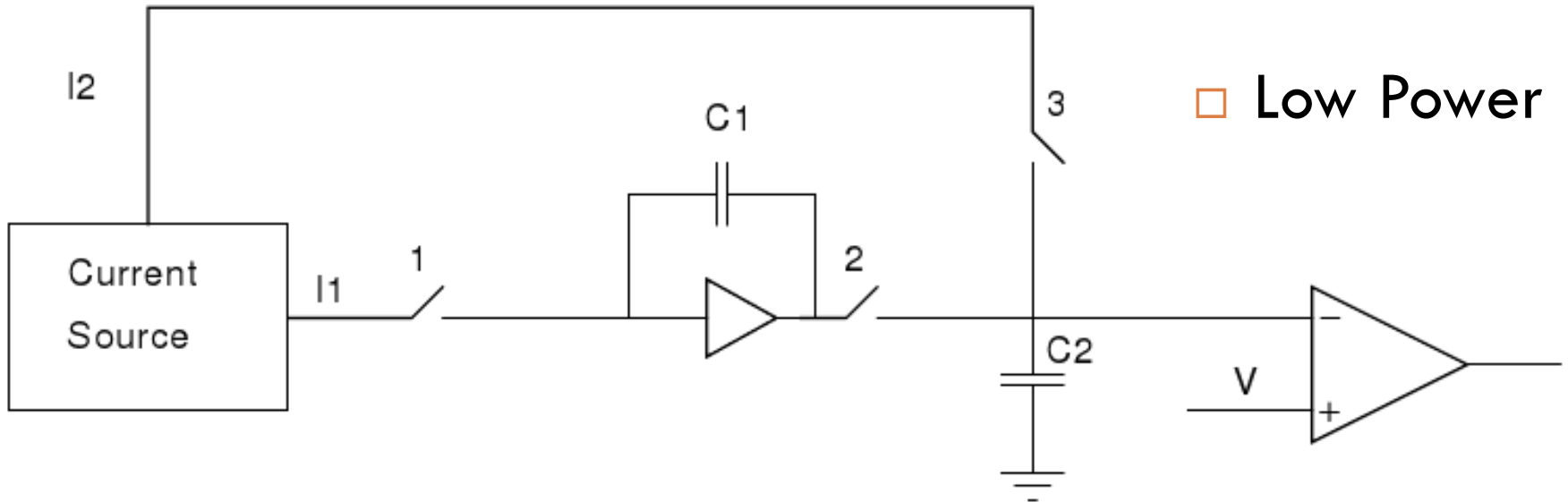
Chip Architecture



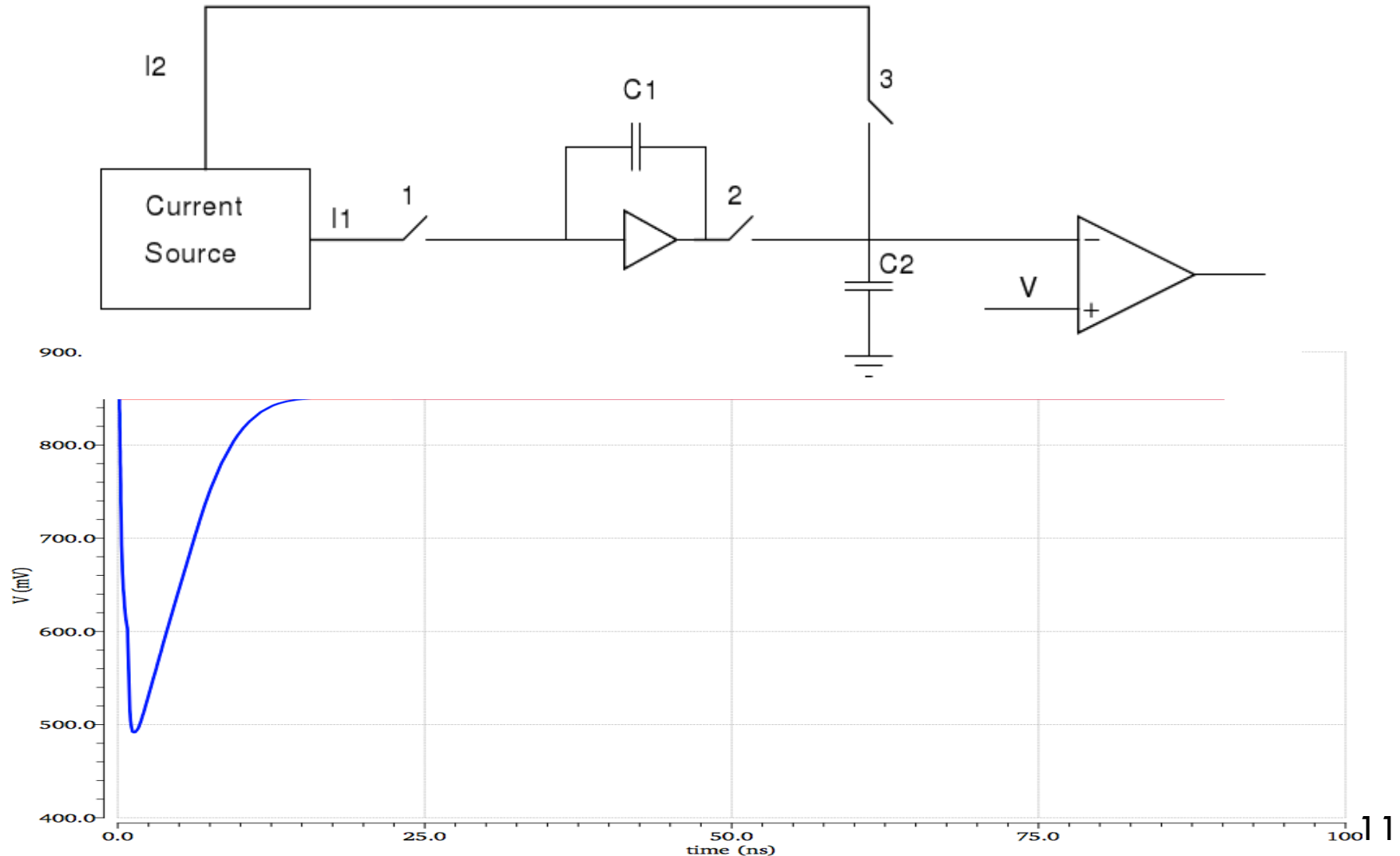
1. Amplification & discrimination
2. Time interpolation, Wilkinson ADC
3. Control charging & initiate storing
4. Handling configuration & channel data

TDC Implementation

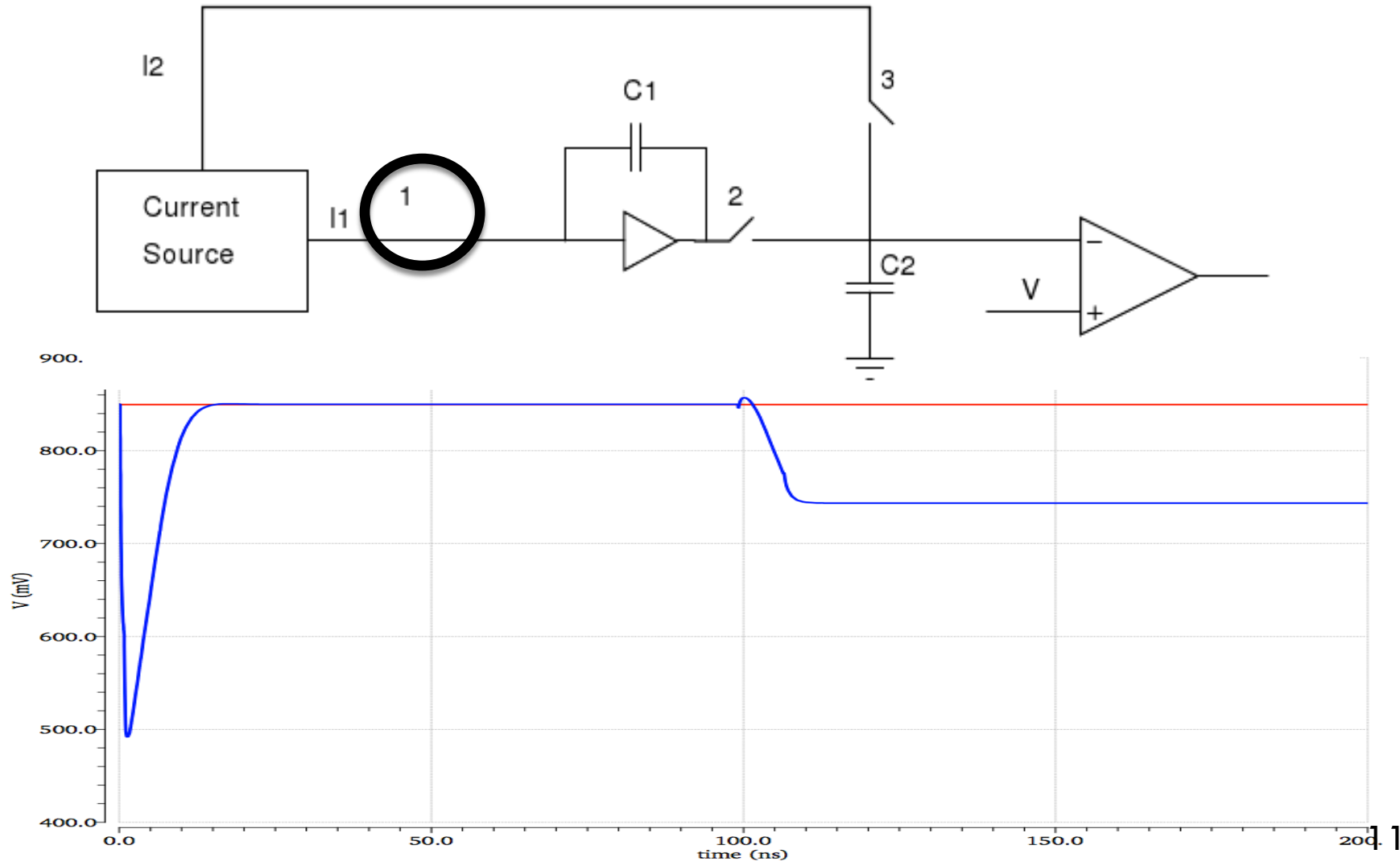
- Accurate
- Compact
- Low Power



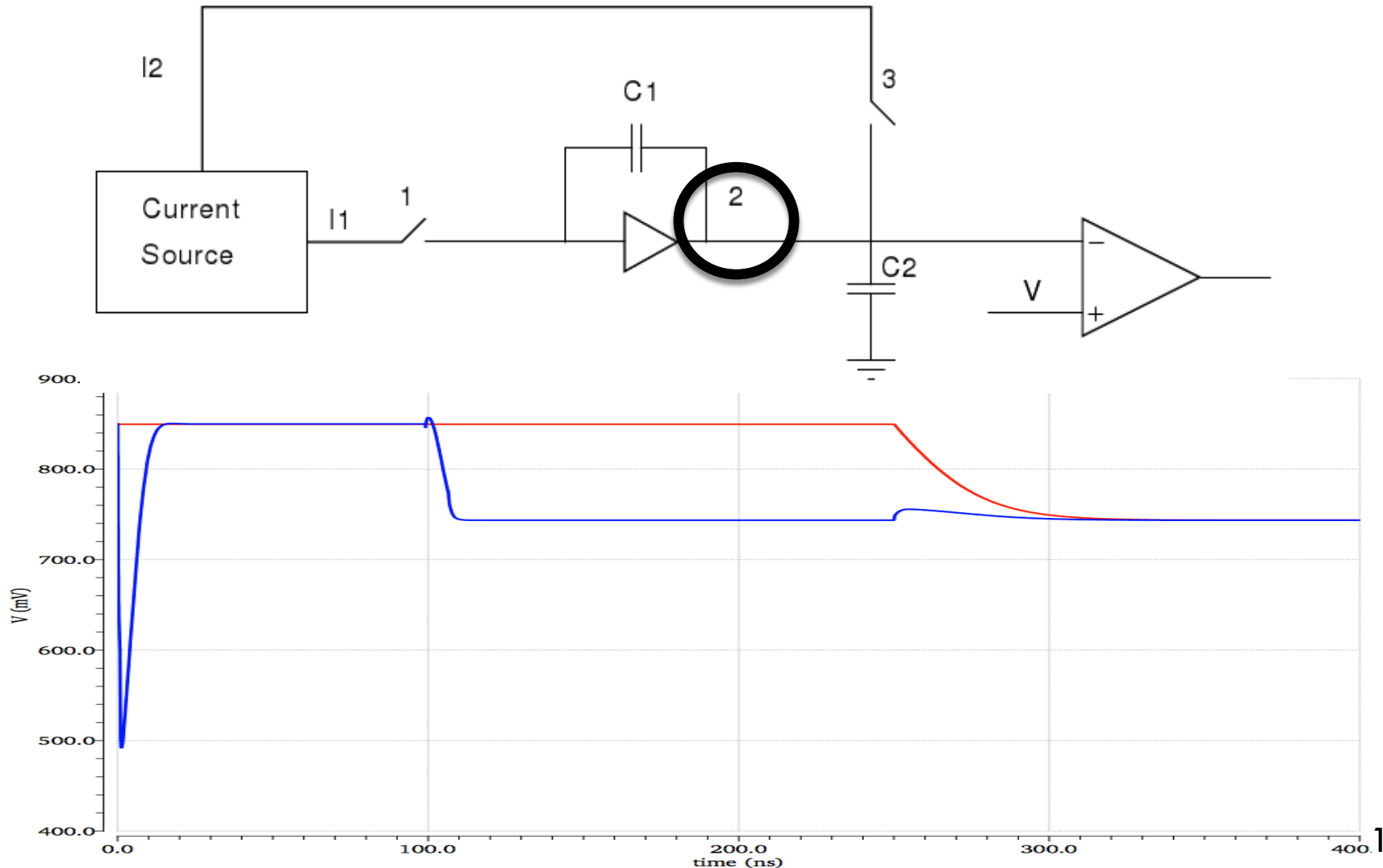
TDC Implementation



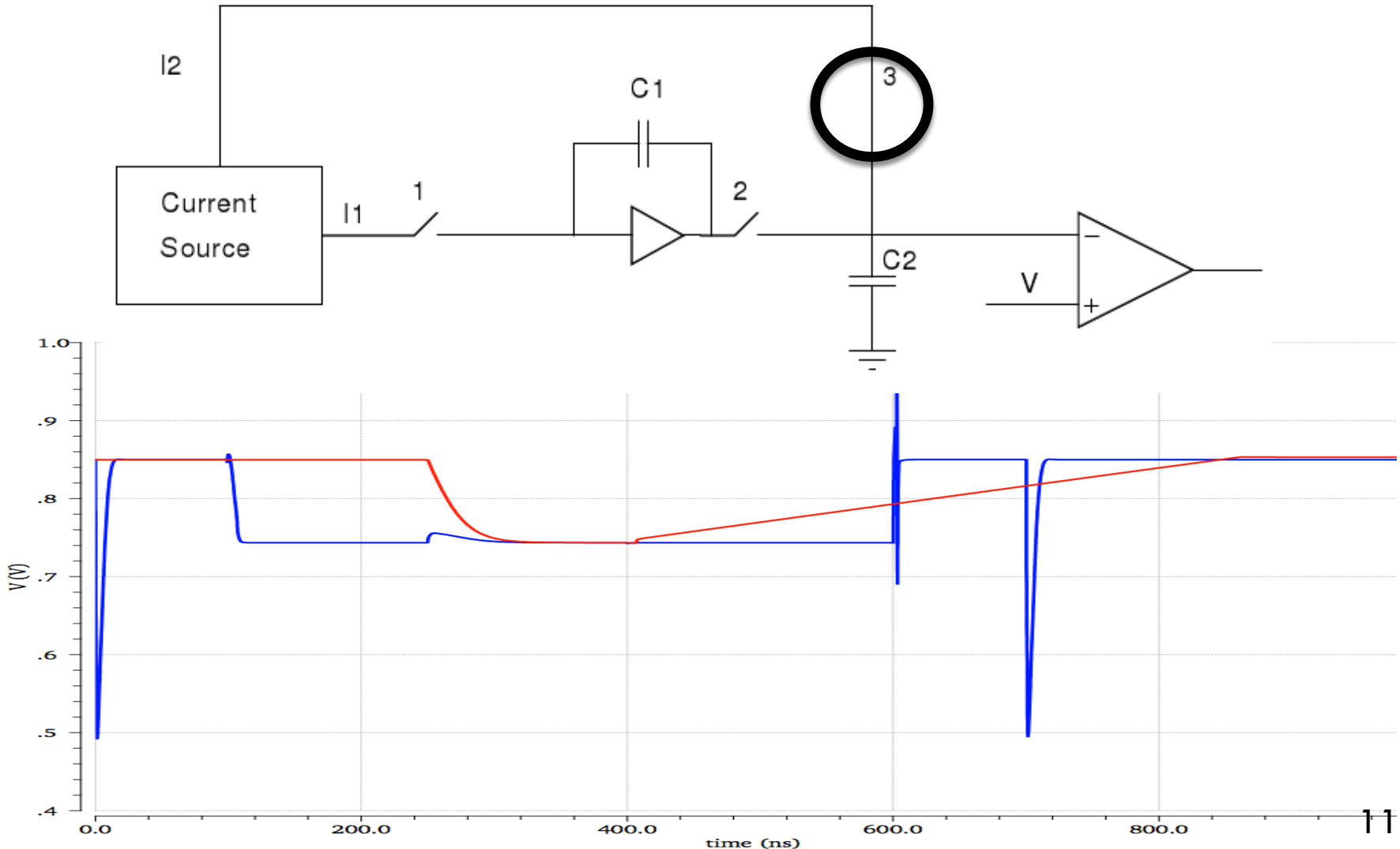
TDC Implementation



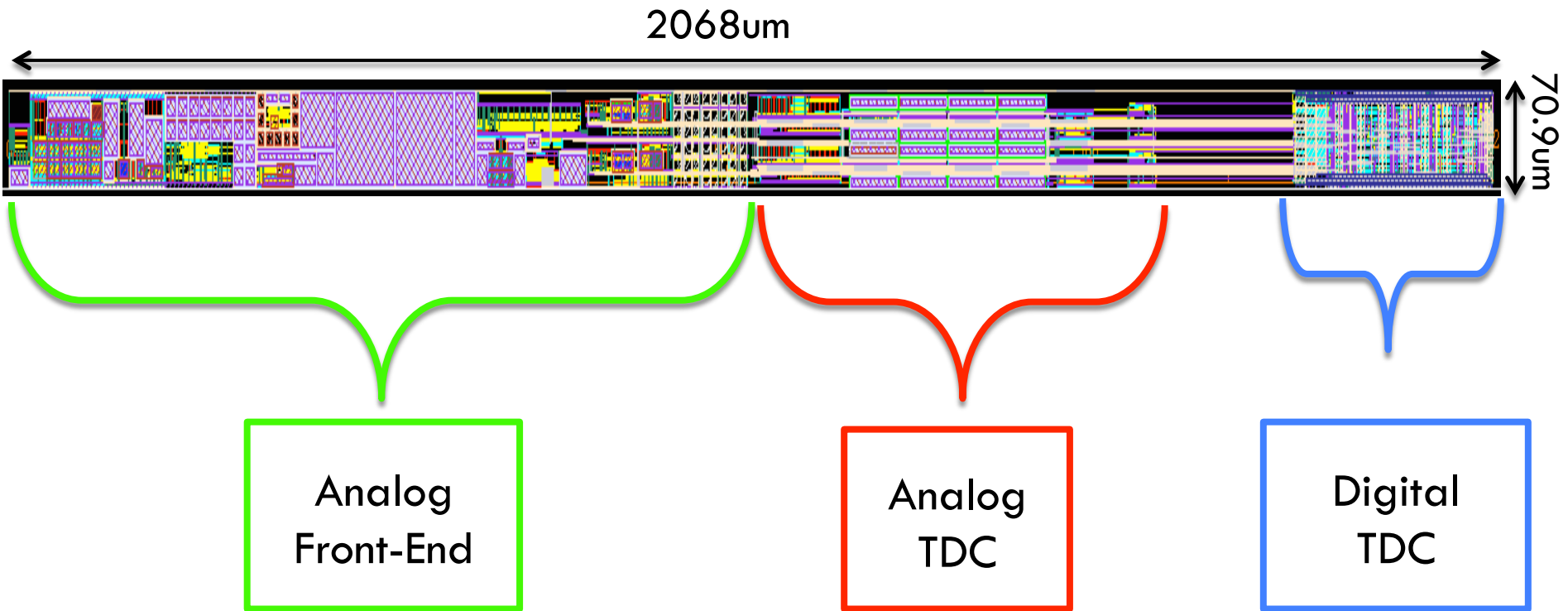
TDC Implementation



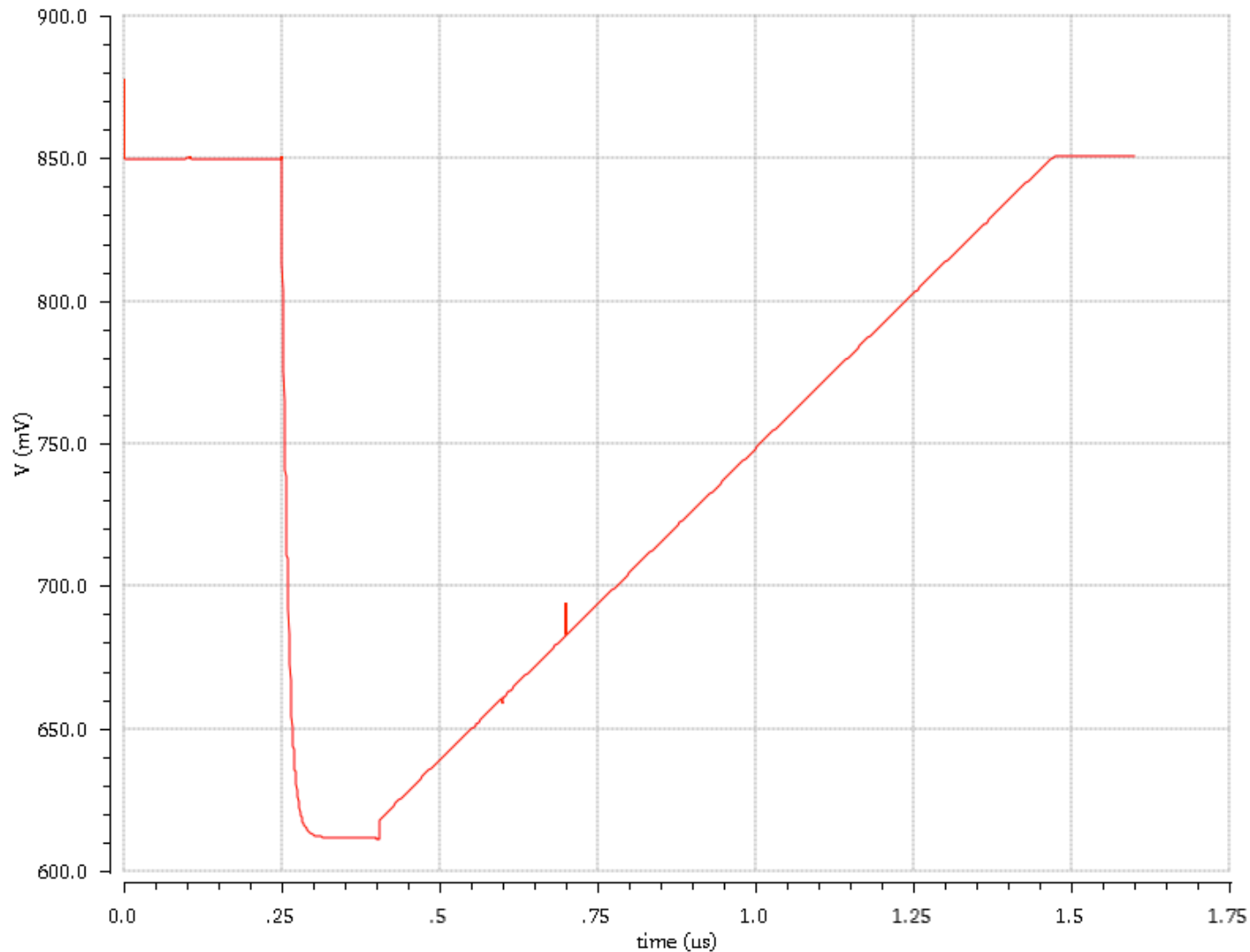
TDC Implementation



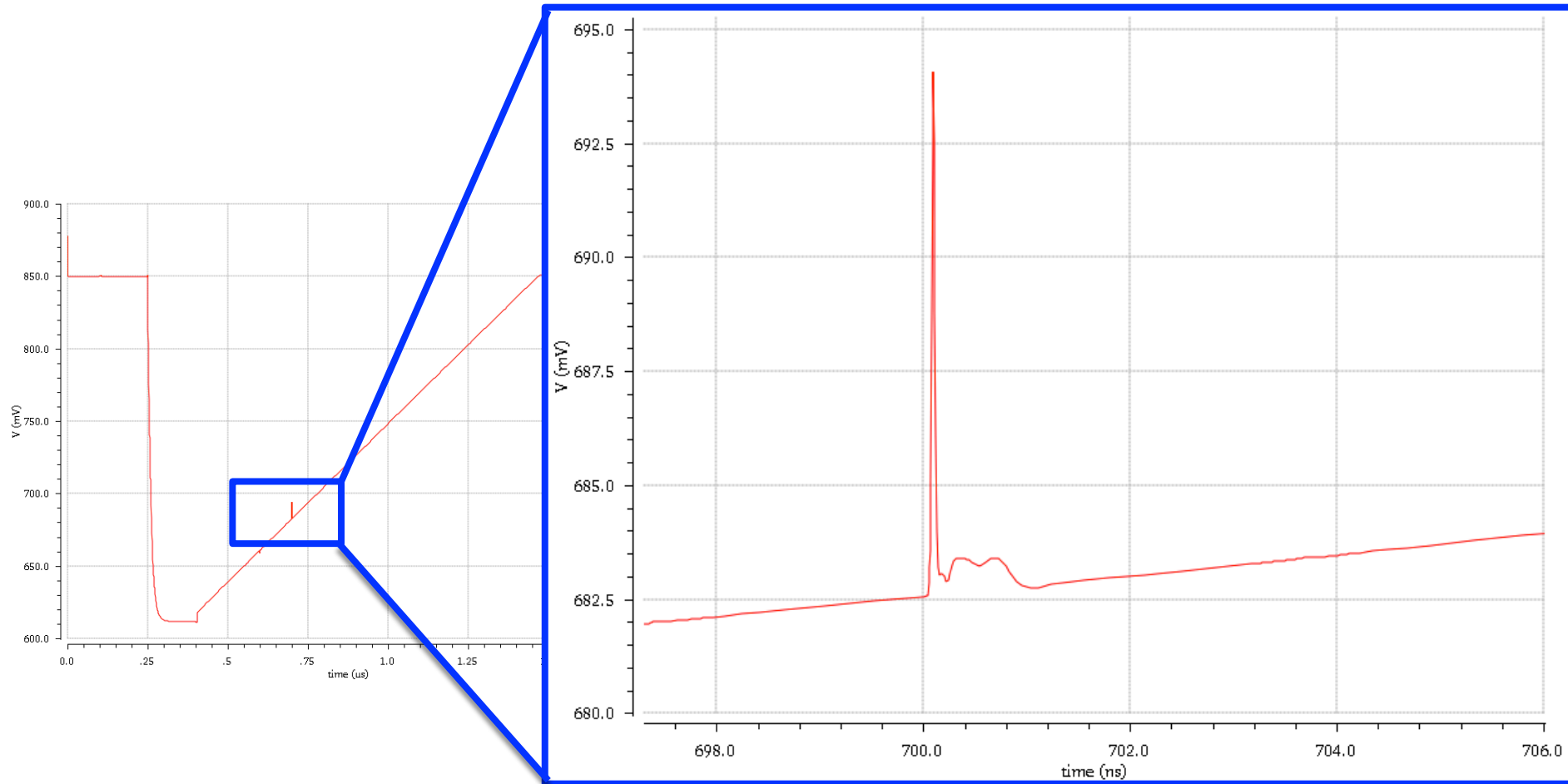
Channel Layout



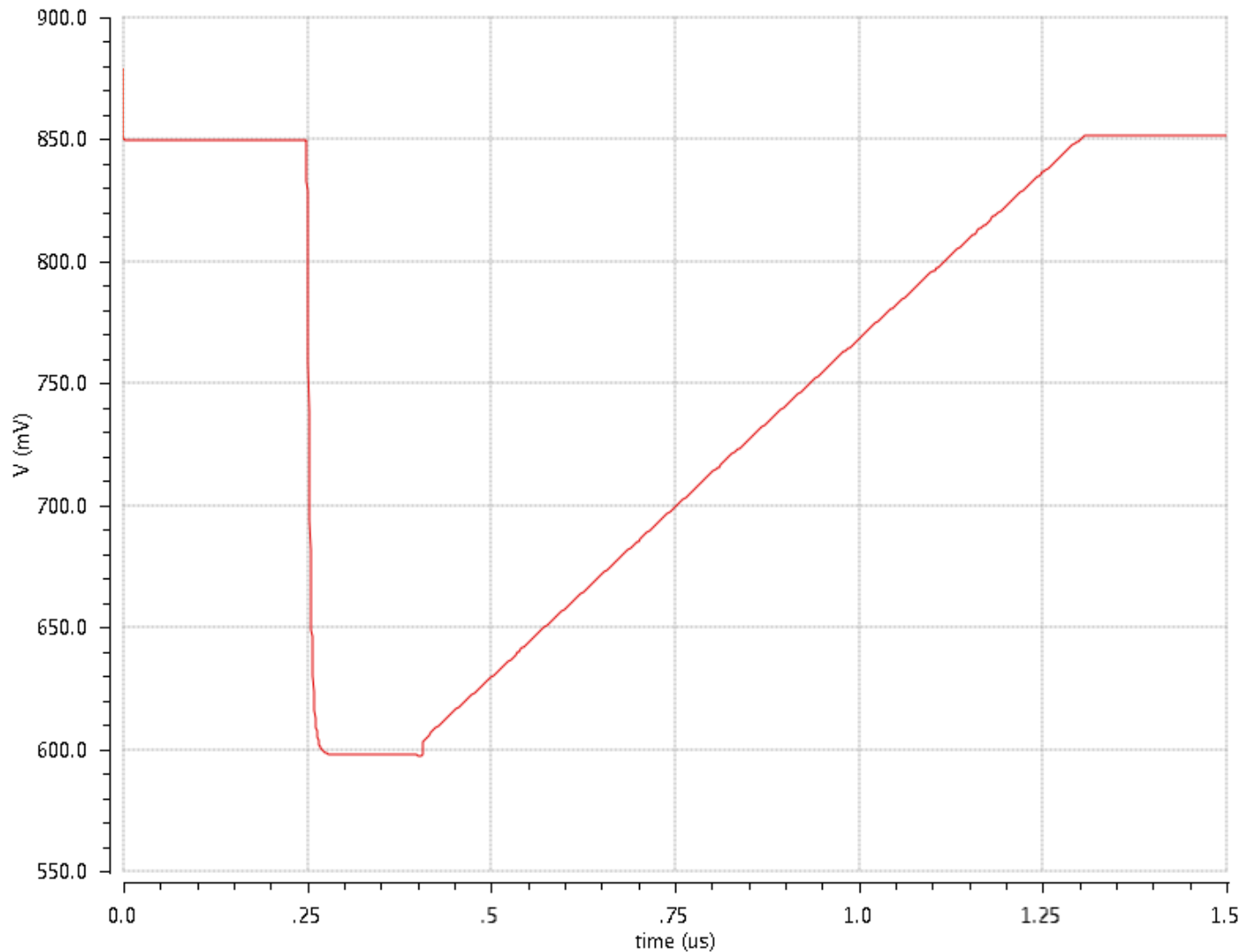
TDC Post-Layout Simulations (1)



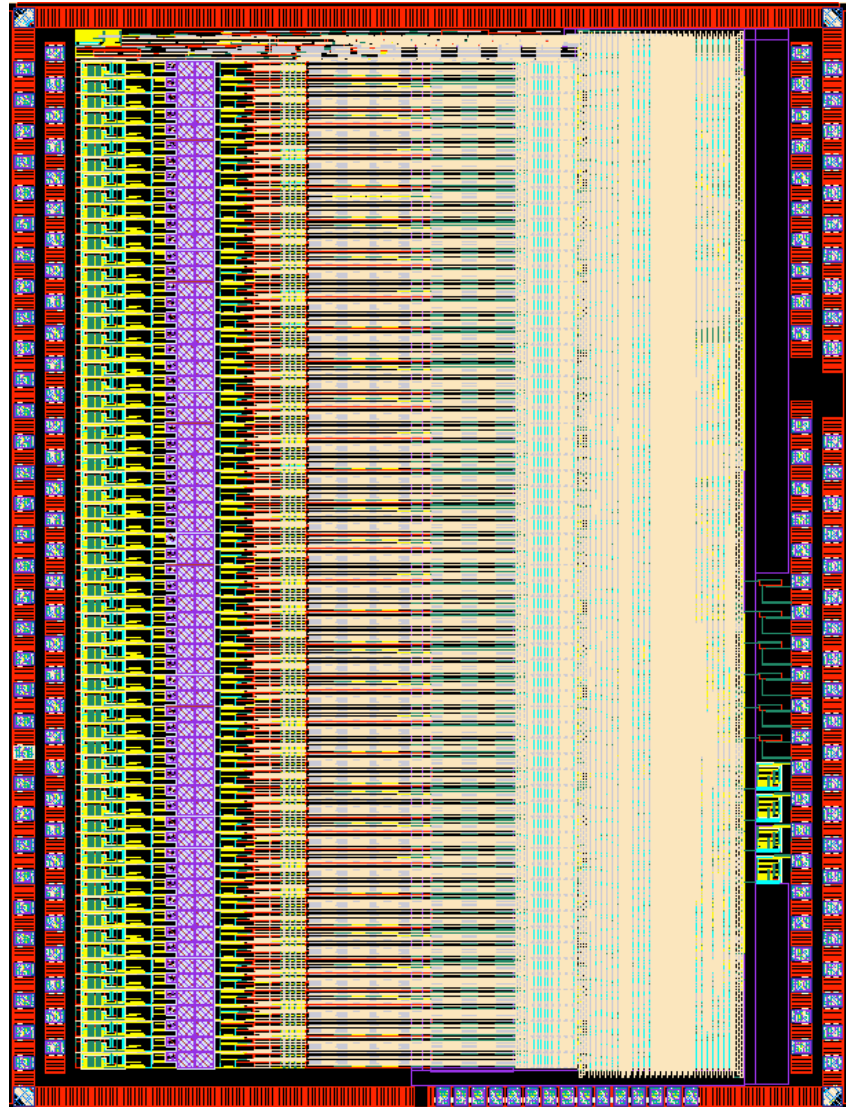
TDC Post-Layout Simulations (1)



TDC Post-Layout Simulations (2)



PASTA Layout



Outlooks



- Perform the last simulations
- Work on the readout system

Thank you for your attention

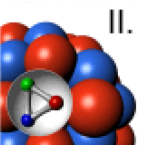
Alberto Riccardi

Alberto.Riccardi@exp2.physik.uni-giessen.de

GEFÖRDERT VOM



Bundesministerium
für Bildung
und Forschung



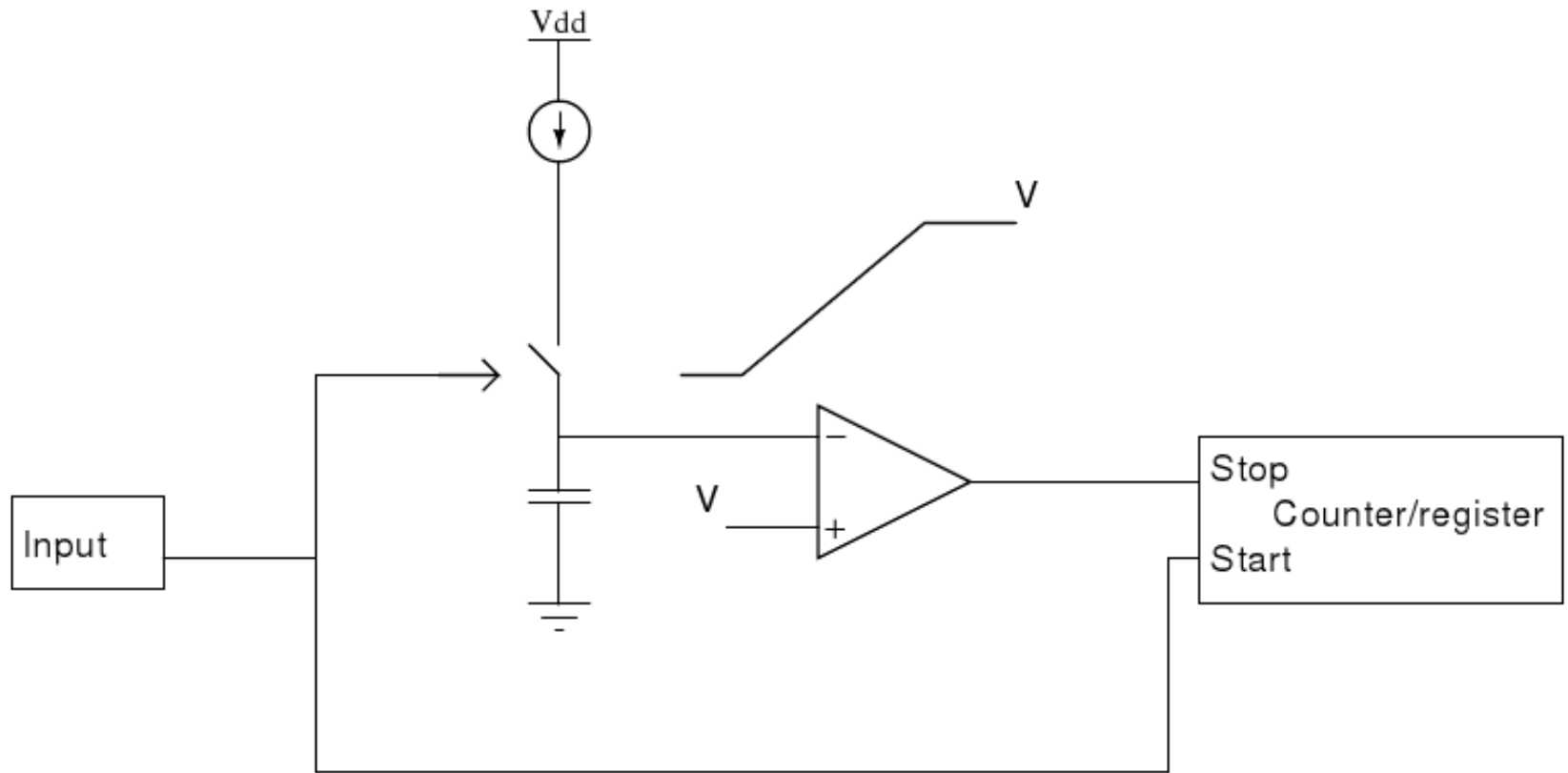
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HGS-HIRe for FAIR
Helmholtz Graduate School for Hadron and Ion Research

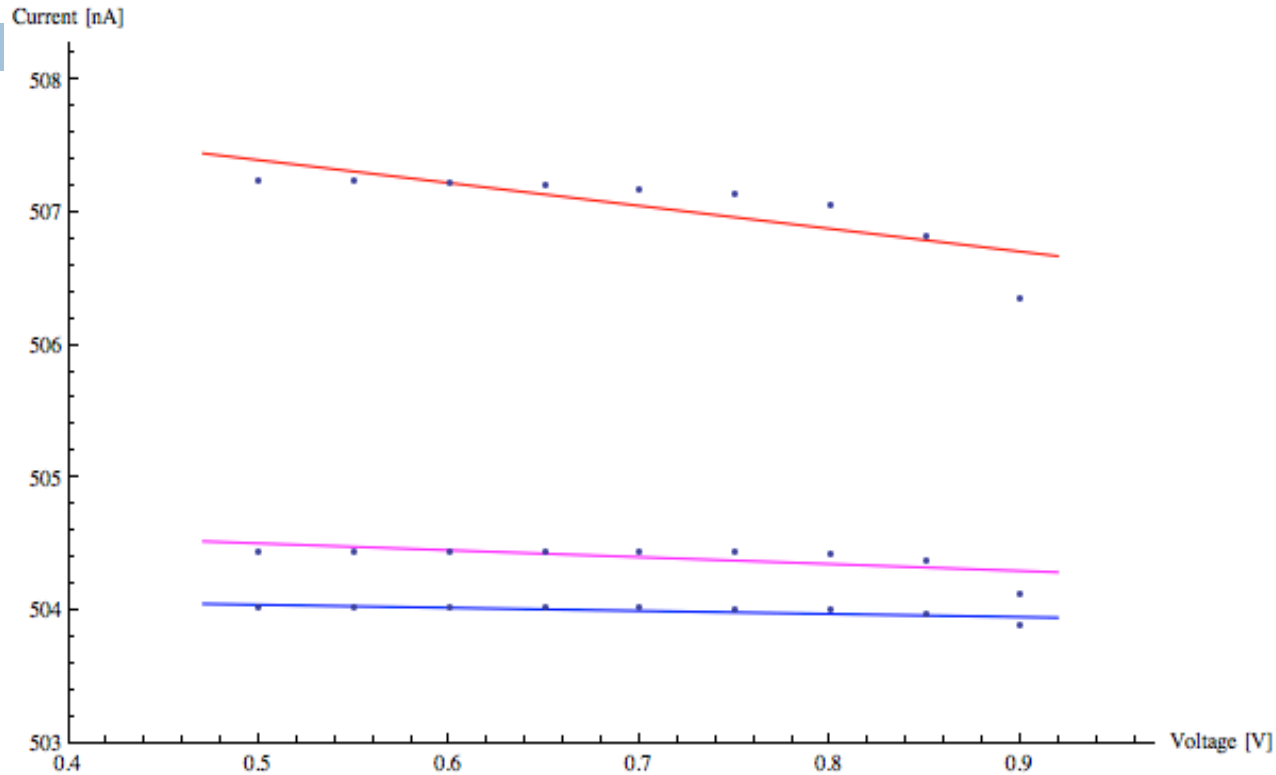
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UNIVERSITÄT
GIESSEN



Wilkinson ADC

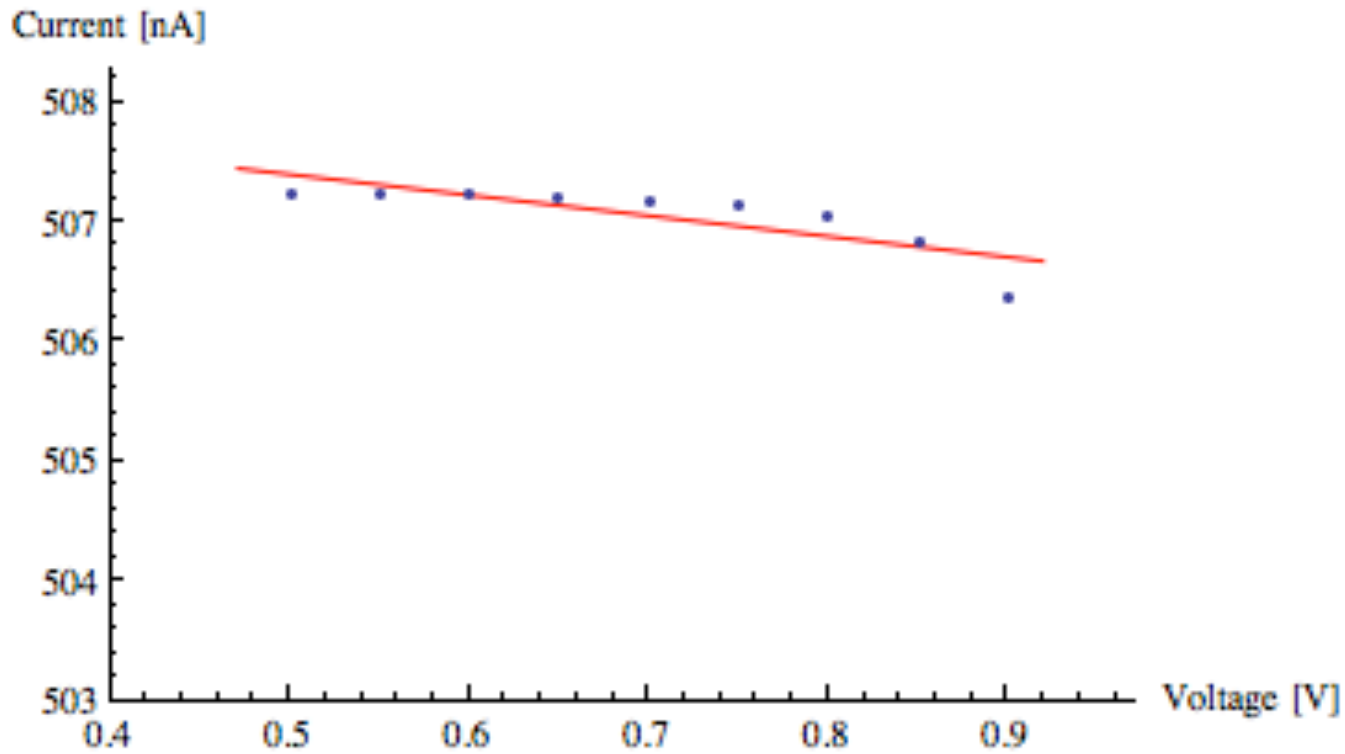


Costant Current Source: I_2 (2)



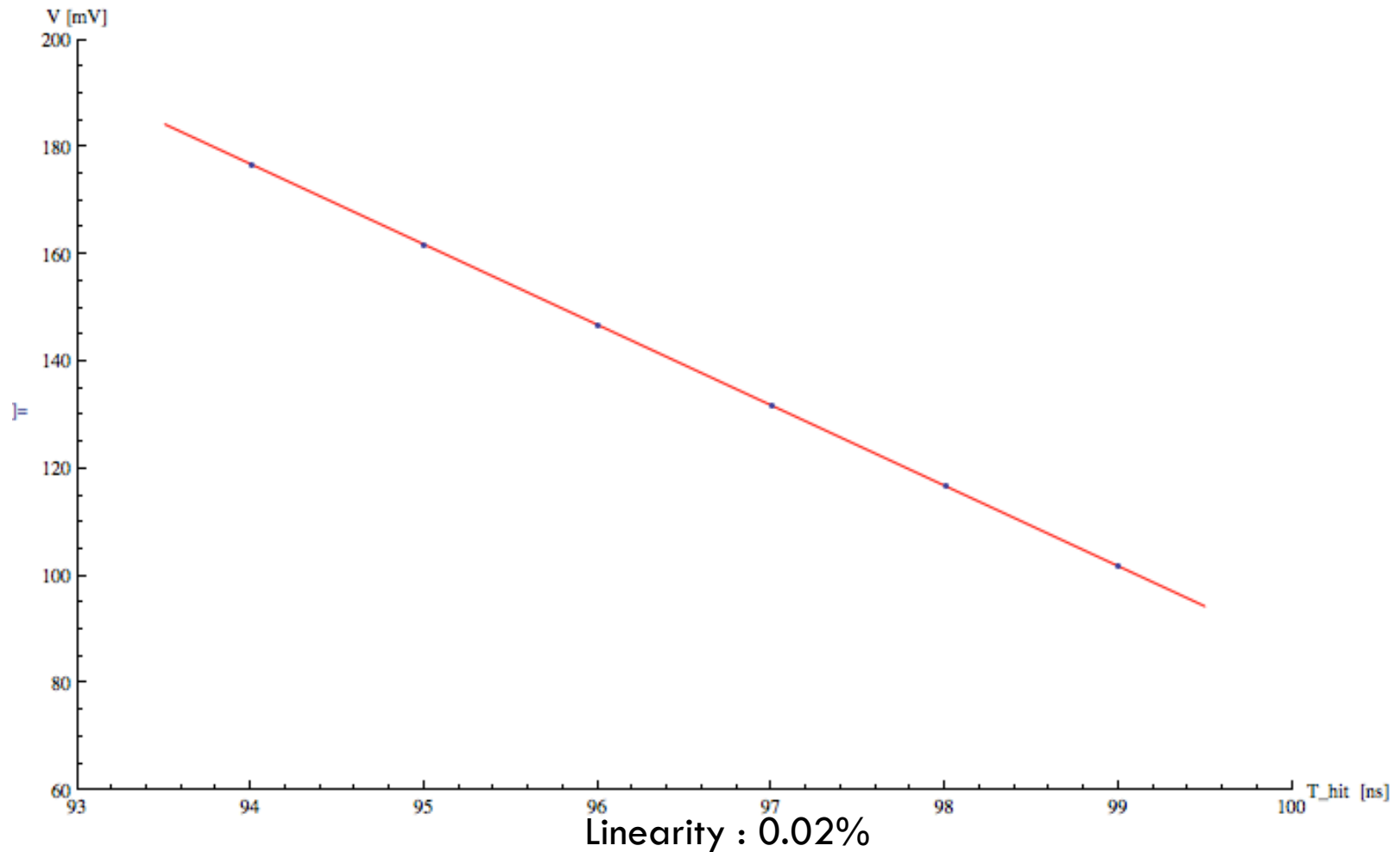
Nominal	0.408‰
FF	0.176‰
SS	1.360‰

Current error

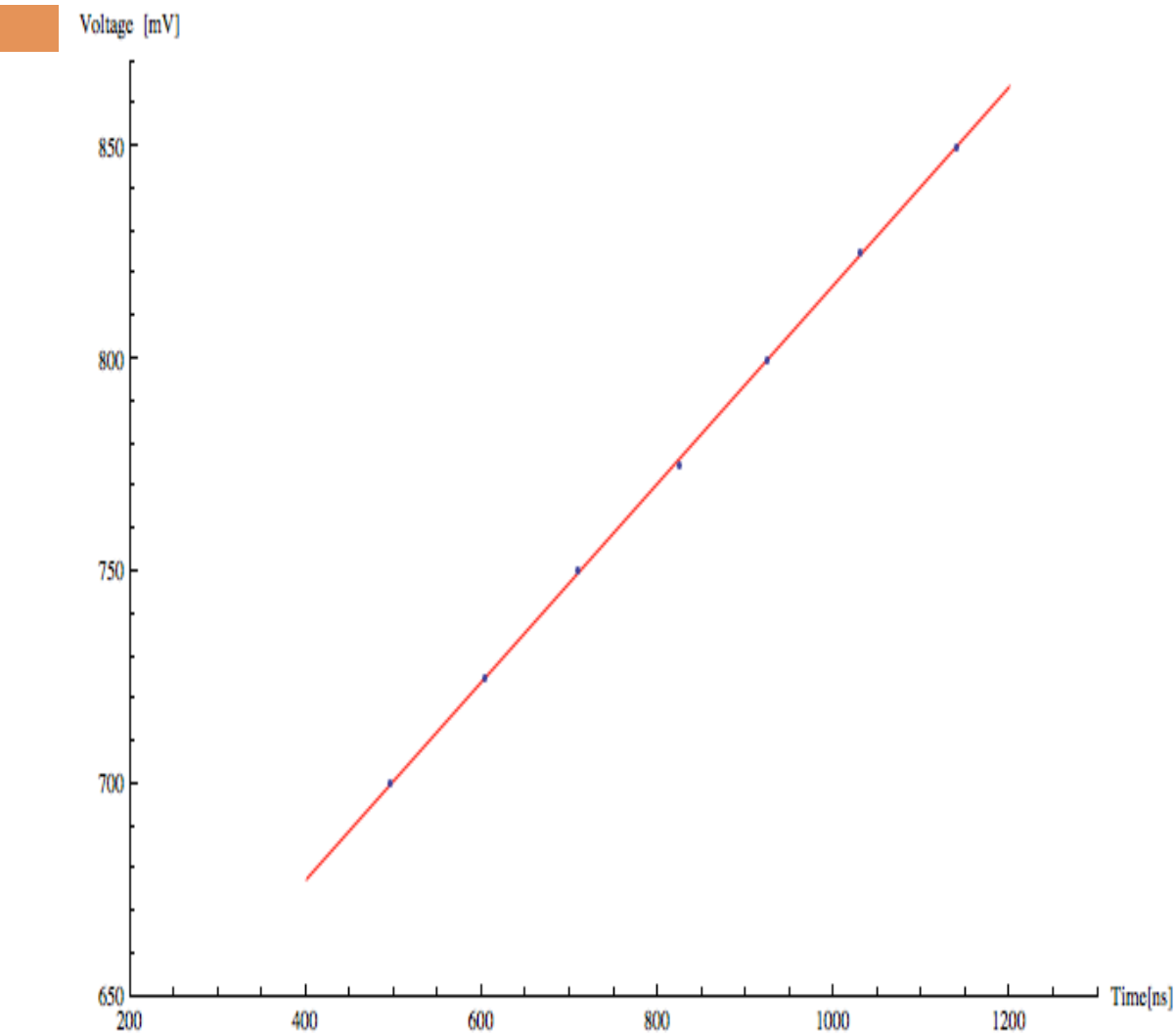


$$y = a + bx = 508.257 + 1.724x \quad \frac{\Delta y}{\langle y \rangle} = \frac{b}{\langle y \rangle} = 0.00340 \quad 0.00340 * 0.4V = 0.00136 = 1.36\%$$

TDC linearity(2)



TDC linearity (3)



T_hit (ns)	Goodness(%)
99	0.021
98	0.025
97	0.030
96	0.005
95	0.008
94	0.011