

FPGA-gestützte Auslese für eine Teststation zur Charakterisierung von Siliziumstreifendetektoren*

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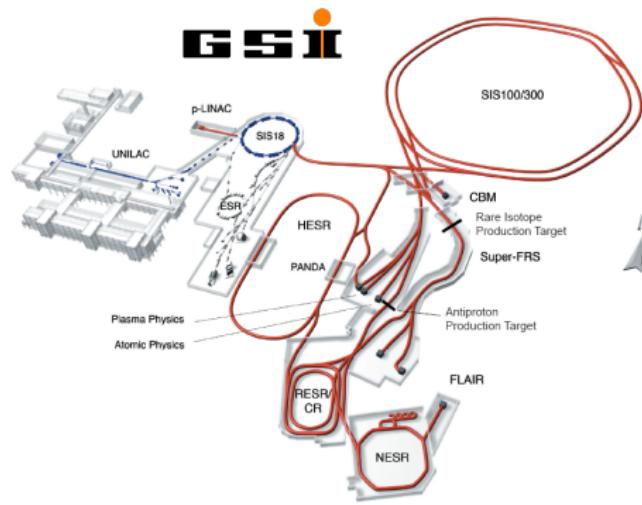
²Technische Universität Dresden, Institut für Kern- und Teilchenphysik

*Unterstützt vom BMBF und der EU



Motivation

PANDA as one experiment at FAIR, GSI



Motivation

R.Schnell

Motivation

MVD

DTS

Readout
structure

Readout
hardware

Results

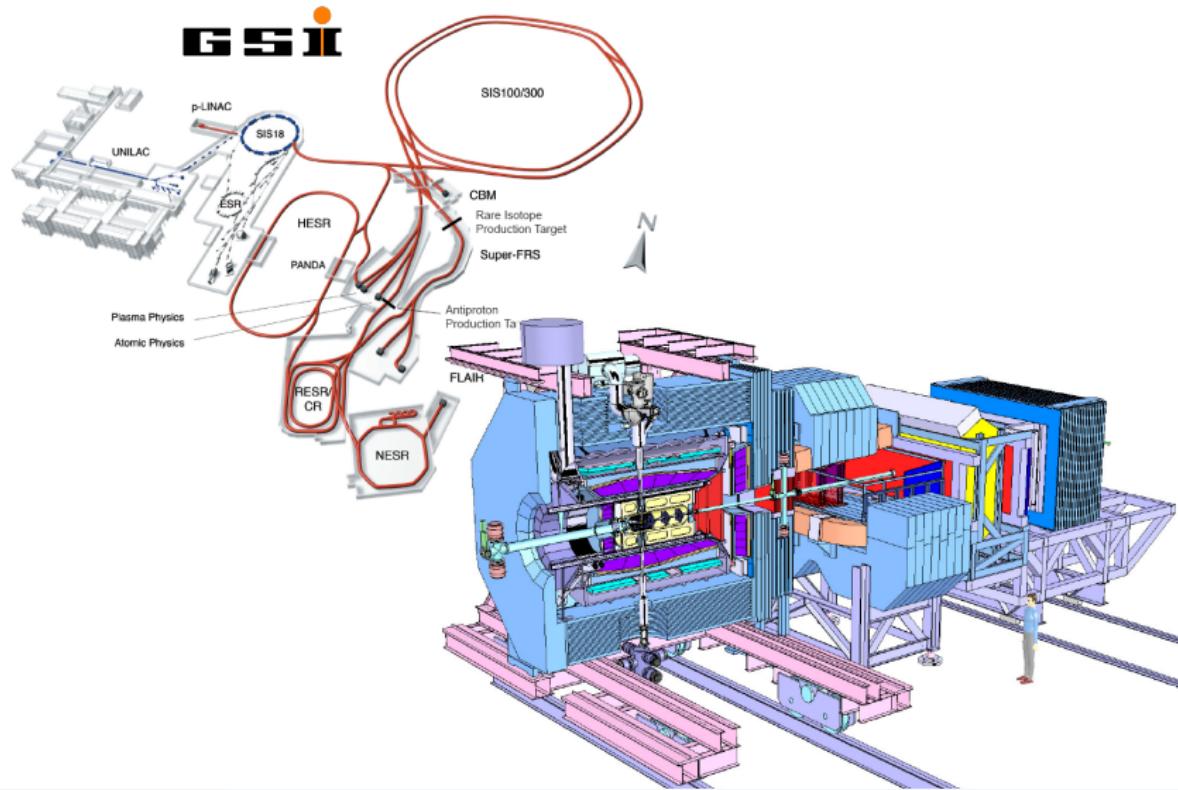
Data processing

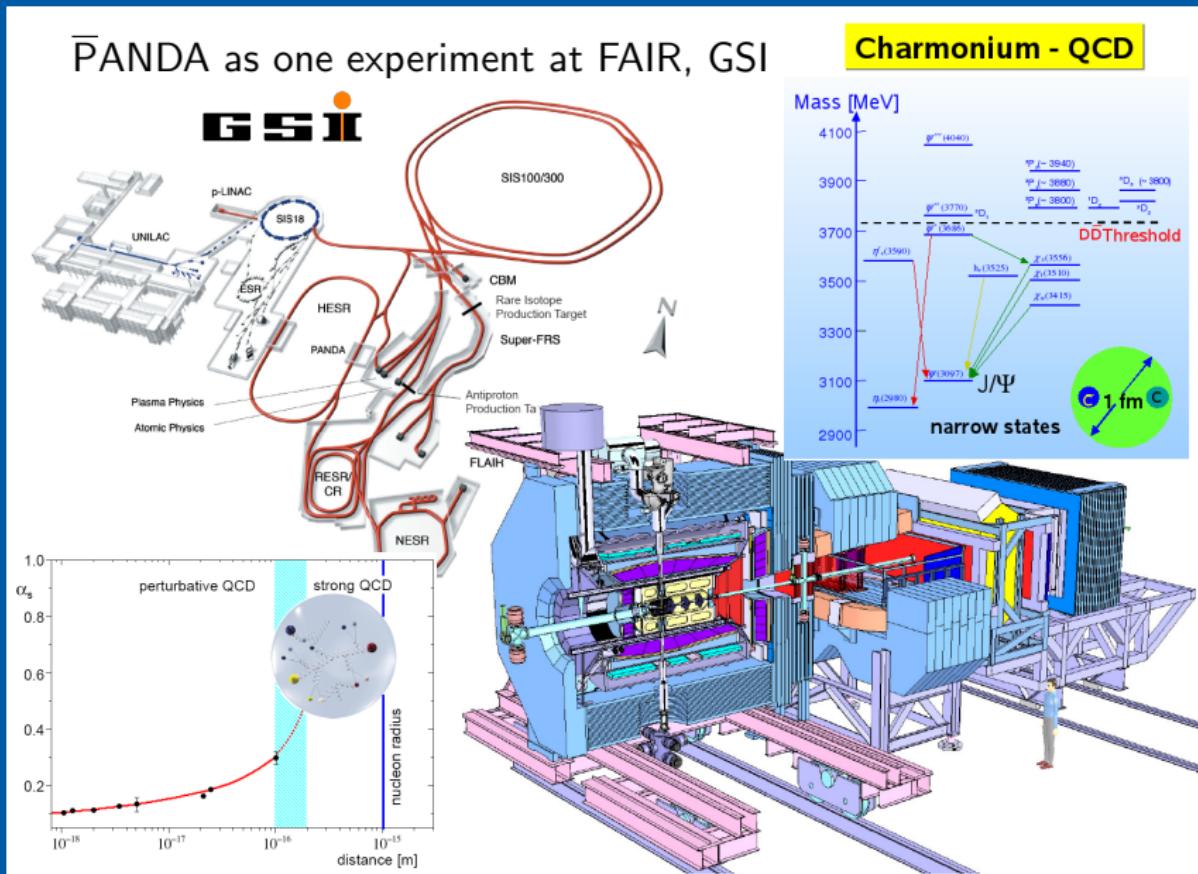
Hitfinder

Measurements

Summary

PANDA as one experiment at FAIR, GSI





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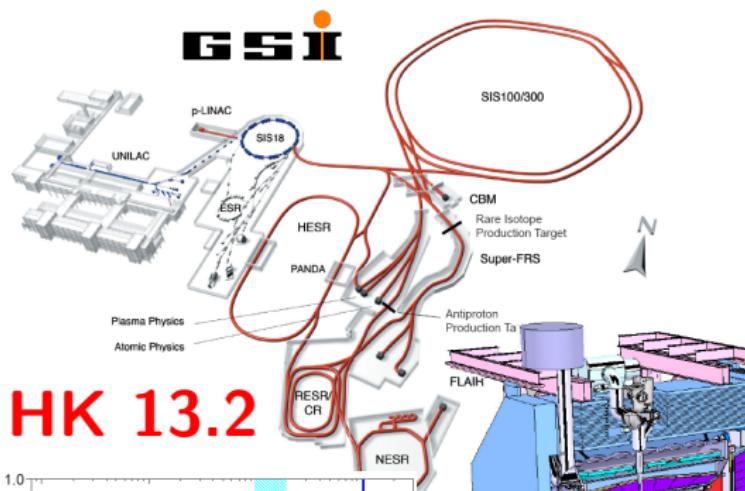
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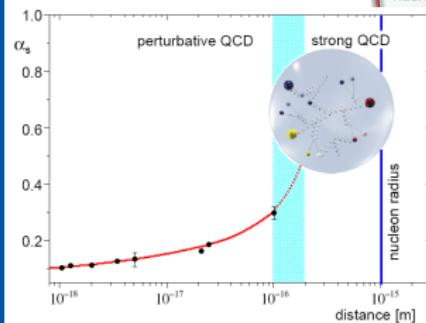
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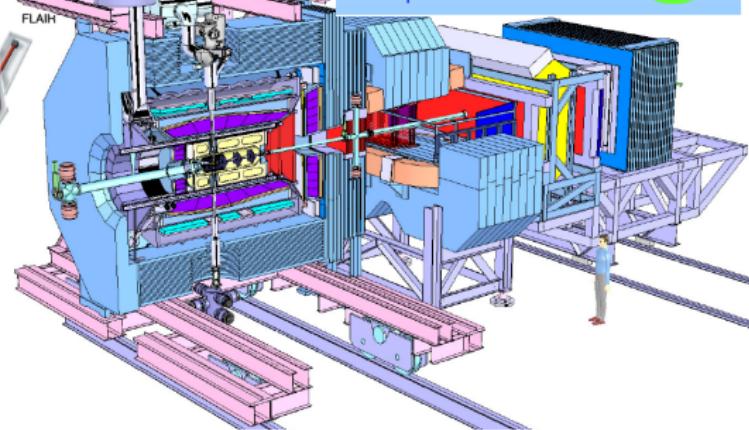
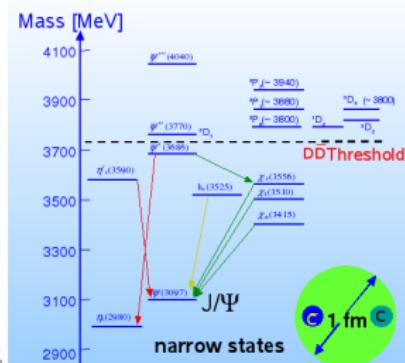
$\bar{\text{P}}\text{ANDA}$ as one experiment at FAIR, GSI



HK 13.2



Charmonium - QCD



The Micro-Vertex-Detector

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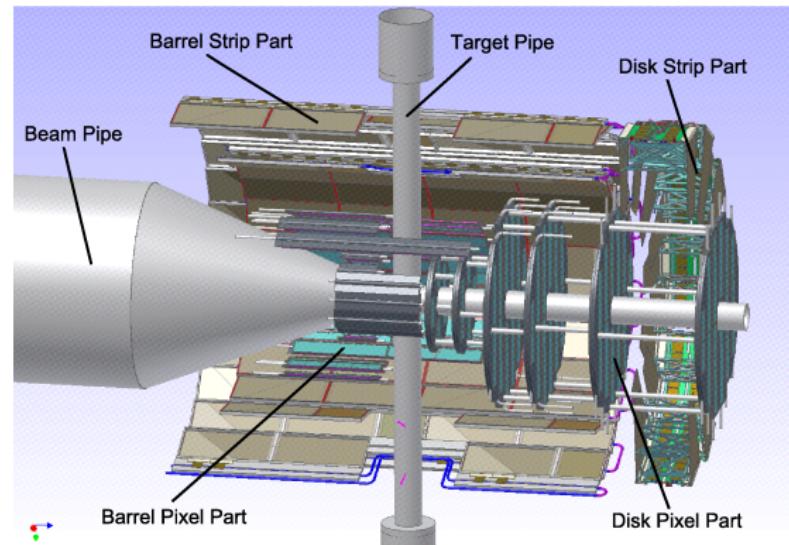
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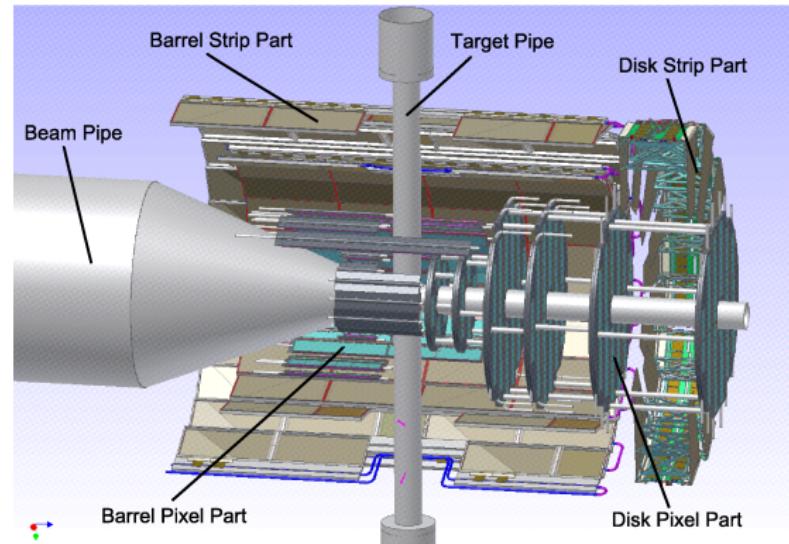
- pixel part
 - pixel size $(100 \cdot 100) \mu\text{m}^2$
 - 12,000,000 channels
- strip part
 - strip pitch: barrel 130 μm , 90°; disk 70 μm , 15°
 - 200,000 channels



The Micro-Vertex-Detector

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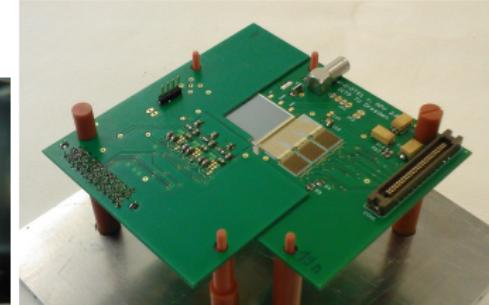
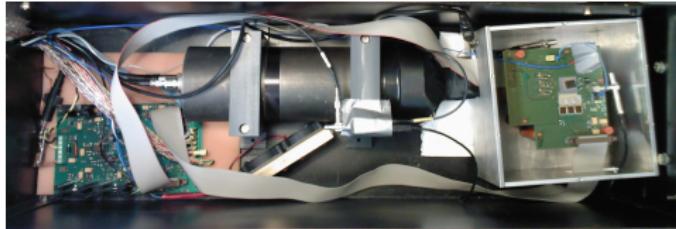
HK 21.1



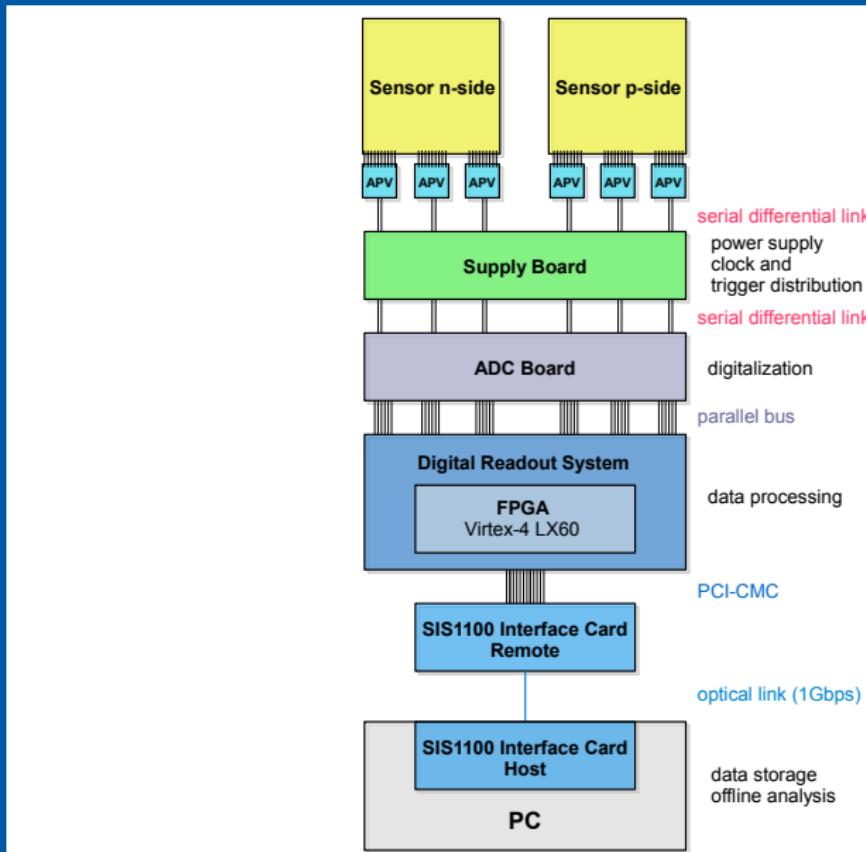
The Dresden Test Station

currently utilized components:

- Frontend APV25
- double-sided strip sensor, 50 μm pitch, 90° stereo angle



Readout structure



custom ADC card

- ADC AD9238
 - 2 chn per ADC
 - 6 chn in total
 - 12 bit resolution
 - differential inputs
 - parallel outputs
 - max. 65 MSPS
 - running @ APV clock



Readout hardware

New readout components 2

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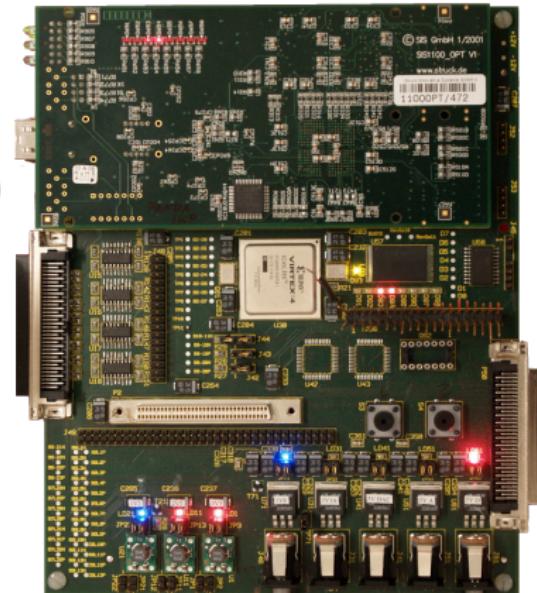
Results
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Hitfinder
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Summary

a versatile digital readout system for the PANDA MVD



- developed at ZEL
(FZ Jülich)
- FPGA: Xilinx Virtex-4 LX60
- 136 digital I/O's
- optical interface to PC via
SIS1100-OPT cards

- **MRF-MVD Readout
Framework**



Readout hardware

FPGA processes

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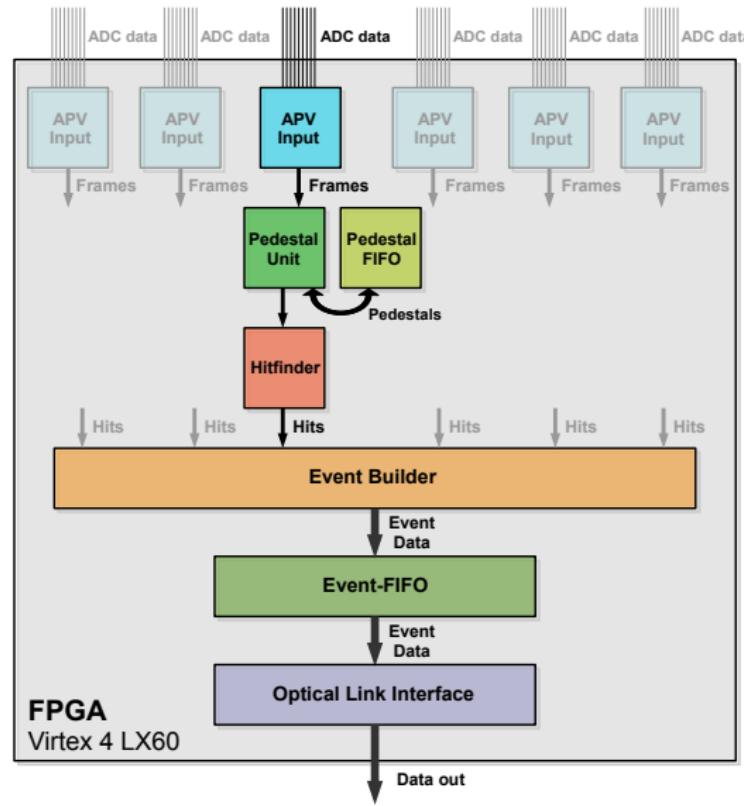
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Data processing

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Summary



Results

Frontend data

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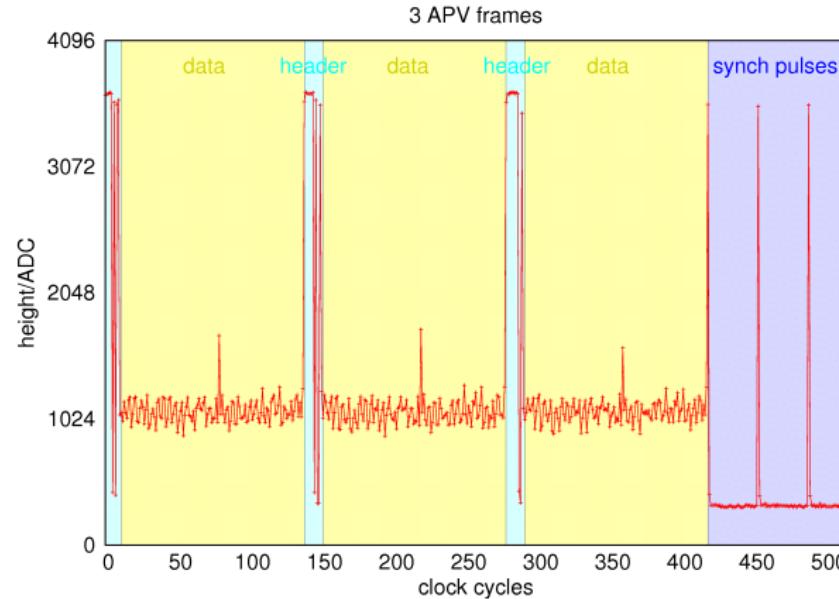
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Summary

- APV25 response on a single trigger
- APV in 3-Sample-Mode



- FPGA-readout triggered on header start condition

Results

Data processing

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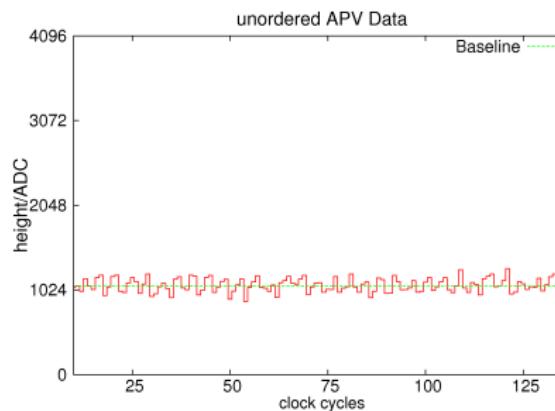
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Summary



Step 1: separation of data
and header

Results

Data processing

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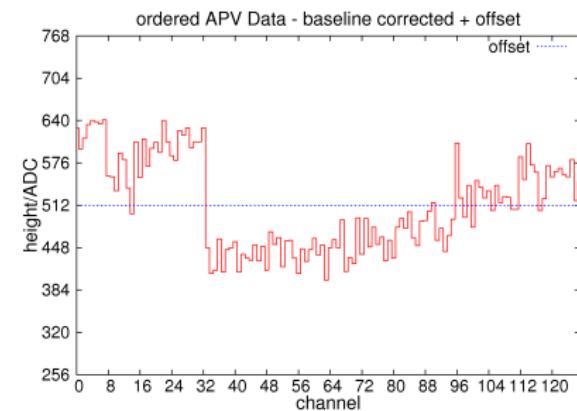
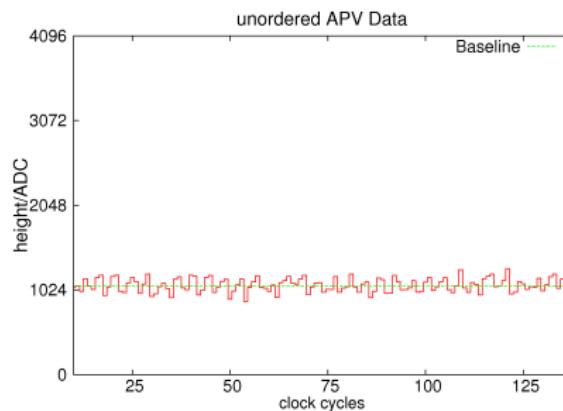
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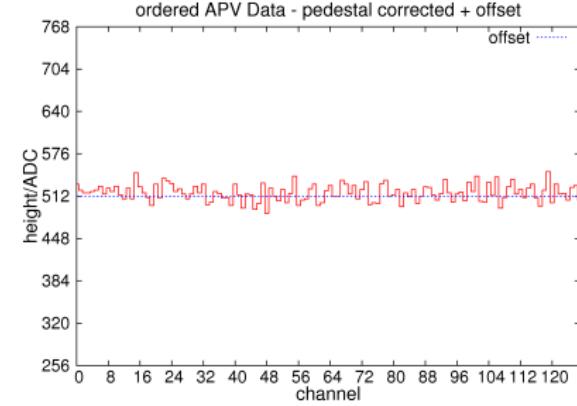
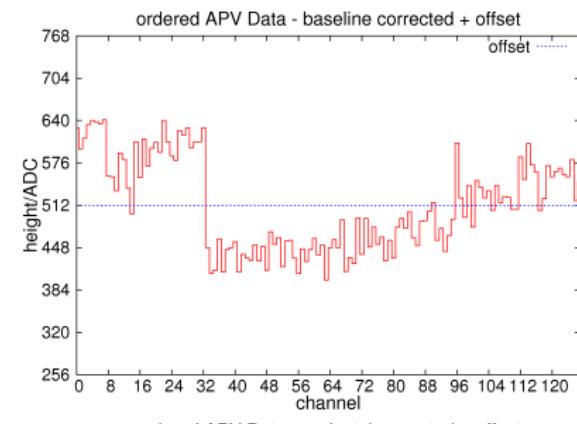
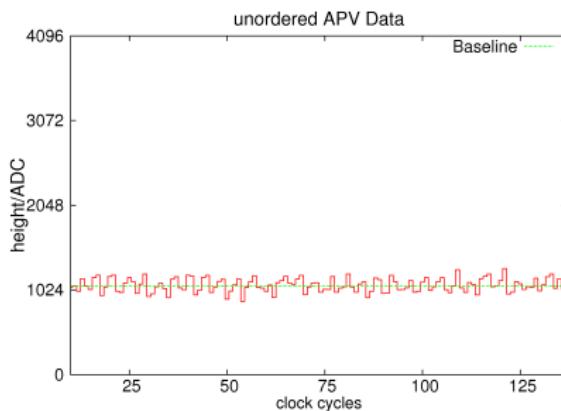


Step 1: separation of data
and header

Step 2: baseline correction

Results

Data processing



Step 1: separation of data
and header

Step 2: baseline correction

Step 3: pedestal correction

Results

Hitfinder

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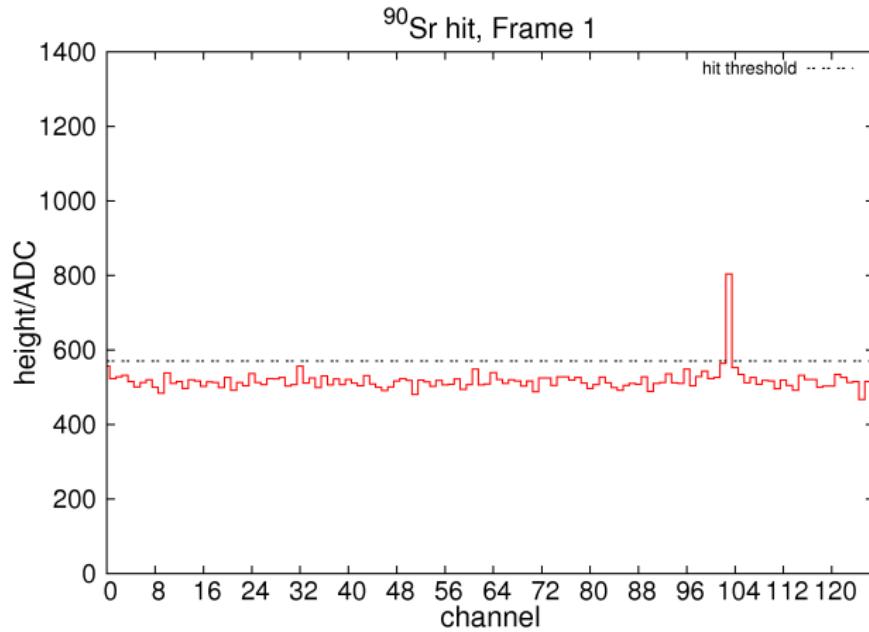
Data processing

Hitfinder

Measurements

Summary

- searches for hits
- hitfinder parameter: threshold, minimum length
- extraction of *maxHeight*, *Length* and *FrameID_begin*



Results

Hitfinder

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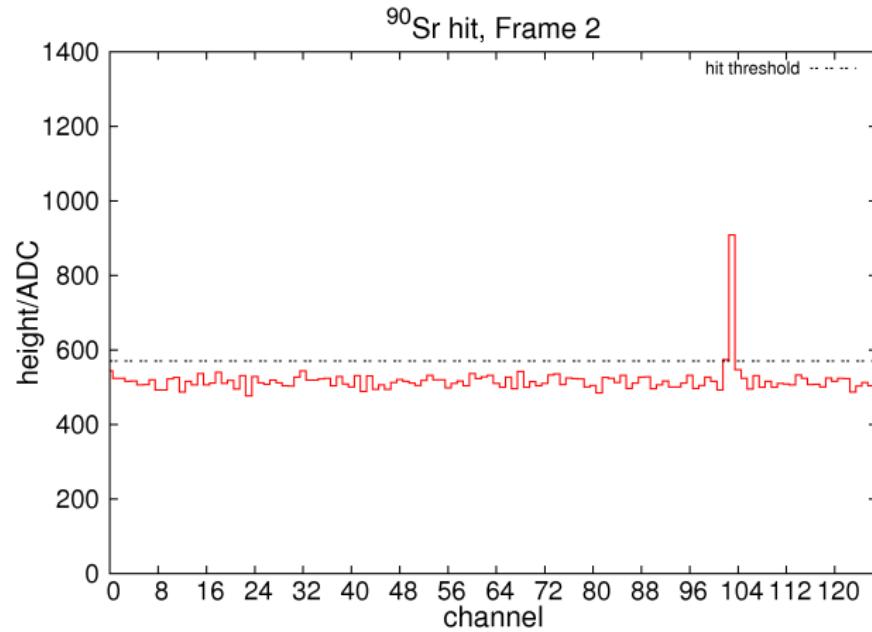
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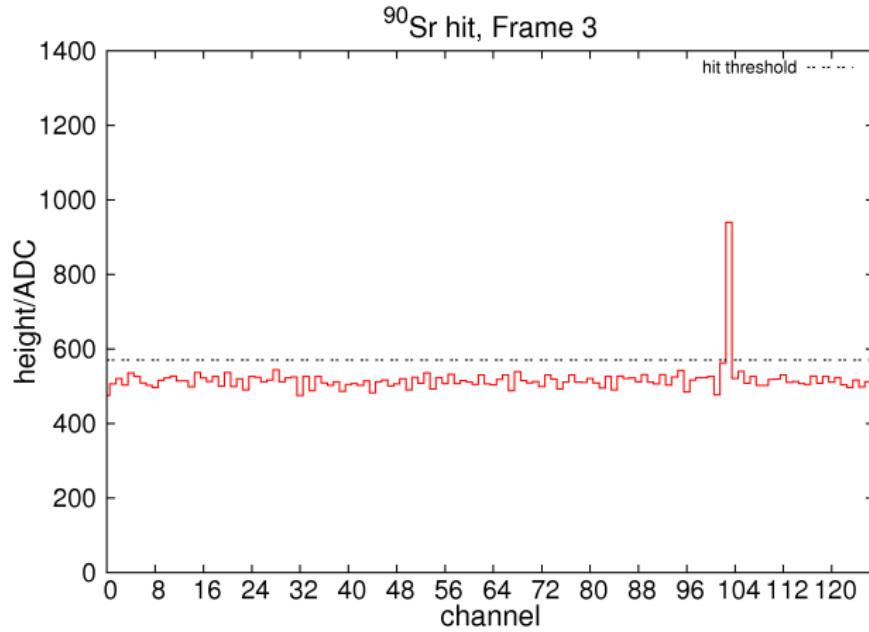
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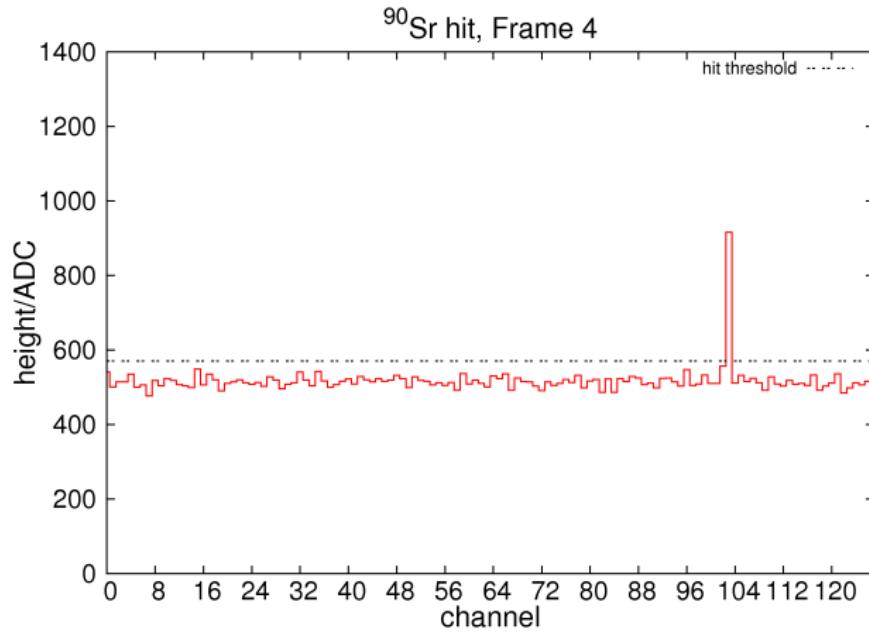
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Results

Data format / dead time

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Summary

- hit data format stored in Event-FIFO:

position	31	30...27	26...24	23...17	16...5	4...0
value	EventID	FrameID_begin	FEID	Channel	maxHeight	Length
length	1 bit	4 bit	3 bit	7 bit	12 bit	5 bit

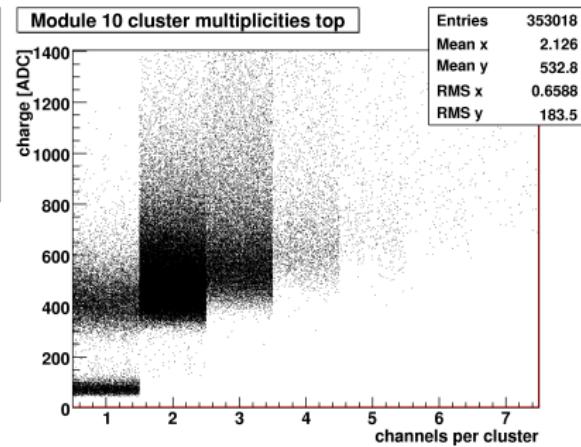
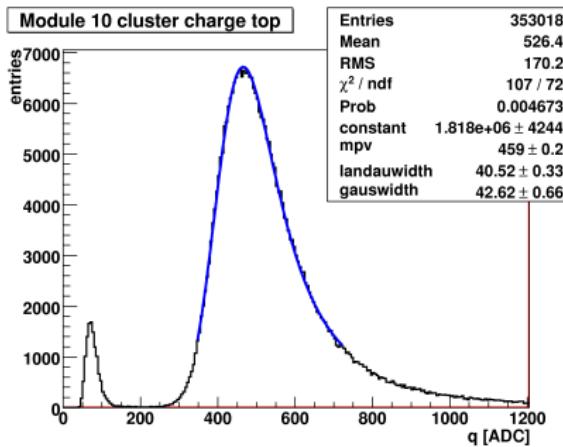
- dead time scales linear with number of requested frames:

# trigger	# frames	max. readout rate /kHz	dead time /clocks	dead time (@40 MHz) /μs
1	3	40,819	980	24,5
2	6	28,572	1400	35,0
3	9	21,978	1820	45,5
4	12	17,857	2240	56,0
5	15	15,038	2660	66,5

Results

Analyzed data

- electrons from a ^{90}Sr source
- energy loss distribution and hit multiplicity:



Results

2D imaging

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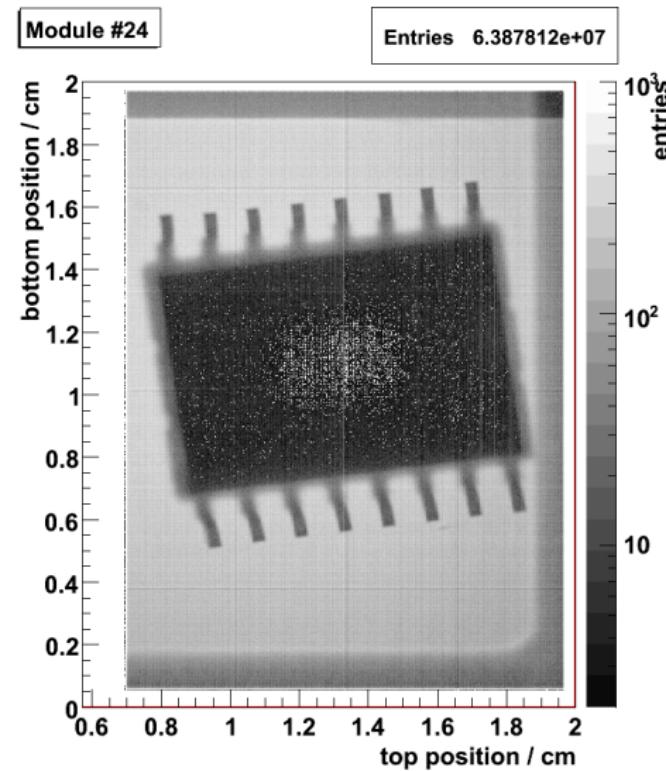
Results

Data processing
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Measurements

Summary

- SMD device placed on the sensor
- acts as an absorber for electrons from a ^{90}Sr source



Summary

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Summary

- Test Station for double-sided silicon strip sensors
- demonstrated a powerful FPGA based readout for APV25 frontends
- implemented online feature extraction

Thank you for your attention

HK 13.2

HK 21.1