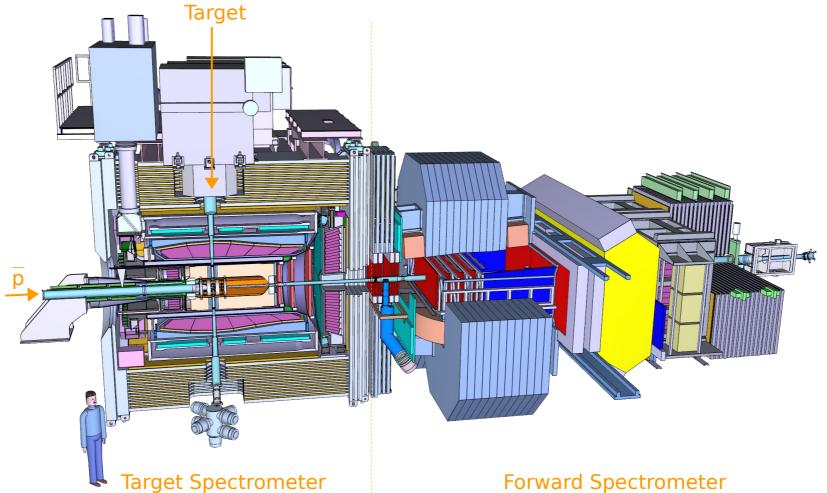
#### Characterization of the Strip Front-End ASIC of the PANDA MVD with the JDRS

18.03.2019 | DPG SPRING MEETING, ALESSANDRA LAI

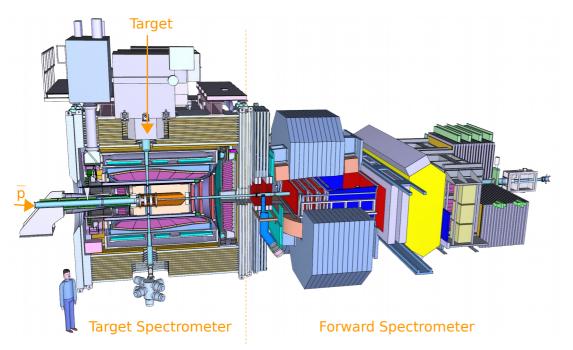




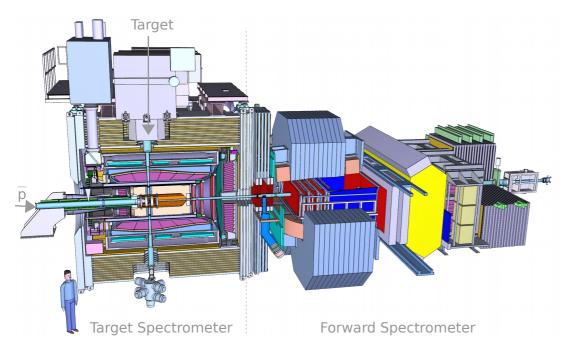
- Cooled  $\overline{p}$  beam @HESR
  - 1.5 GeV/c
  - $-\Delta p/p < 10^{-4}$

#### Forward Spectrometer

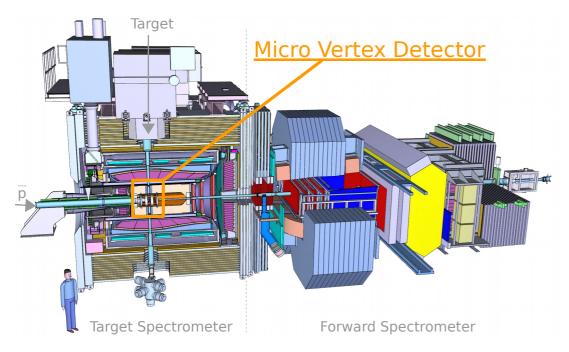
- Study strong interaction
  - Multi-s and c hadron spectroscopy
  - Exotic states
  - Nucleon structure
  - pA collisions



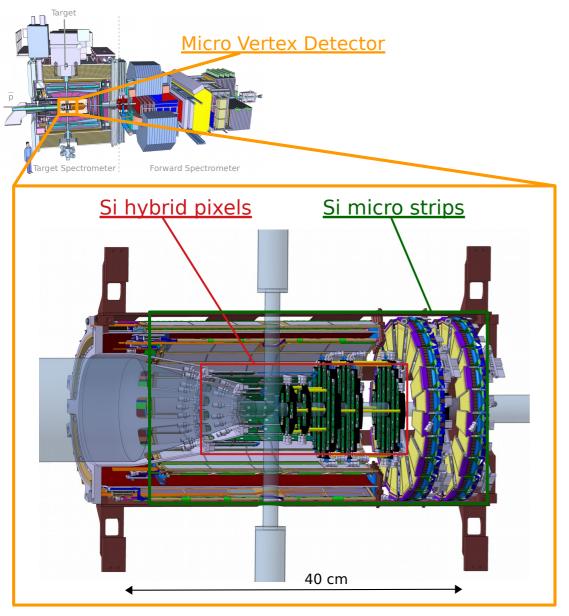
- Cooled antiproton beam @HESR
  - 1.5 GeV/c < p < 15 GeV/c
  - $-\Delta p/p < 10^{-4}$
- Study strong interaction
  - Multi-s and c hadron spectroscopy
  - Exotic states
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  - $\overline{p}A$  collisions



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  - Exotic states
  - Nucleon structure
  - $\overline{p}A$  collisions
- → Precise event timing
- $\rightarrow$  Charged particles tracking
  - primary and displaced vertices

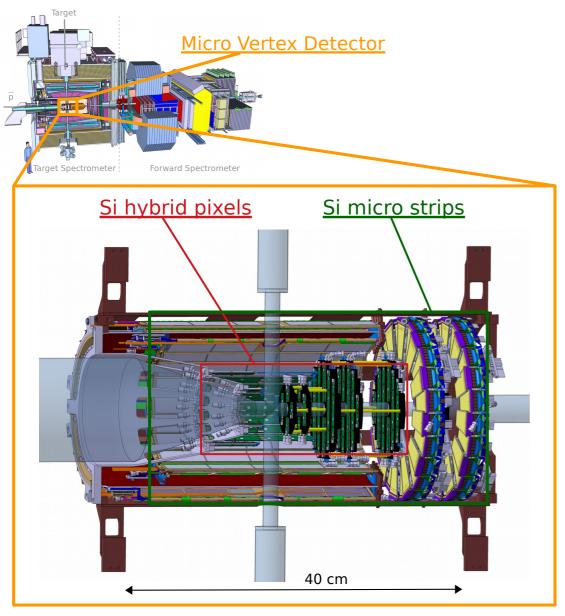


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  - 1.5 GeV/c < p < 15 GeV/c
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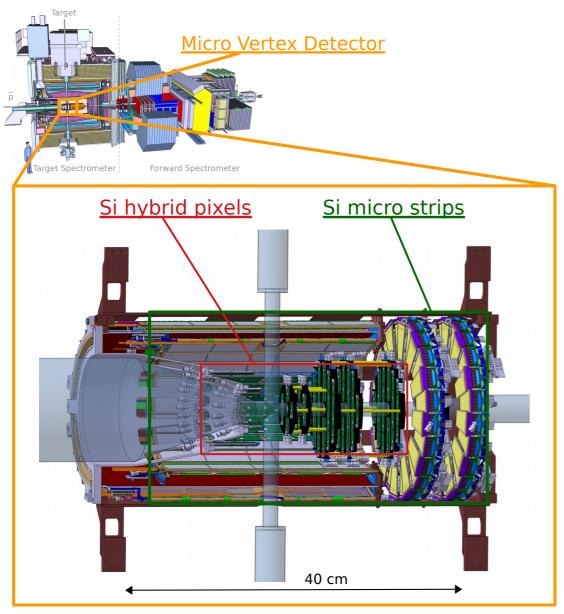
- Spatial resolution < 100  $\mu m$
- Time resolution < 10 ns
- Continuous readout



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Custom front-end chips
→ ToPix, PASTA

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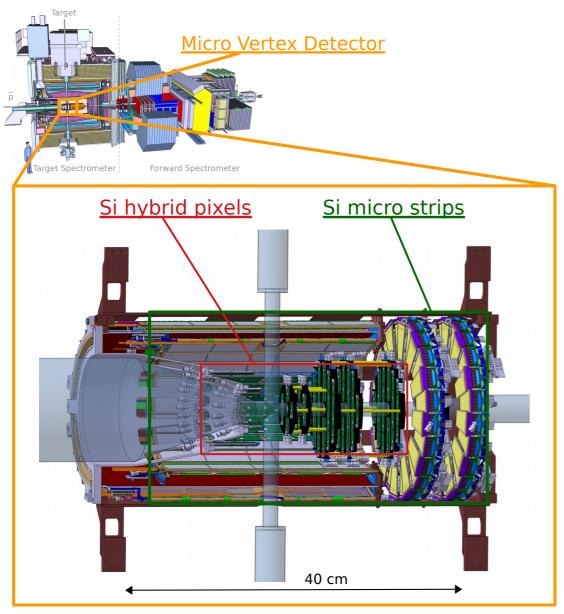


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Versatile data acquisition system for the different front-end prototypes



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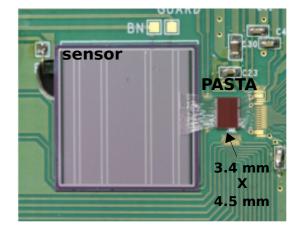
Custom front-end chips
→ ToPix, PASTA

Versatile data acquisition system for the different front-end prototypes Jülich Digital Readout System

#### PASTA

- Time-over-threshold: time + charge measurement
  - low threshold: leading edge time stamp
  - high threshold: deposited charge

Self trigger capability	
Number of channels	64
Frequency	160 MHz
Time resolution	6.25 ns

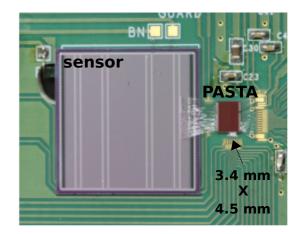


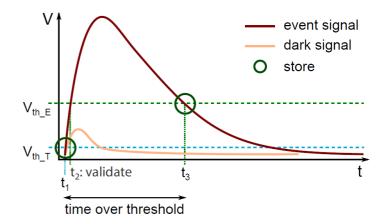
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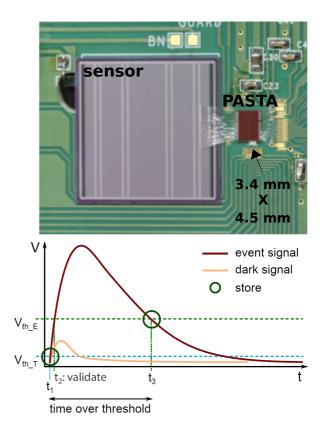




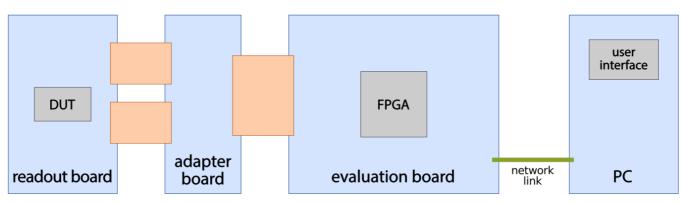
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160 MHz
6.25 ns



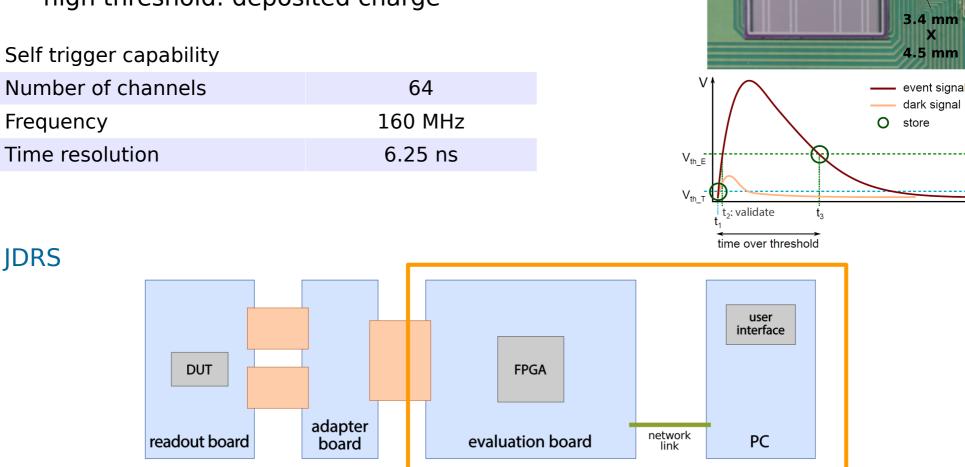
#### JDRS



- Data flow
  - Encoded event data in PASTA
  - First processing and storing in FPGA register
  - Transfer to PC and further processing

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ΒN

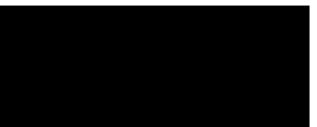
PAST

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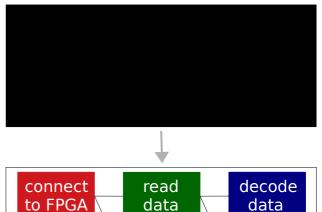
sensor

- Former version of JDRS (ToPix)
  - Lack of modularity and flexibility

Former version of JDRS (ToPix)
Lack of modularity and flexibility



- Former version of JDRS (ToPix)
  - Lack of modularity and flexibility
- Restructuring of the code
  - Use multiple interconnected modules
  - Separate reusable modules from ASIC specific



send

data

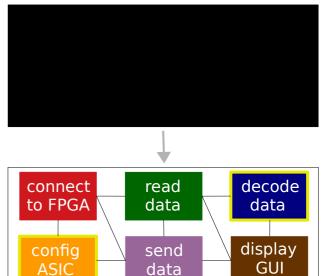
config

ASIC

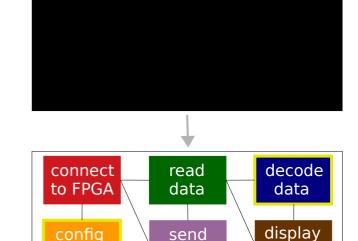
display

GUI

- Former version of JDRS (ToPix)
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  - Use multiple interconnected modules
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- Communication to and from PASTA
  - Configuration operations
  - Data collection and processing



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data

GUI

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ASIC

64 channels

	Item	Pos	Len	Min	Max	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	1
1	HCLDAC_e	28:32	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	(
2	HCLDAC_t	23:27	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	(
3	If	18:22	5	0	31	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	;
4	Iref_ratio_e	37:40	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	
5	Iref_ratio_t	33:36	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	
6	channel_en	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	
7	count_discarded_evt	13	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
8	count_local_SEU	16	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
9	count_missed_evt	14	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
10	count_noise_evt	12	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
11	count_refresh	15	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
12	count_valid_evt	11	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
13	finish_config	41	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
14	hit_validation	5	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
15	parallel_sync_FF	6	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
16	prediction_mode	4	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
17	stop_signal_delay	9:10	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
18	sync_chain_length	7:8	2	0	3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
19	test_mode_en	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
20	trigger_mode	2:3	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
21	use_delay_line	17	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

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parameters

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- Data collection and processing

	Item	Pos	Len	Min	Max	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
1	HCLDAC_e	28:32	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	HCLDAC_t	23:27	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	If	18:22	5	0	31	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
4	Iref_ratio_e	37:40	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
5	Iref_ratio_t	33:36	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
6	channel_en	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
7	count_discarded_evt	13	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	count_local_SEU	16	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	count_missed_evt	14	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	count_noise_evt	12	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	count_refresh	15	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	count_valid_evt	11	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	finish_config	41	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	hit_validation	5	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15	parallel_sync_FF	6	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	prediction_mode	4	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
17	stop_signal_delay	9:10	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	sync_chain_length	7:8	2	0	3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19	test_mode_en	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	trigger_mode	2:3	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	use_delay_line	17	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

#### 64 channels

to FPGA

config

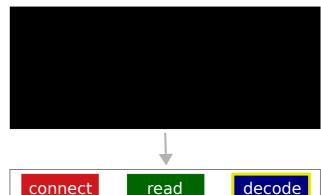
ASIC

More than 1000 parameters to tune

data

display

GUI



data

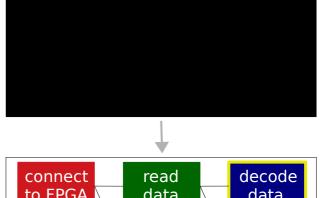
send

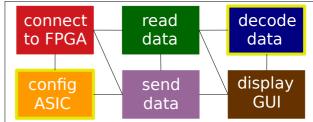
data

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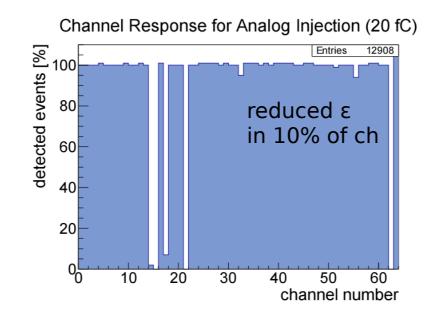
	Item	Pos	Len	Min	Max	0	1	2	3	4	5	6	7	8 9	10	11	12	13	14	15	16 1	7 1	B 19	9 20	21	22	23	24	25	
1	HCLDAC_e	28:32	5	0	31	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	More than 1000
2	HCLDAC_t	23:27	5	0	31	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
3	If	18:22	5	0	31	8	8	8	8	8	8	8 8	3 8	8	8	8	8	8	8	8	3 8	8	8	8	8	8	8	8	8	parameters to tu
4	Iref_ratio_e	37:40	4	0	15	10	0 10	10	10	10	10	10 1	10 1	0 1	0 10	10	10	10	10	10	10 1	0 1	0 10	0 10	10	10	10	10	10	
5	Iref_ratio_t	33:36	4	0	15	10	0 10	10	10	10	10	10	10 1	0 1	0 10	10	10	10	10	10	10 1	0 1	0 10	0 10	10	10	10	10	10	
6	channel_en	0	1	0	1	1	1	1	1	1	1	1 1	1 1	1	1	1	1	1	0	1	1 1	1	1	1	1	1	1	1	1	
7	count_discarded_evt	13	1	0	1	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
8	count_local_SEU	16	1	0	1	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
9	count_missed_evt	14	1	0	1	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
10	count_noise_evt	12	1	0	1	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	<b>.</b>
11	count_refresh	15	1	0	1	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	Automatic routin
12	count_valid_evt	11	1	0	1	1	1	1	1	1	1	1 1	1 1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	
13	finish_config	41	1	0	1	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
14	hit_validation	5	1	0	1	1	1	1	1	1	1	1 1	1 1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	
15	parallel_sync_FF	6	1	0	1	1	1	1	1	1	1	1 1	1 1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	
16	prediction_mode	4	1	0	1	1	1	1	1	1	1	1 1	1 1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	
17	stop_signal_delay	9:10	2	0	3	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
18	sync_chain_length	7:8	2	0	3	1	1	1	1	1	1	1 1	1 1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	
19	test_mode_en	1	1	0	1	0	0	0	0	0	0	0 (	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
20	trigger_mode	2:3	2	0	3	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	
21	use_delay_line	17	1	0	1	1	1	1	1	1	1	1 1	1 1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1	

64 channels

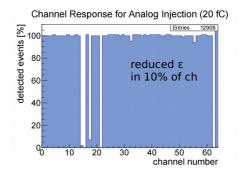


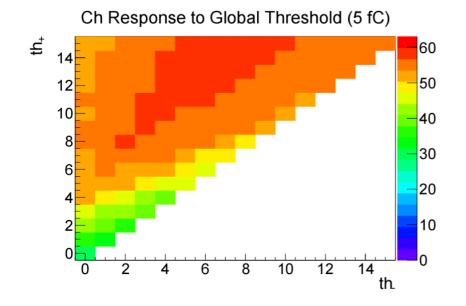


- Internal injection
  - Channel response

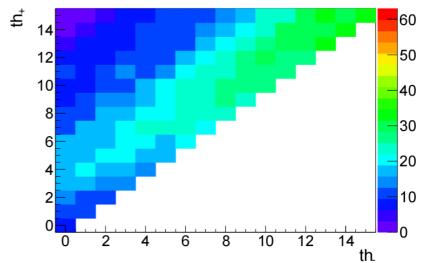


- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>1</sub>  $\ge$  0)

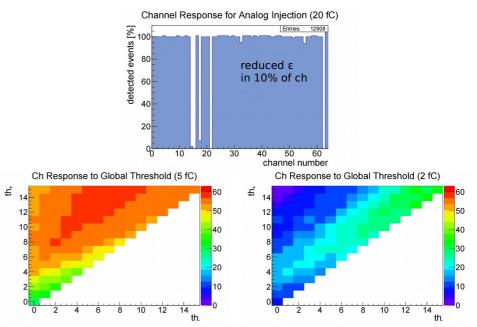


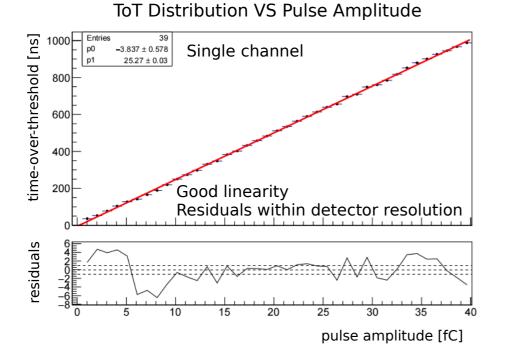


Ch Response to Global Threshold (2 fC)



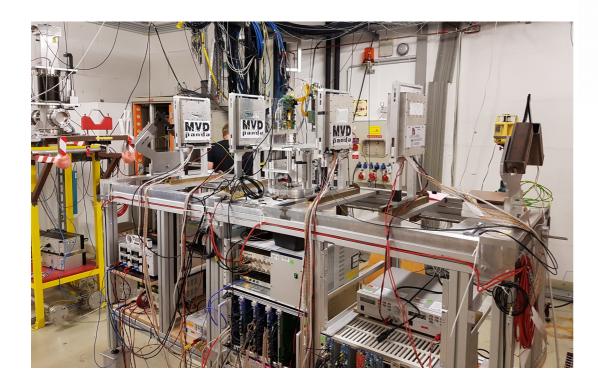
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>1</sub>  $\ge$  0)
  - Linearity of the front-end

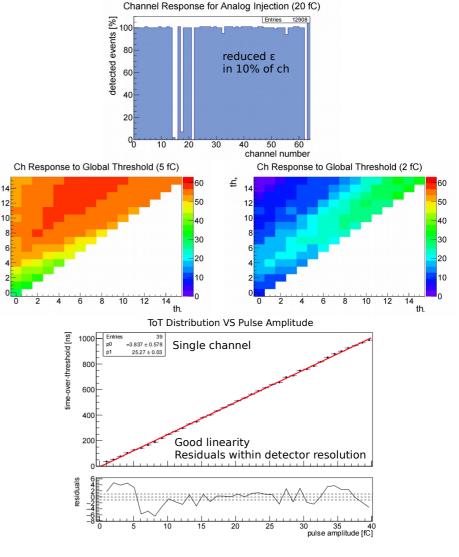




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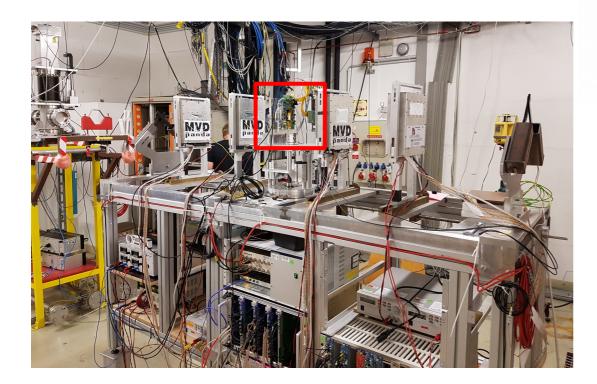
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam

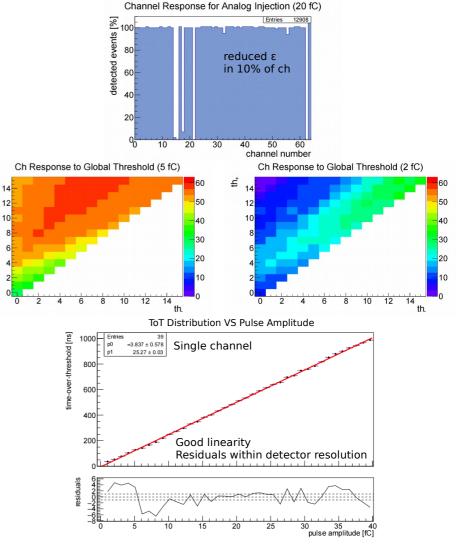




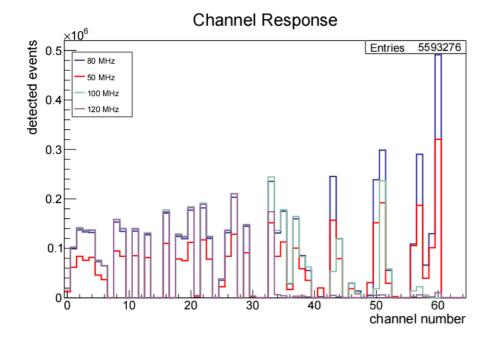
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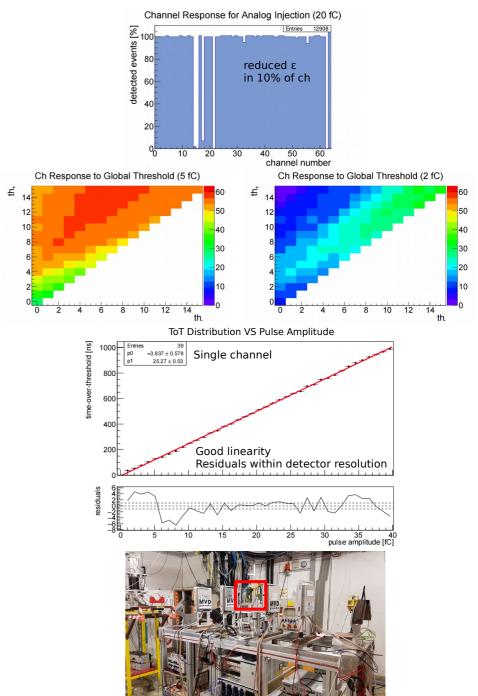
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam



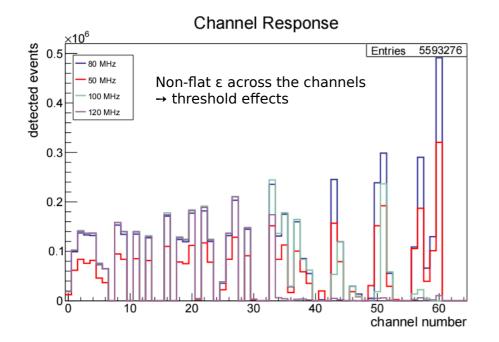


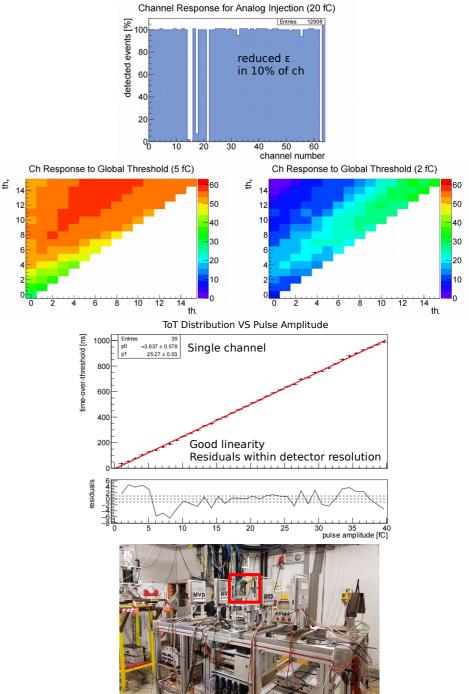
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response



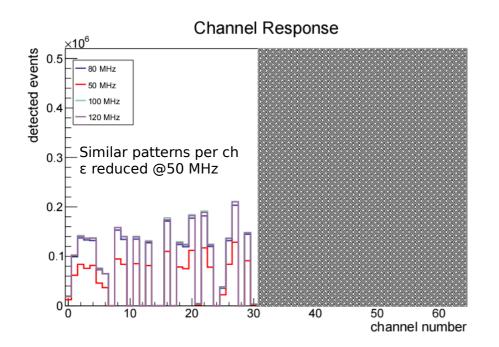


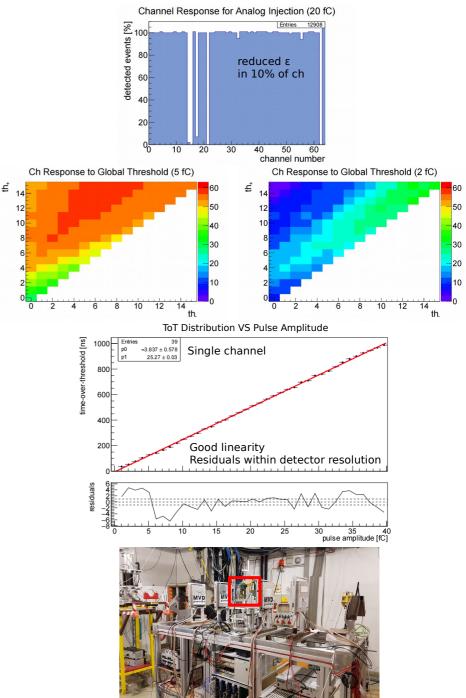
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub>-th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response





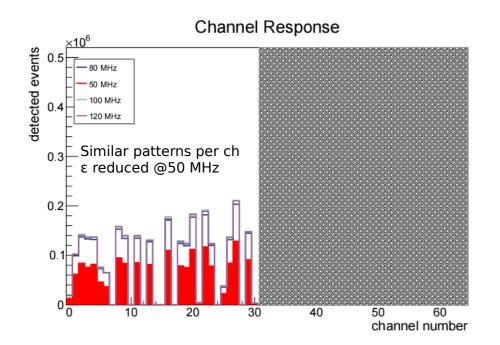
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response

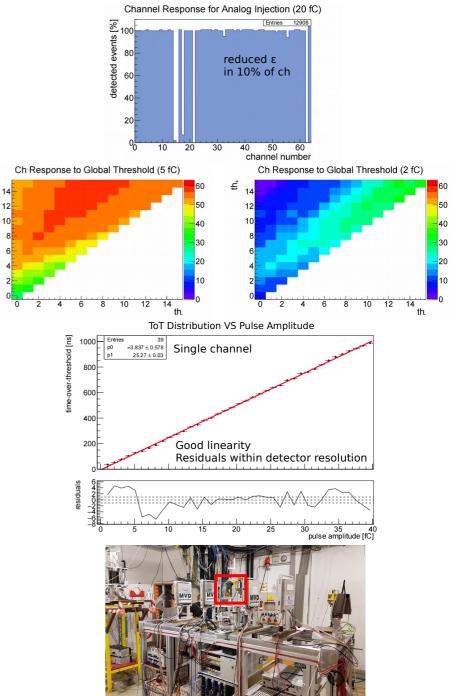




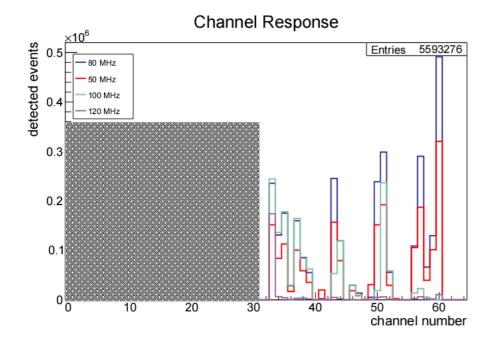
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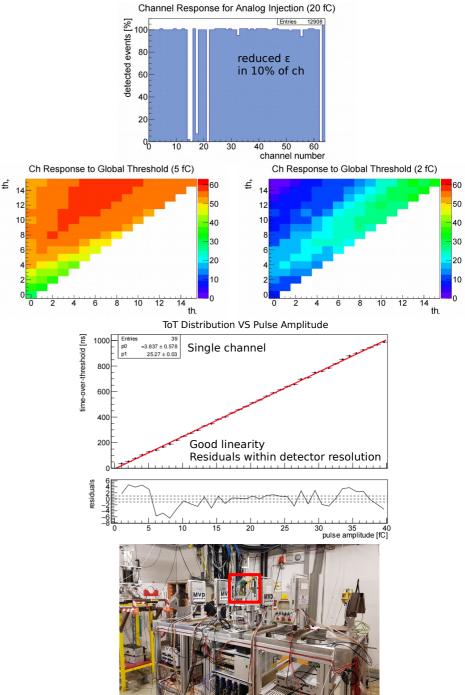
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th\_- th\_  $\geq 0$ )
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response



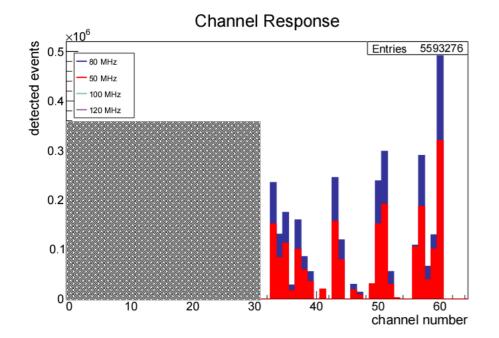


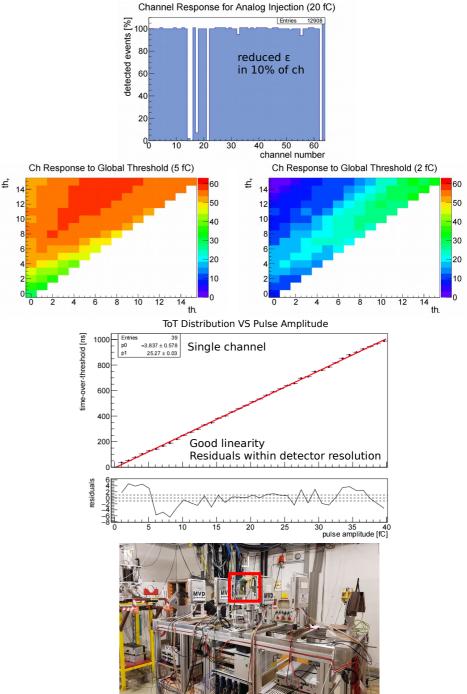
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response



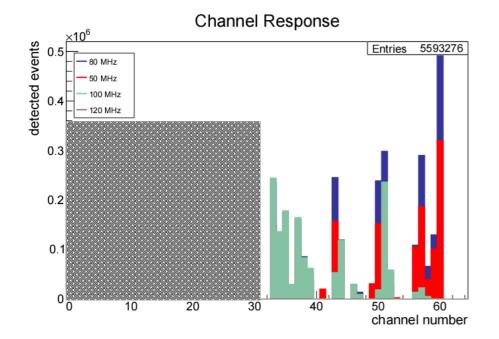


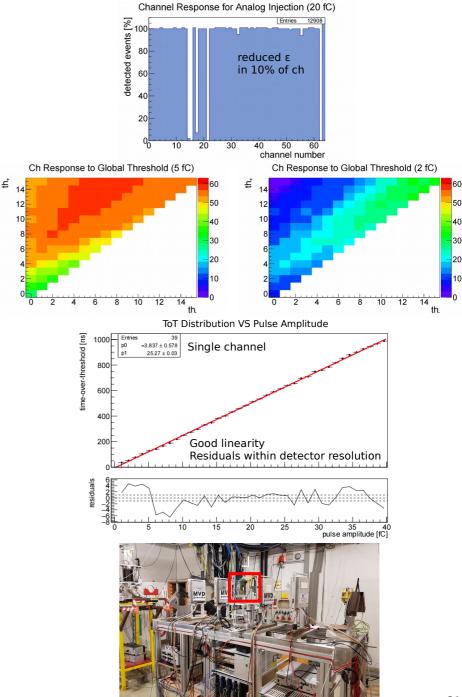
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th\_- th\_  $\geq 0$ )
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response



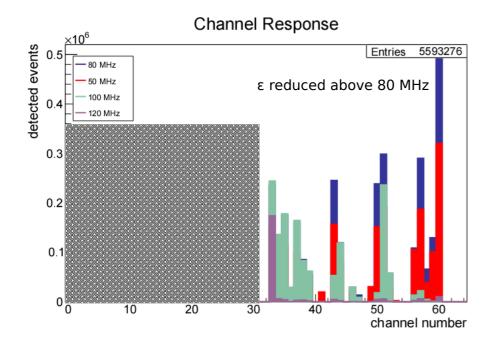


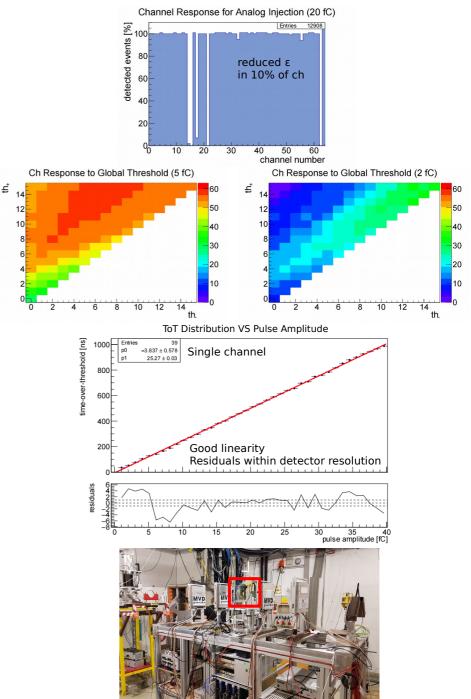
- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub>-th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response





- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th\_- th\_  $\geq 0$ )
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response





- Internal injection
  - Channel response
  - Threshold calibration
    - differential scheme (th<sub>1</sub> th<sub>2</sub>  $\ge$  0)
  - Linearity of the front-end
- Proton beam
  - Frequency-dependent response

<sup>∞</sup> 100 80 reduced *ε* in 10% of ch 60 40 10 20 30 40 50 60 channel number Ch Response to Global Threshold (5 fC) Ch Response to Global Threshold (2 fC) 12 10 12 14 ToT Distribution VS Pulse Amplitude Entries

Channel Response for Analog Injection (20 fC)

#### Data acquisition system

- Modular integration of PASTA in the JDRS
- User-friendly GUI

- Stable operation (incl. in-beam)

#### • PASTA

- Principle of operation verified
- Operation of individual channel
- Critical optimization of global settings
- Frequency-related issues
- Significant input for PASTA 2.0

