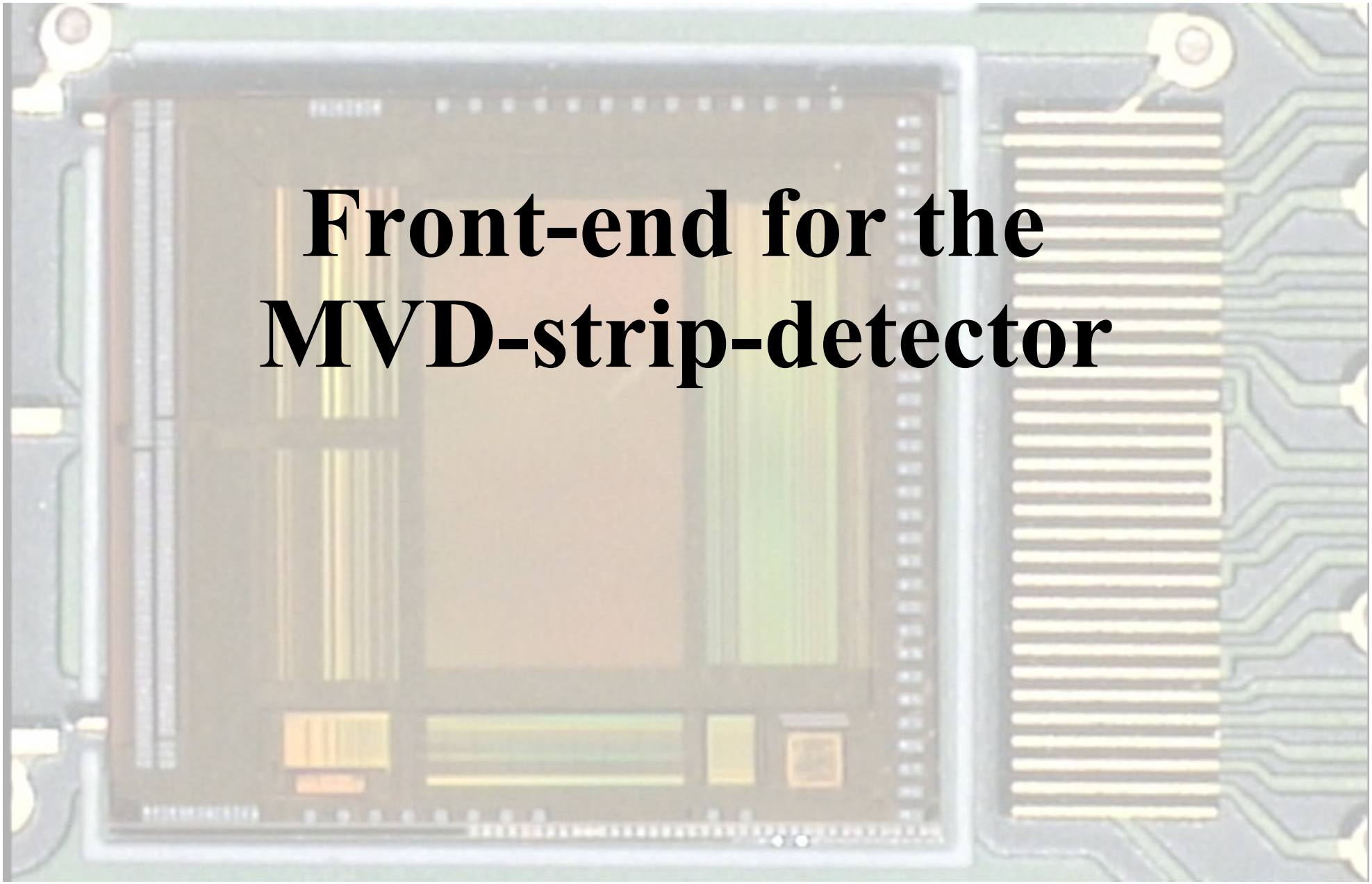


Front-end for the MVD-strip-detector

PANDA MVD Workshop Turin - May 23-25, 2011

Status

- no decision yet about front-end for the strip detector readout
- a mayor “loose end” of the strip part
- lack of adequate (final) option

Requirements

- PANDA specific requirements:
  - self triggering
  - precise time resolution
  - fully digital hit information

=> not many front-end types available to comply with these requirements

Options

- adapted ToPix3
- STS-XYTER
- (modified) FSSR2
- development by Marek Idzik et al.

Requirements

- will be discussed in PANDA-MVD note 6
- some parameters depend each other:
  - hit rate → dead time, data link, buffer
  - digitization resolution → point resolution, PID
  - time resolution → event building
  - power consumption → cooling
  - supply → cabling effort

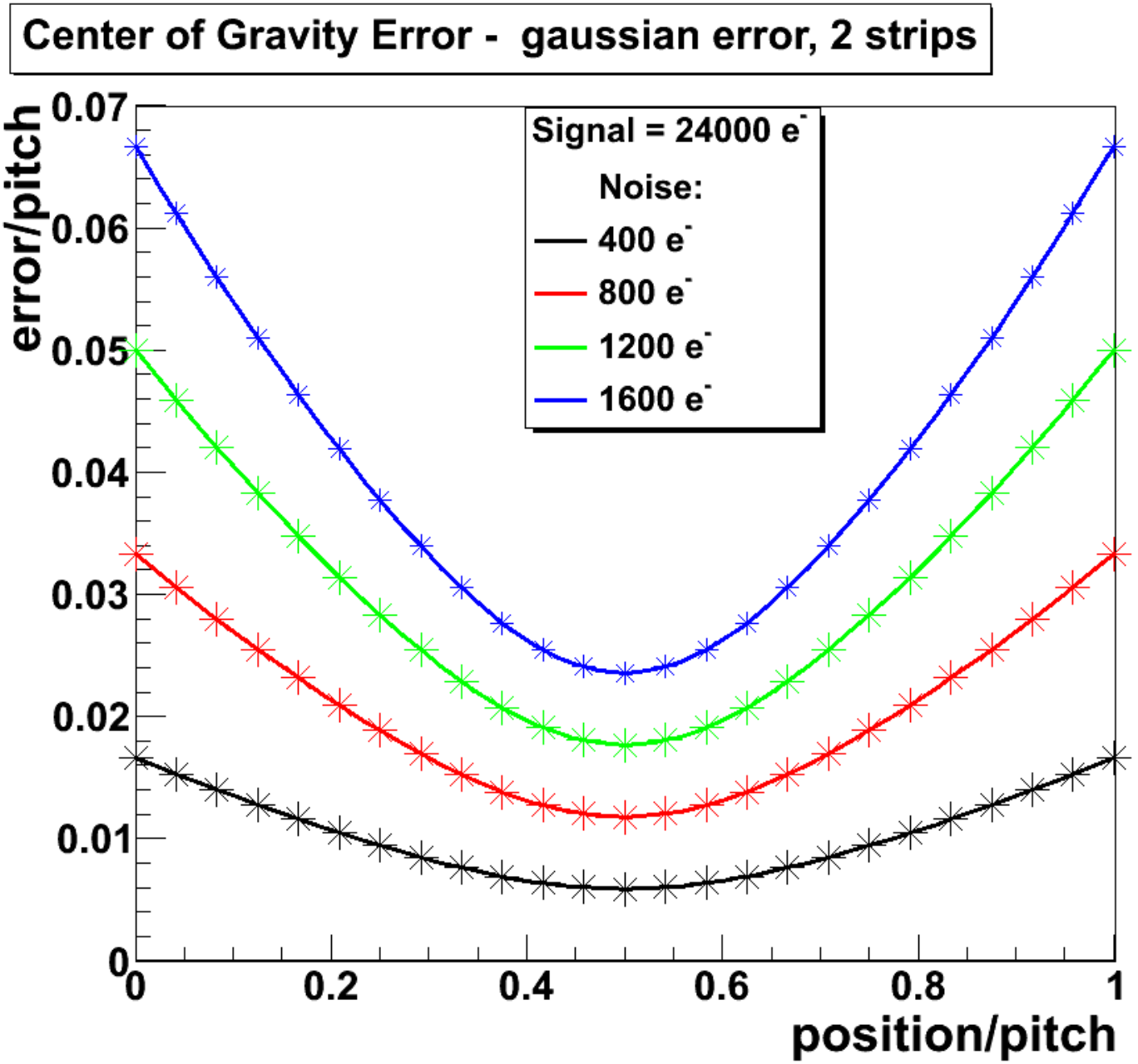
Requirements

- radiation hardness, SEU mitigation
  → technology
- detector capacitance → noise
- shaping time → noise, dead time
- linearity → energy resolution
- dimension, pad layout → stave layout

Digitization Resolution

- important parameter for:
  - spatial resolution through clustering
  - PID through energy loss measurement

→ spatial resolution limited by noise


Center of Gravity Error - gaussian error, 2 strips
Signal = 24000 e-
Noise:
400 e-
800 e-
1200 e-
1600 e-
error/pitch
position/pitch
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.2
0.4
0.6
0.8
1

Digitization Resolution

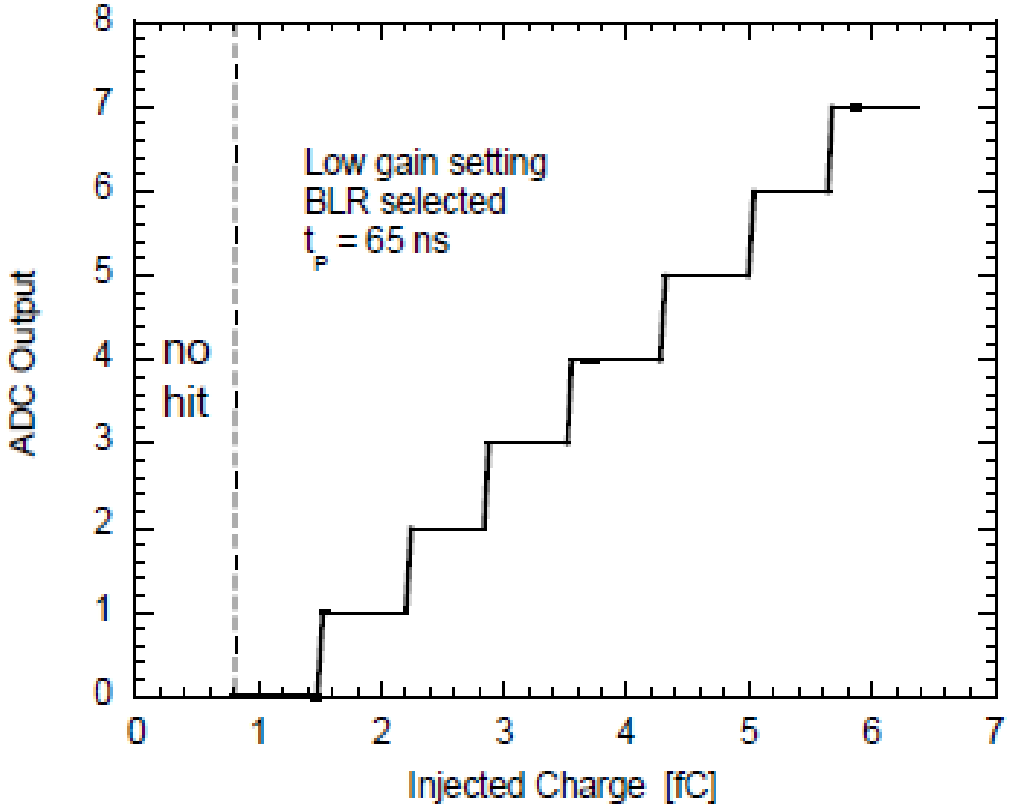
- central question:

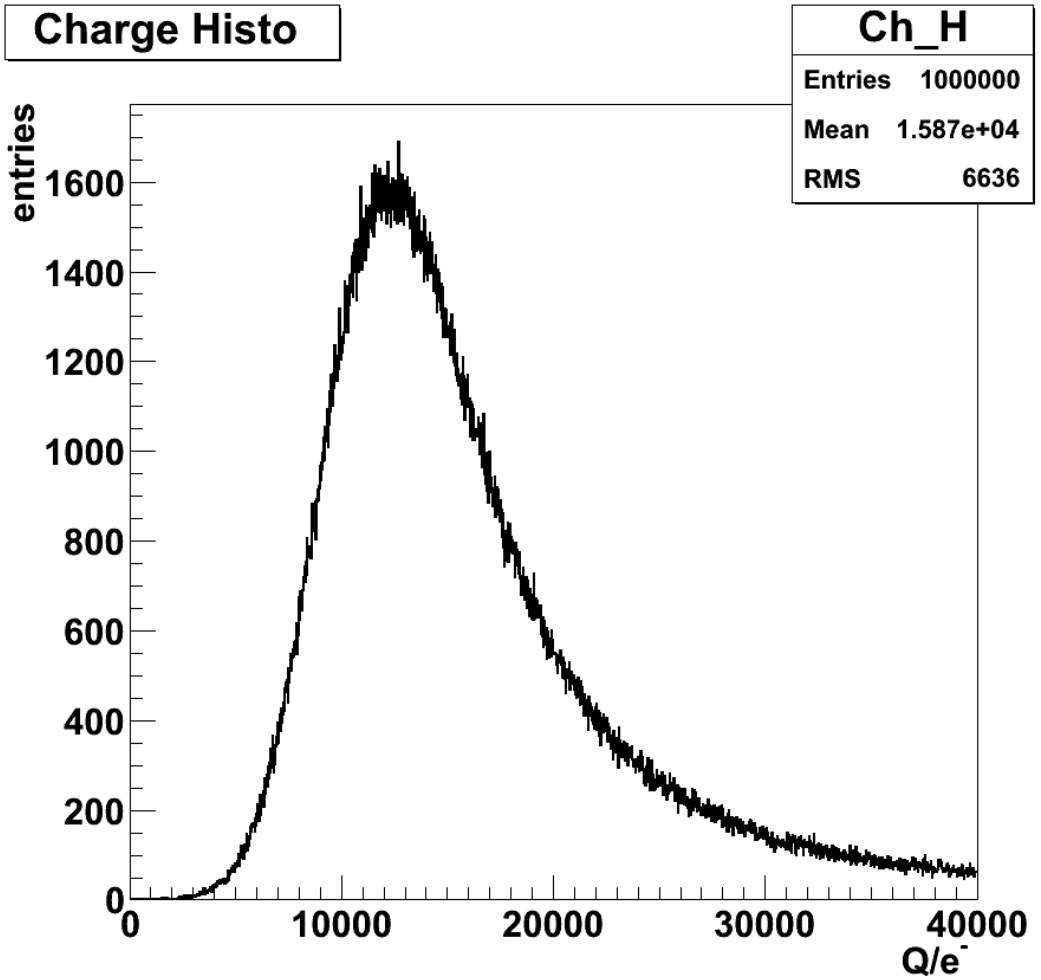
  How many bits of digitization resolution required?

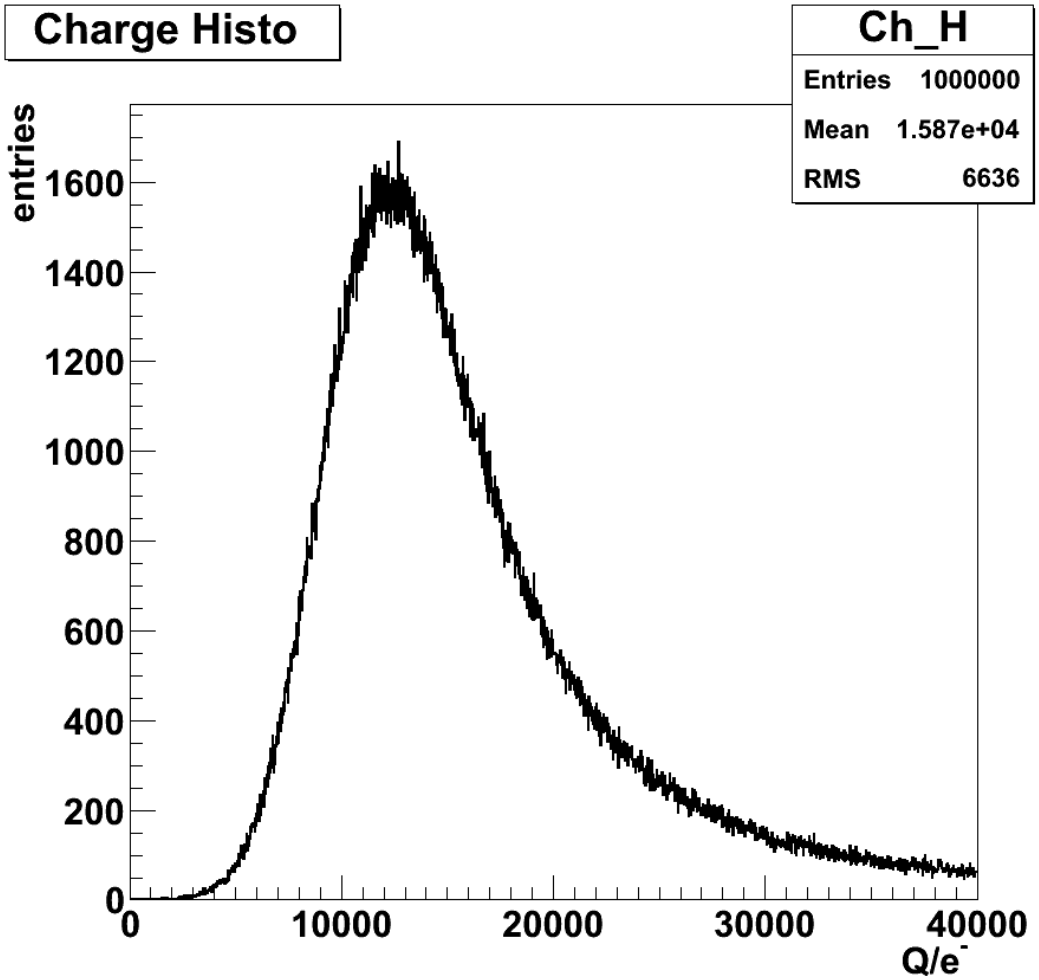
  - contributes to amount of data
  - provoke more power consumption

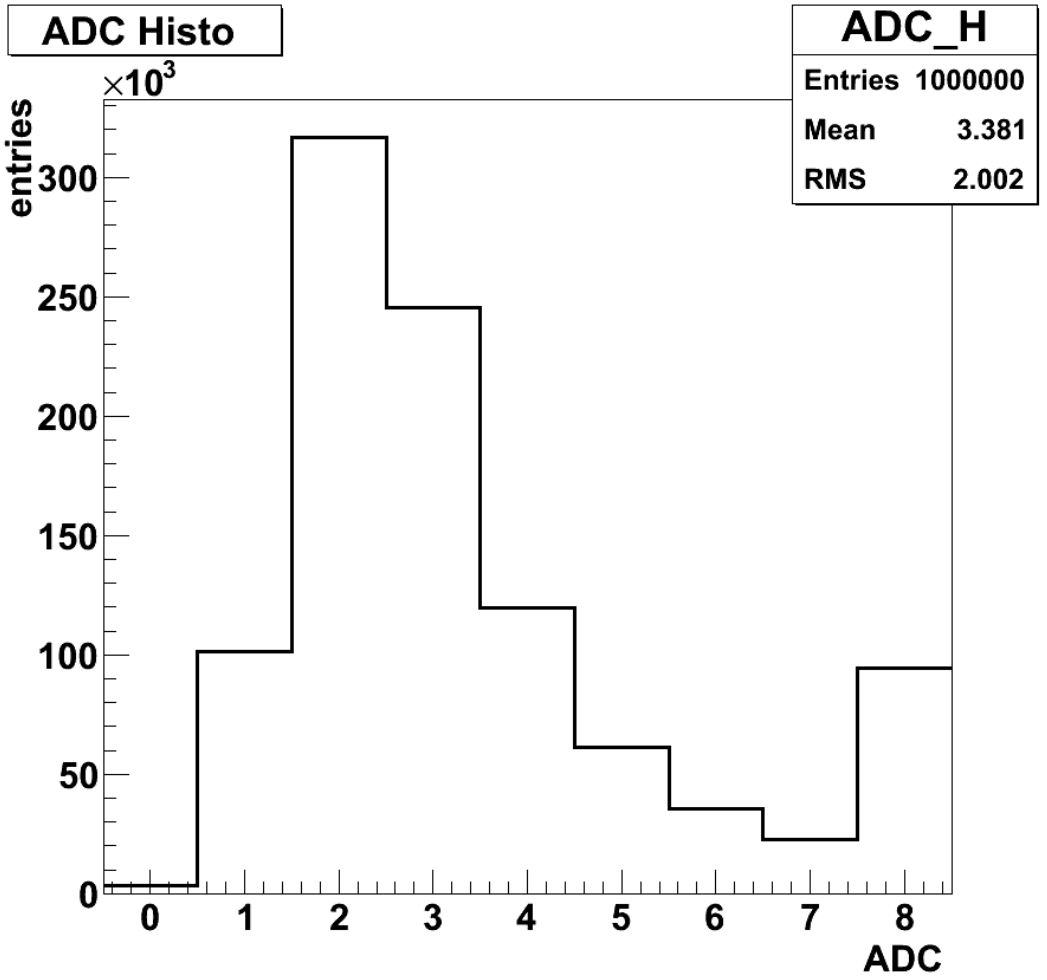
- Example: FSSR2 digitization centered around 1 MIP

(2005 IEEE Nuclear Science Symposium Conference Record)

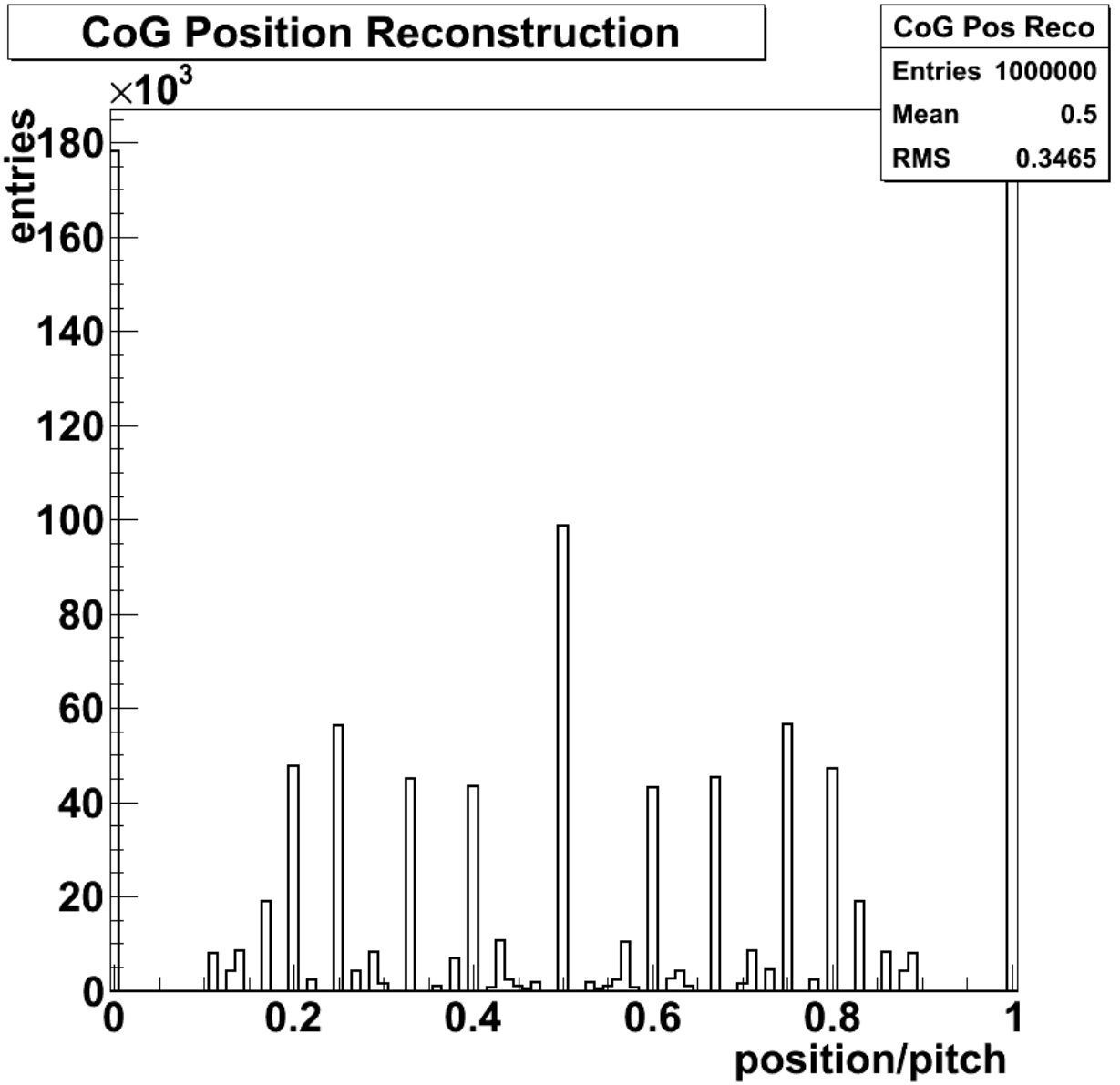



Charge Histo
Ch_H
Entries 1000000
Mean 1.587e+04
RMS 6636
entries
1600
1400
1200
1000
800
600
400
200
0
0
10000
20000
30000
40000
Q/e-

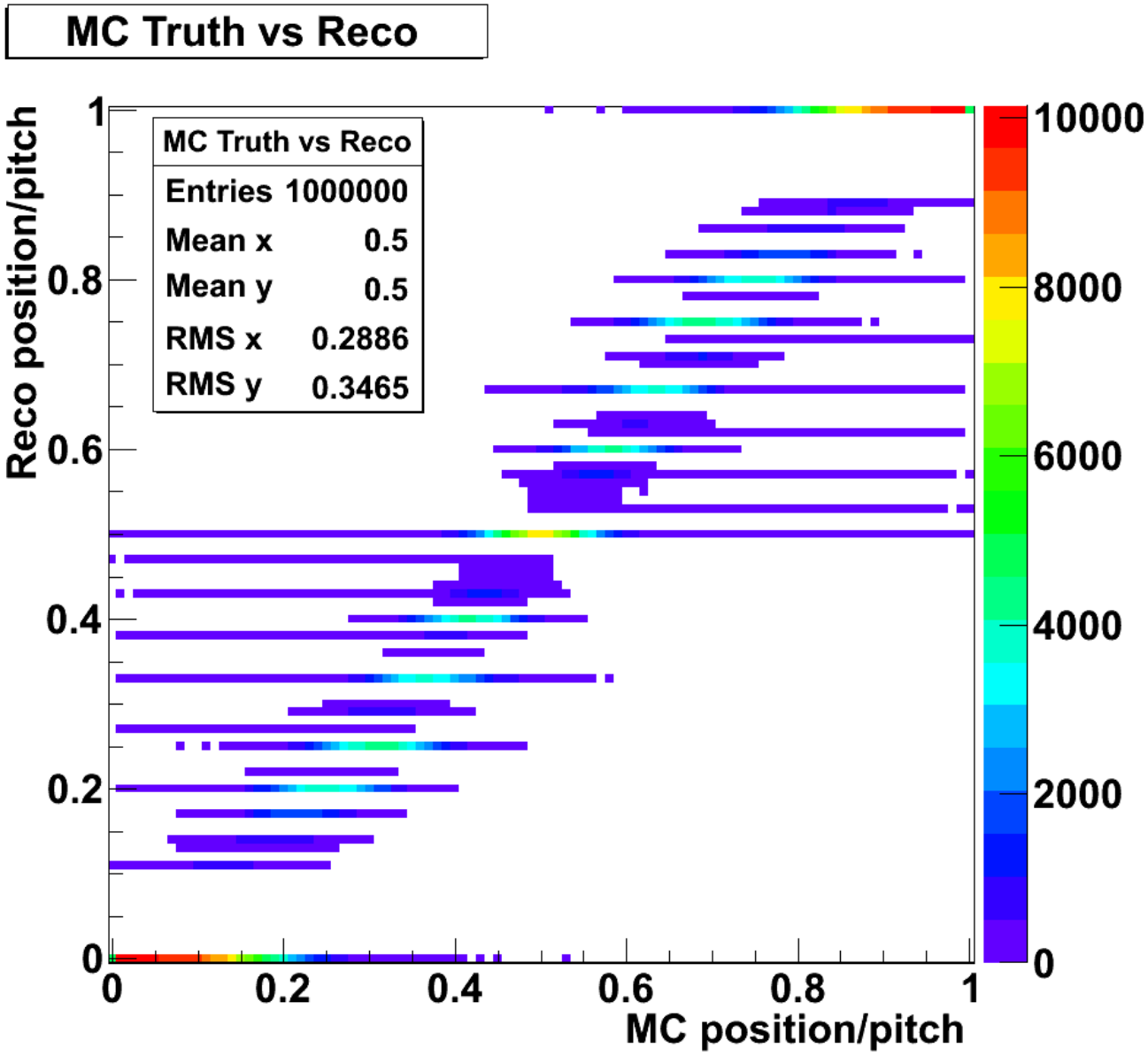

Charge Histo
Ch_H
Entries 1000000
Mean 1.587e+04
RMS 6636
entries
1600
1400
1200
1000
800
600
400
200
0
0
10000
20000
30000
40000
Q/e-


ADC Histo
ADC_H
Entries 1000000
Mean 3.381
RMS 2.002
×10^3
entries
300
250
200
150
100
50
0
0
1
2
3
4
5
6
7
8
ADC

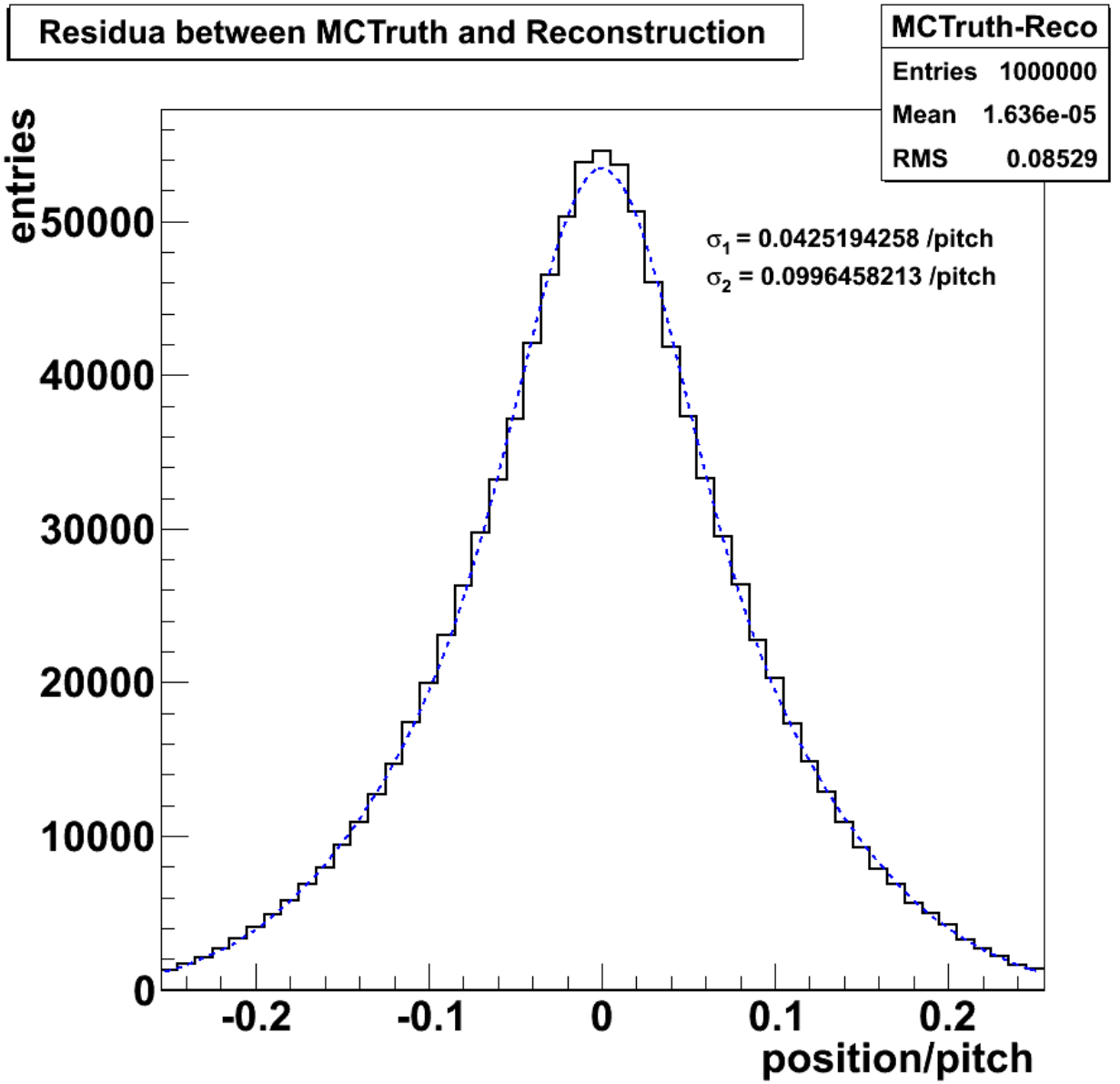
Simulation:
- FSSR2 digi – 3 bit
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- 2 strip hit
- clustering: Center of Gravity



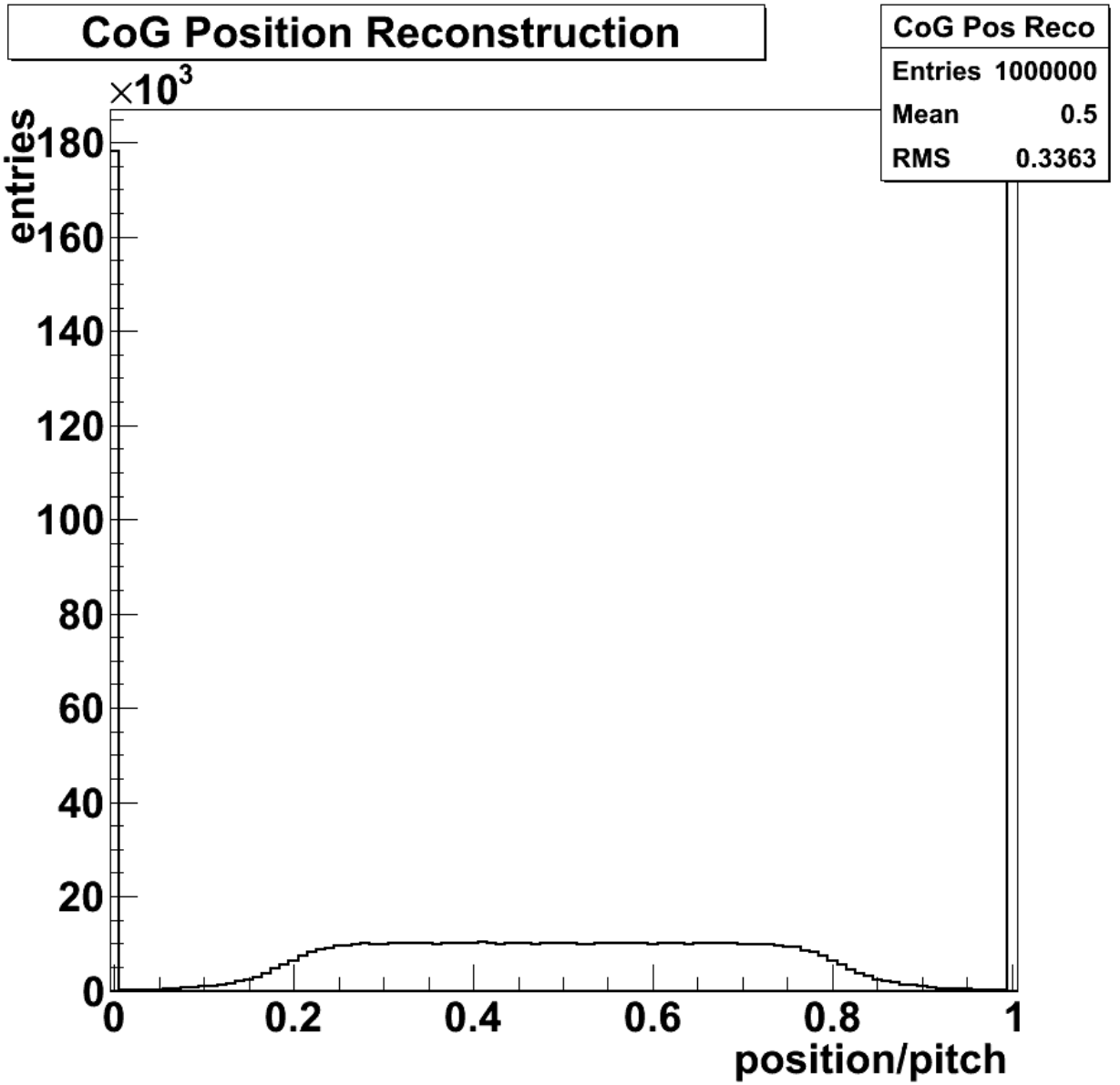
Simulation:
- FSSR2 digi – 3 bit
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- 2 strip hit
- clustering: Center of Gravity



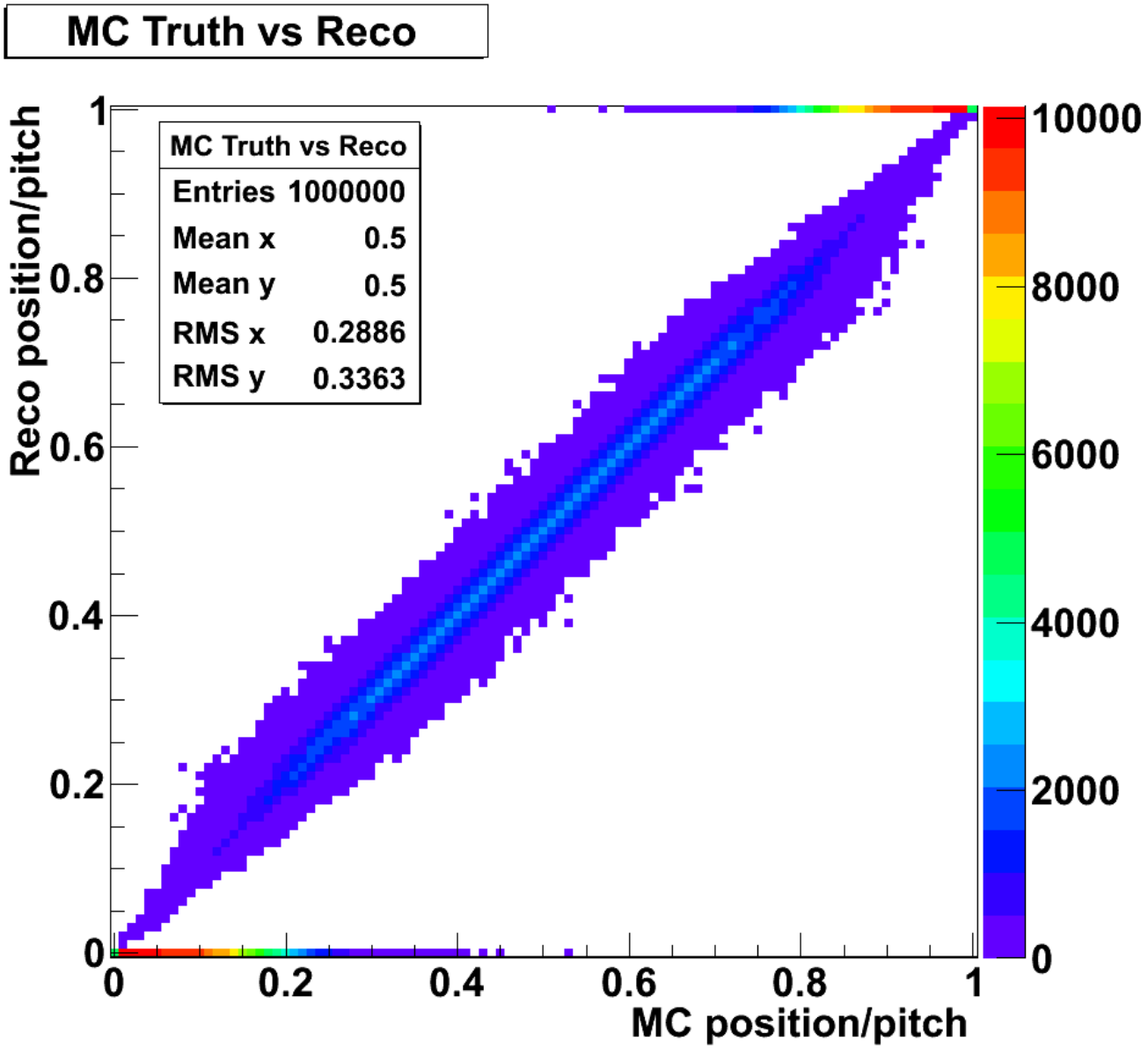
Simulation:
- FSSR2 digi – 3 bit
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- 2 strip hit
- clustering: Center of Gravity



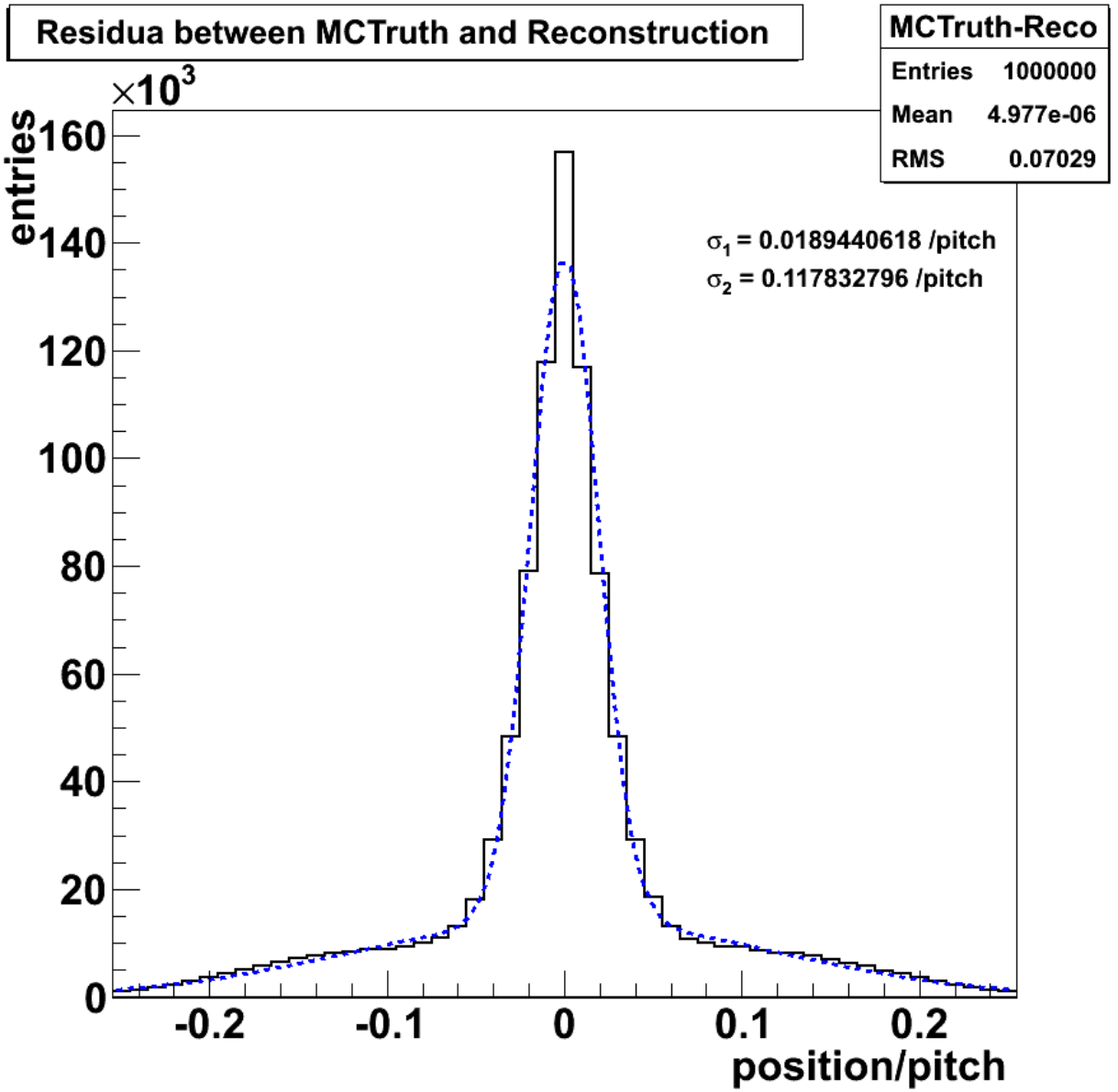
Simulation:
- “analogue” front-end
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- 2 strip hit
- clustering: Center of Gravity



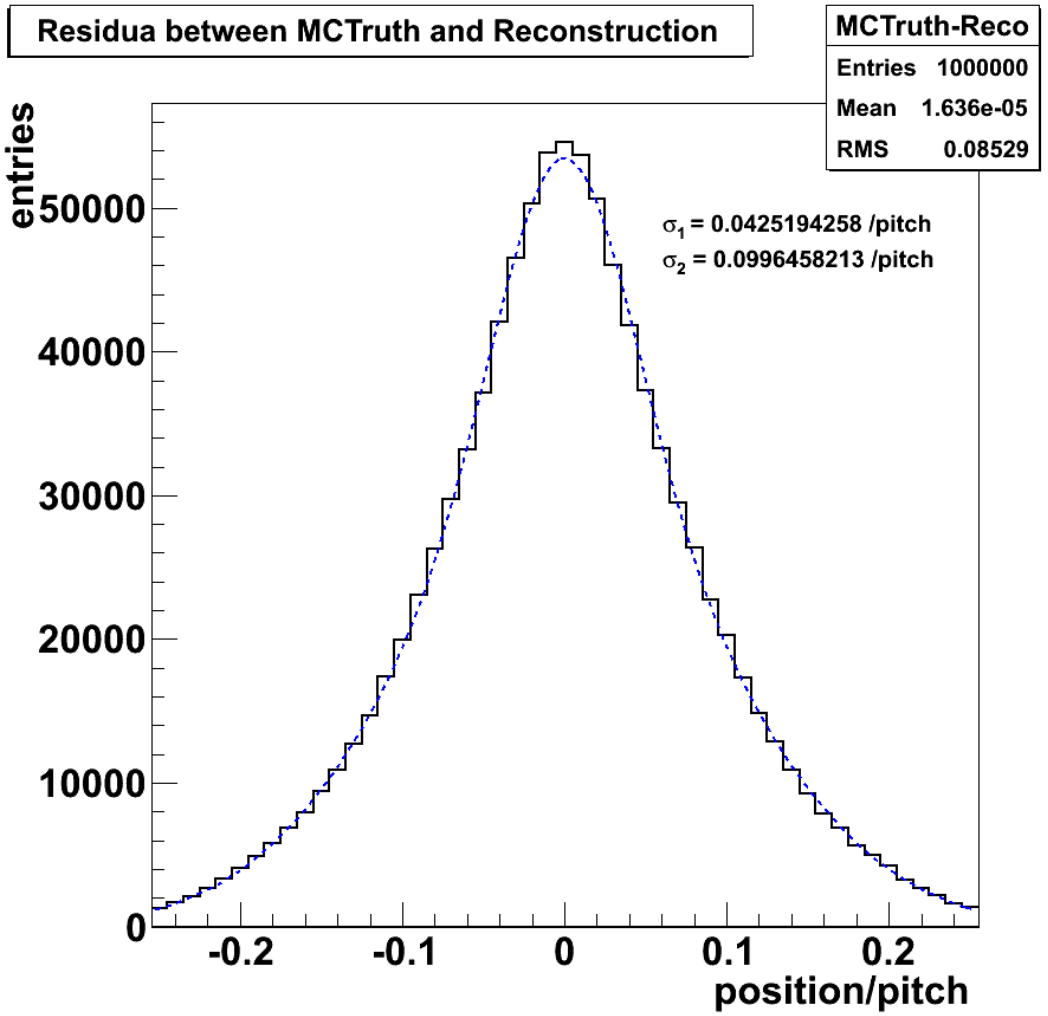
Simulation:
- “analogue” front-end
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- 2 strip hit
- clustering: Center of Gravity



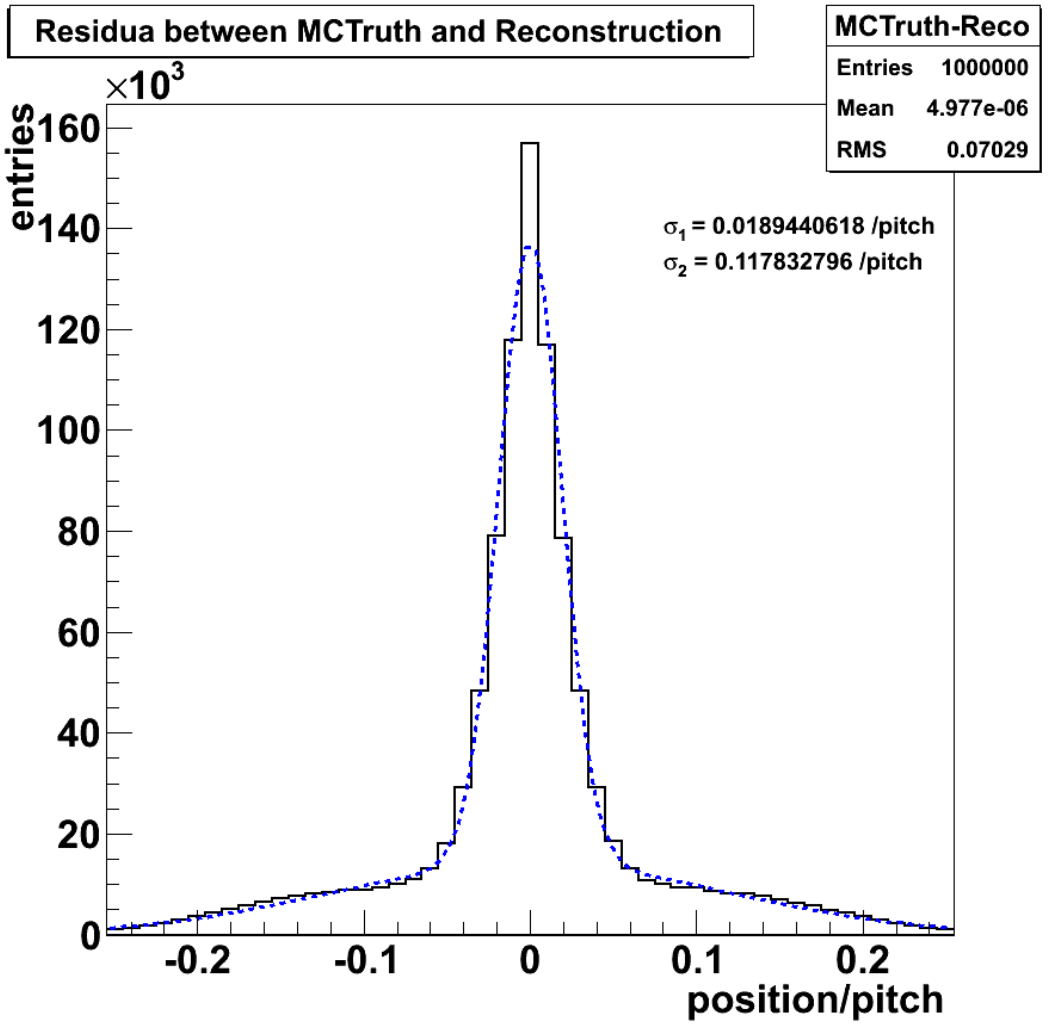
Simulation:
- “analogue” front-end
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- 2 strip hit
- clustering: Center of Gravity



3-bit digital front-end



analogue front-end



Options

- adapted ToPix3
- STS-XYTER
- (modified) FSSR2
- development by Marek Idzik et al.

ToPix3

- adaptation of analog circuits for strip detectors
- would provide comparable readout structures between pixel and strip part
- has been investigated by Alberto Potenza, Turin

ToPix3

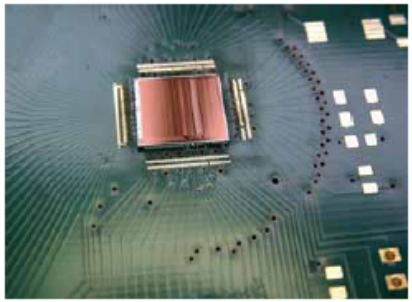
- performance achieved for the circuit:
  - power consumption 800 µW/chn, 1,2V
  - dynamic range up to 100 fC
  - minimum detectable charge 1,5 fC and
  - ENC 1000e^- for 20 pF detector capacitance
  - 130 nm CMOS technology
- key conclusion: no show-stopper found

STS-XYTER

- development by R. Szczygiel et al., AGH Krakow – in early prototype state
- self triggered architecture
- low power and low resolution dedicated for silicon strip detectors
- ToT-based digitization

CBM-XYTER Family Development

Interim work-horse front-end ASIC for FAIR detector prototyping



n-XYTER,
non rad hard
AMS 0.35µ

- Detector operation with
  purely data driven, self triggered readout
- engineering run prepared by H.K. Soltveit, PI Heidelberg

In parallel: chip development started in radiation hard UMC 0.180µ

CBM-dedicated FEE chip development

CBM STS XYTER
Low power, low resolution, TOT
AGH Krakow, R. Szczygiel et al.
work on 16 ch. test chip ongoing

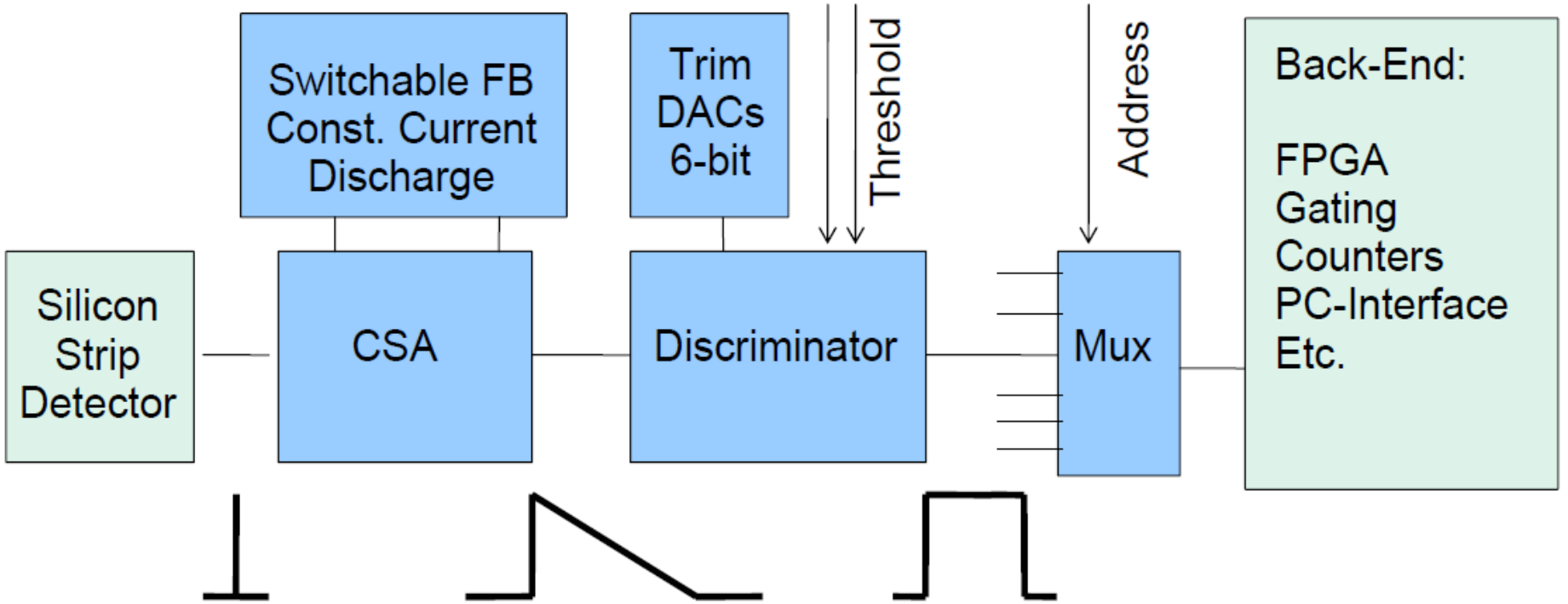
CBM Gas (TRD) –XYTER
SPADIC
higher res., adv. signal processing
ZiTi Heidelberg, P. Fischer et al
work on 32 ch. test chip ongoing

discussion ongoing towards a thrid, Much-Readout Chip with simple on-chip feature extraction

Low Power STS-XYTER in Second Iteration

Chip Overview - Architecture

UMC 0.180 technology for radiation hardness

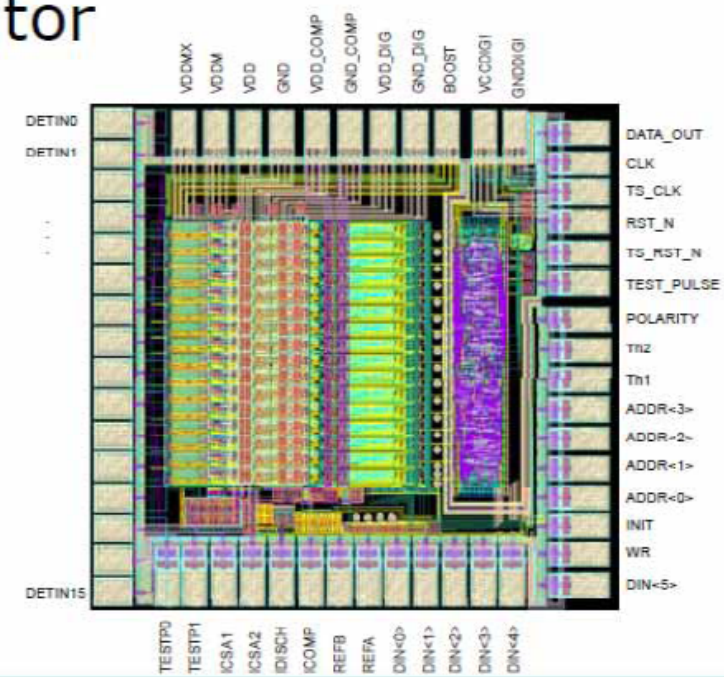


- Time over threshold energy conversion (ToT)
- 2.3 mW/channel at 500 ENC/30pF (c.f. ~20mW on n-XYTER)
- 4 to 6 bit resolution
- 30 channels

R. Szczygiel et al., AGH Krakow

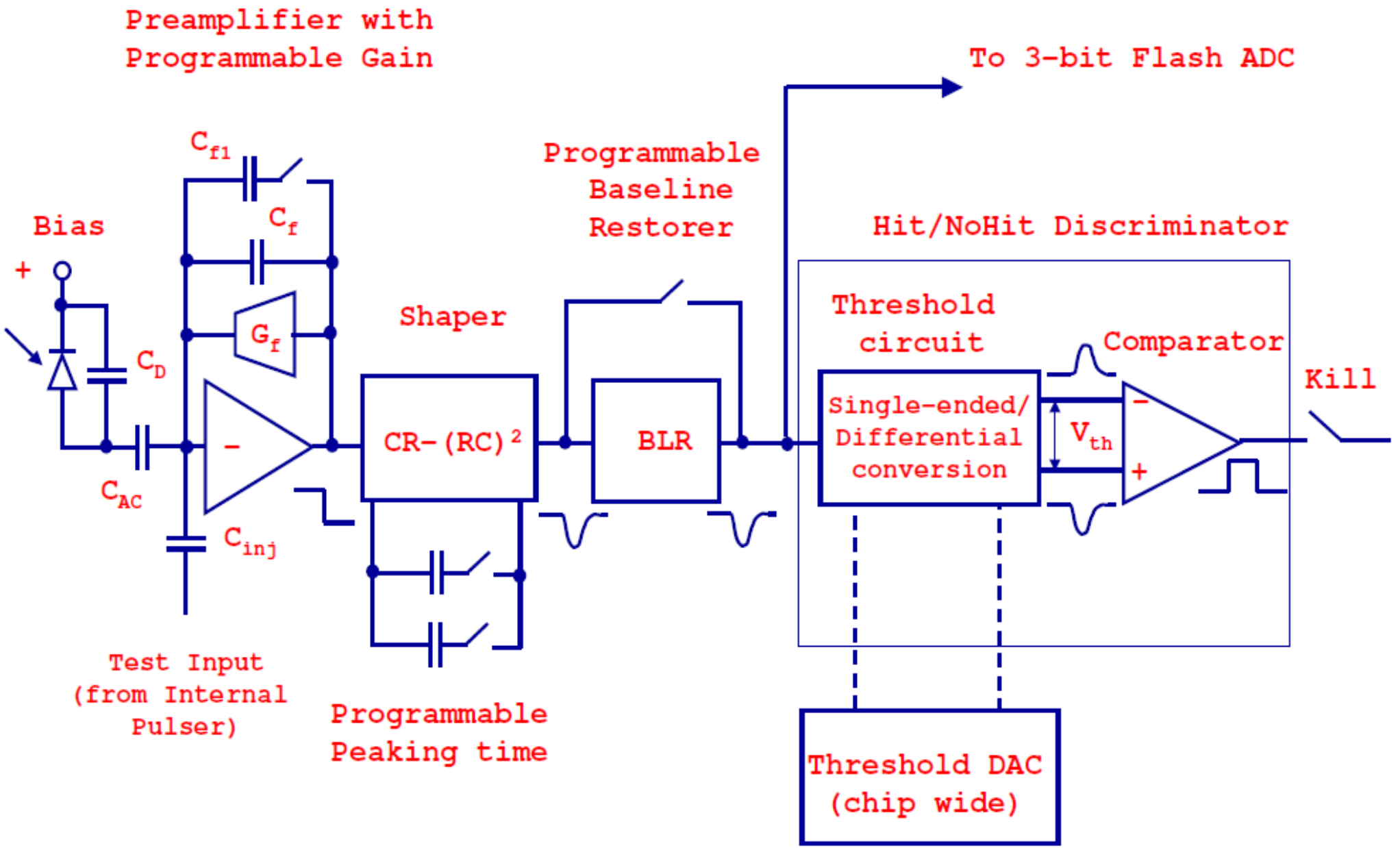
TOT02 new features

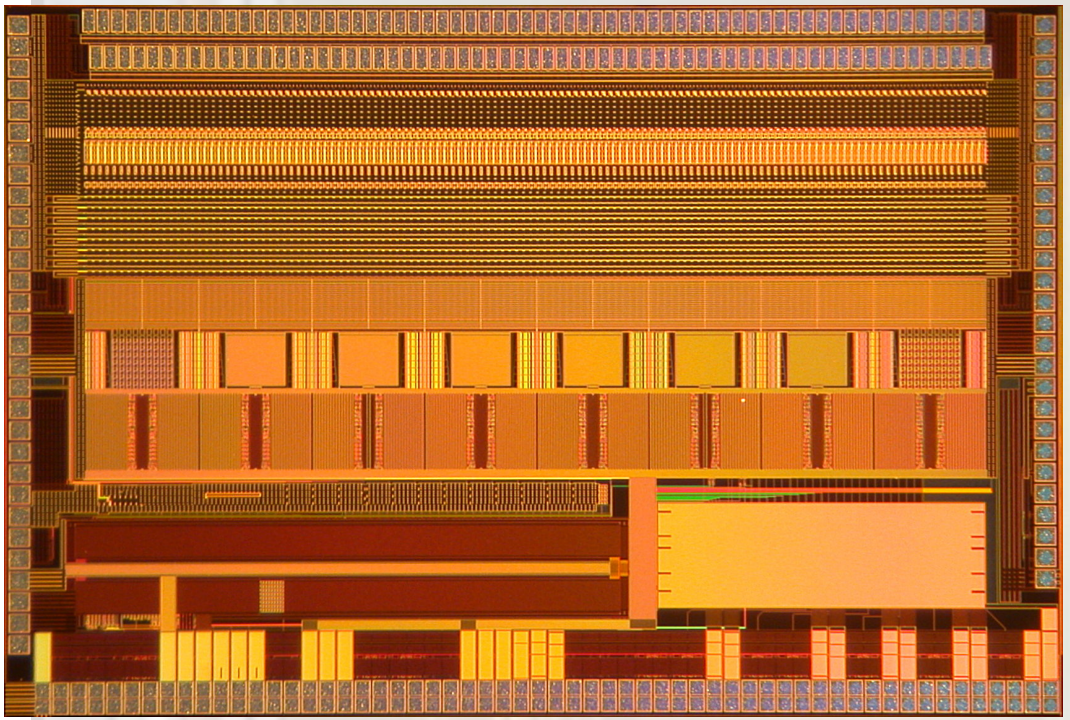
- 16 channels (size: 1.5 µm x 1.5 µm)
- Front-end : CSA core modified, rad hard layout
- Back-end : timestamp, token, serializer
- Other:
  - Pulse streachers after comparator
  - Test capacitors removed



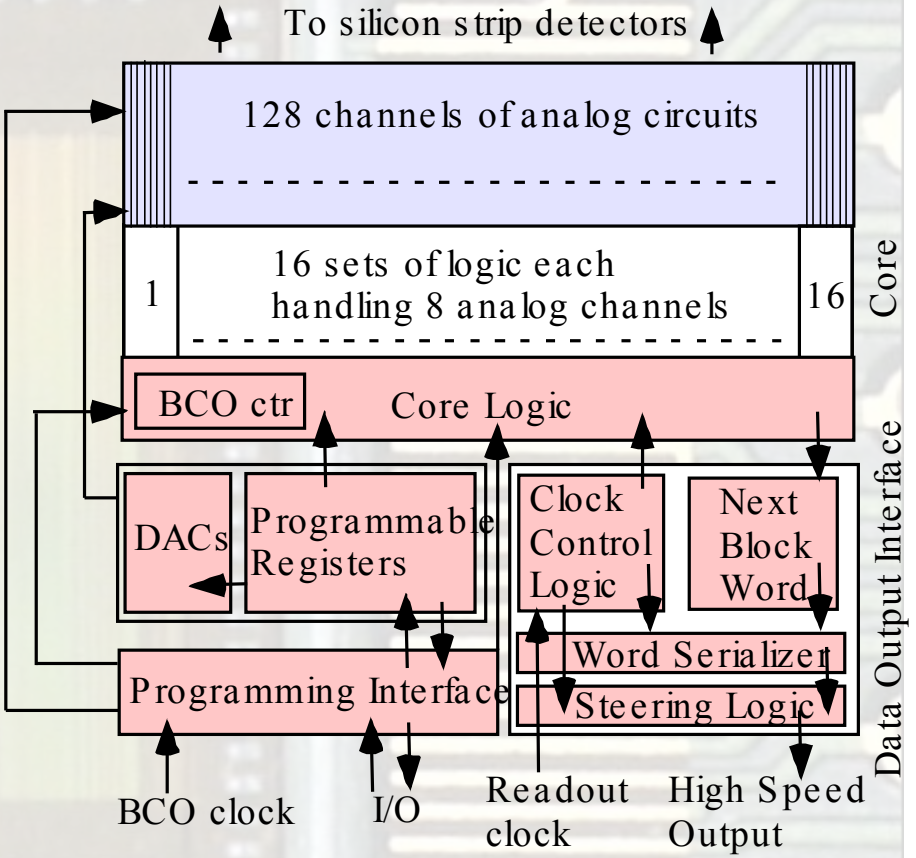
FSSR2

- developed for BTeV, Forward Silicon Tracker
- data driven architecture – no trigger
- peaking time and gain selectable
- 3-bit Flash-ADCs with selectable thresholds
- but: time stamping with beam crossing time of 132 ns


Preamplifier with
Programmable Gain
To 3-bit Flash ADC
Programmable
Baseline
Restorer
Hit/NoHit Discriminator
Bias
Shaper
Threshold
circuit
Comparator
Kill
Single-ended/
Differential
conversion
CR-(RC)²
BLR
Test Input
(from Internal
Pulser)
Programmable
Peaking time
Threshold DAC
(chip wide)



(7.5x5) mm^2, input pads pitch 50 µm



FSSR2

- chance to acquire some chips via Mainz
- planned:
  - build test board
  - get experience with fully digital FE
- needed modifications:
  - time stamping !
  - ADC resolution?
  - data link

Marek Idzik et al.

- development for the ILC luminosity detector
- goals:
  - precise time information
  - good amplitude resolution
  - good pileup rejection
  - low power consumption
- test system with one of our 2x2 cm^2 sensors bonded to his front-end

AGH University of Science and Technology

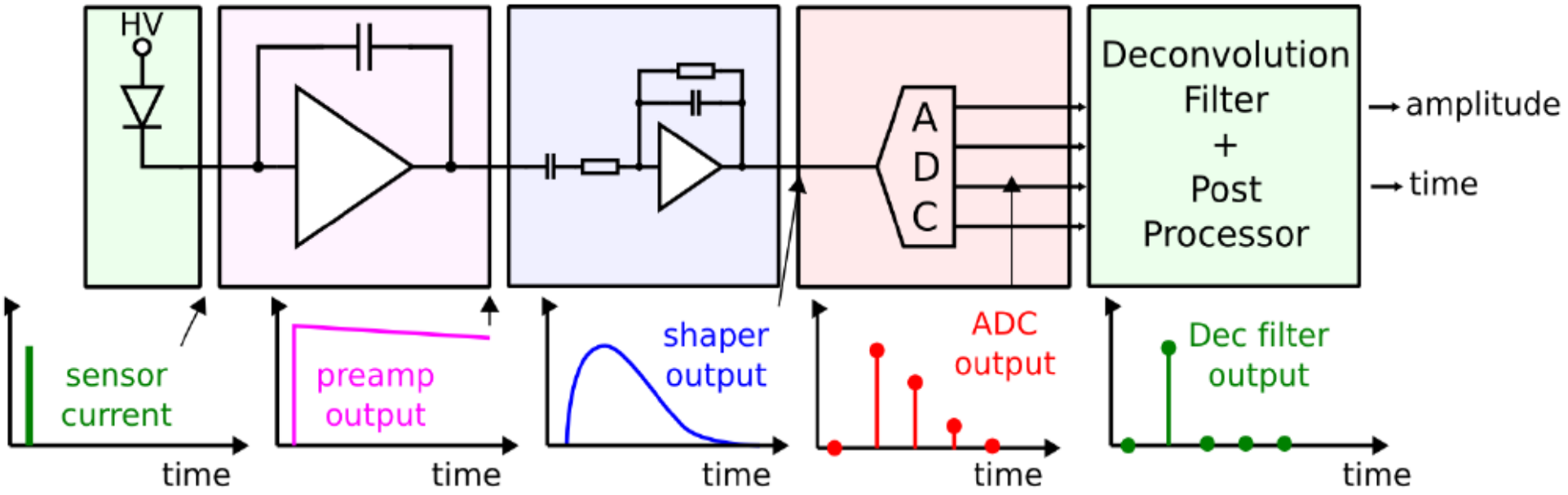
Triggerless readout with time and amplitude reconstruction of event based on deconvolution algorithm

Szymon Kulis, Marek Idzik

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

Kraków | Workshop on Timing Detectors 29-30.XI - 1.XII.2010

Readout electronics diagram - deconvolution



- Pulse at output of shaper v(t) is convolution of input signal (current from sensor – s(t)) and impulse response of readout chain h(t):

$$v(t) = \int_{-\infty}^{+\infty} h(t-x)\,s(x)\,dx$$

- Using data from continuously running ADC and taking advantage of known pulse shape one can perform invert procedure – **deconvolution** – to get information about event time and amplitude

Deconvolution for CR-RC shaping

$$d_i = s_i + w_1 s_{i-1} + w_2 s_{i-2}$$

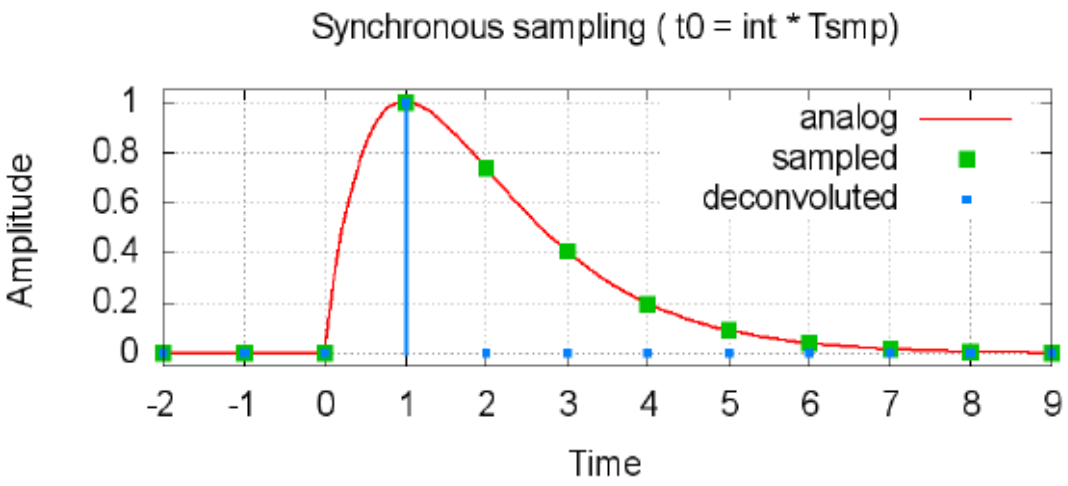
CR-RC, $T_{smp} = T_{peak} = 1$, amp = 1

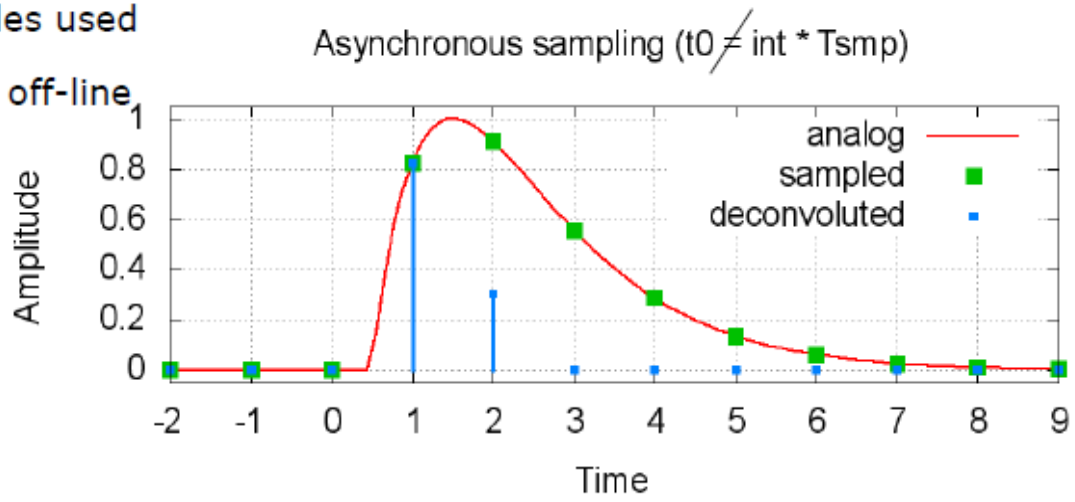
- Only two multiplications and three additions (very fast and light !)
- Deconvolution produces non-zero data only when one or two first samples are on baseline, and second/third is on pulse
- **Initial time** of pulse is found from ratio of those samples
- **Amplitude** is found from sum of those samples, multiplied by time dependent correction factor

} Look Up Tables used

Can be done off-line

- Deconvolution reduces (infinite number) of CR-RC pulse samples to 1 or 2 non zero samples !



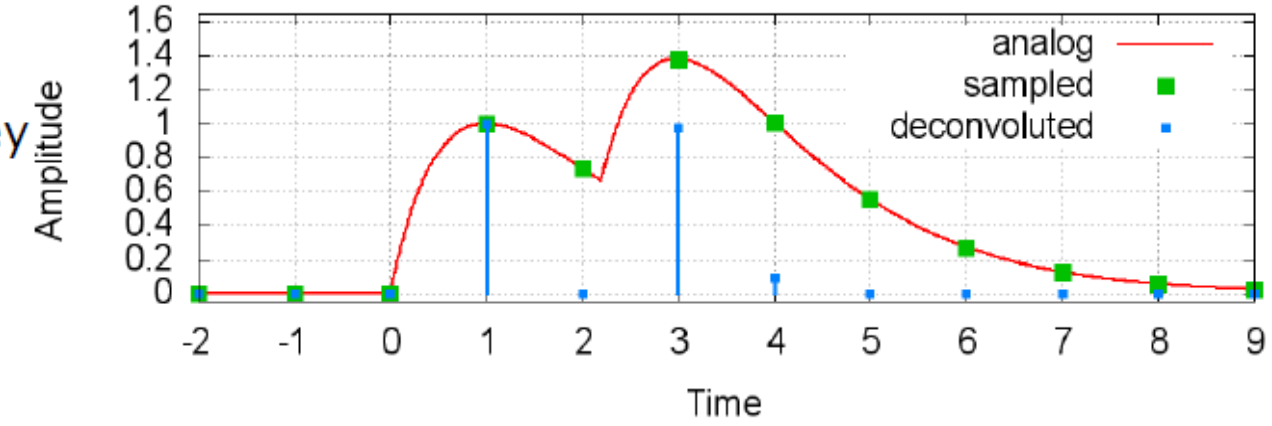


CR-RC Deconvolution properties | Pileup

CR-RC, $T_{smp}=T_{peak}=1$, amp =1

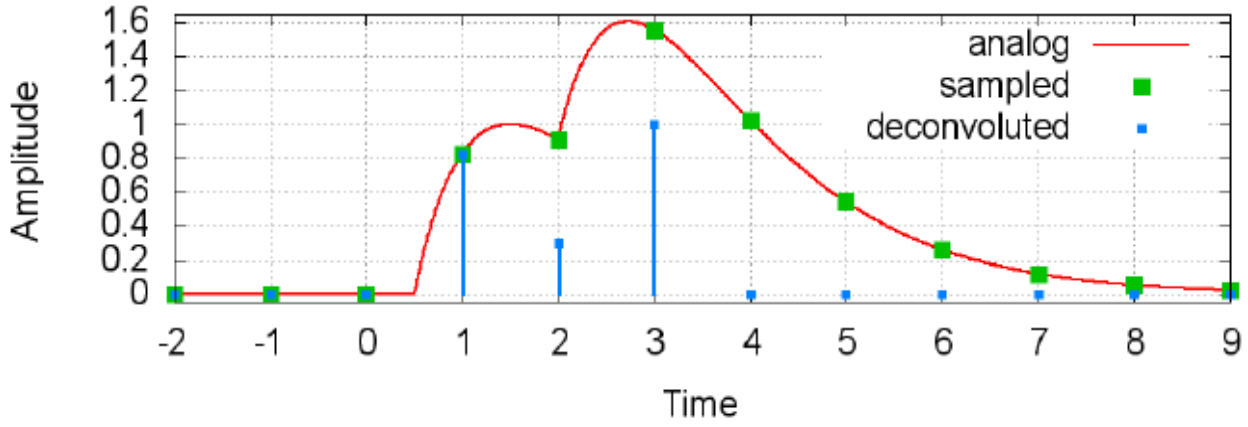
- Two events can be separated and precisely measured if they are distant 2-3 T_{smp}

Resolvable pileup : $t_0 - t_1 = 2.1 * T_{smp}$

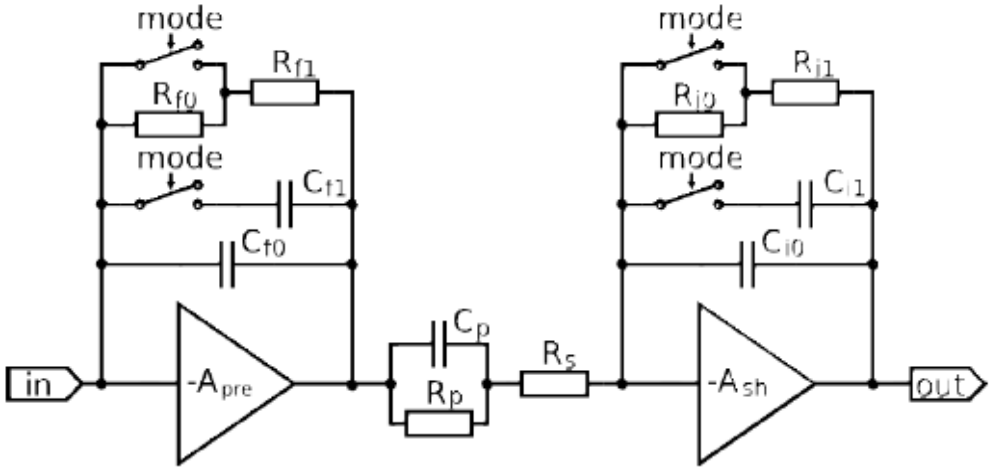


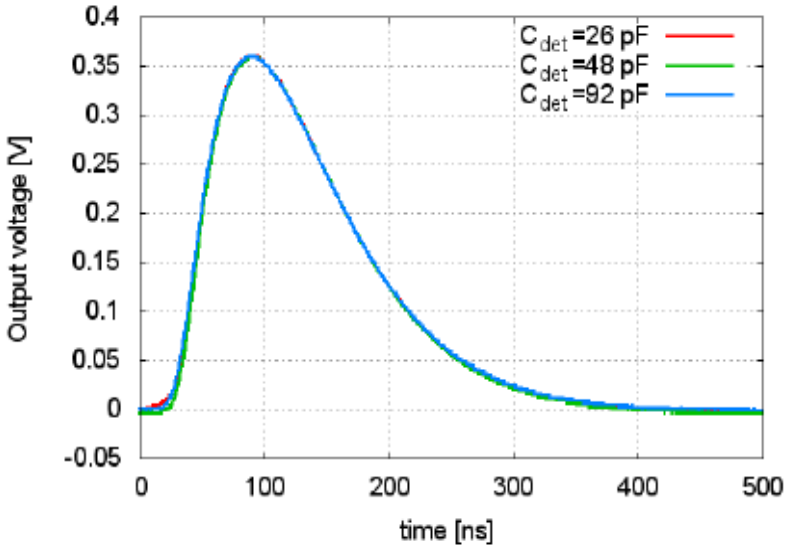
- For shorter distance between pulses additional signature of not resolvable pileup may be used (more than 2 non zero samples)

Detected non-resolvable pileup : $t_0 - t_1 = 1.5 * T_{smp}$



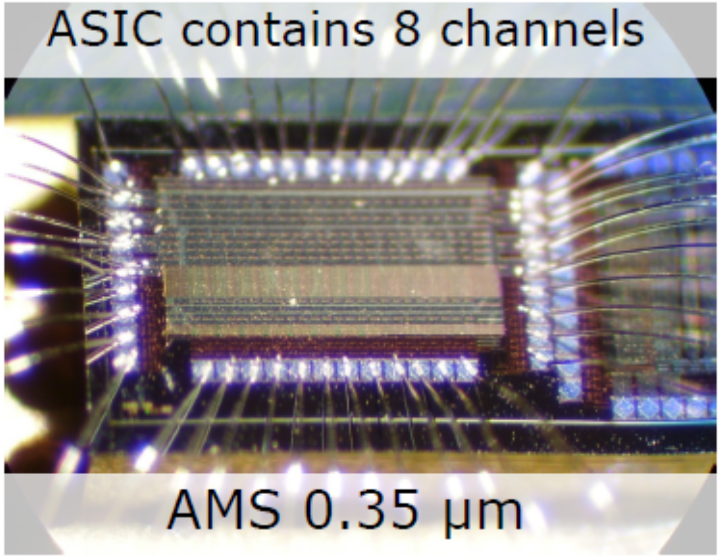
Front-end Electronics & Sensor (designed for LumiCal detector@ILC)





Front-end spec:

- $C_{det} \approx 0 \div 100pF$
- 1st order CR-RC shaper ($T_{peak} \approx 60$ ns)
- variable gain
- SNR ~ 20 for MIP

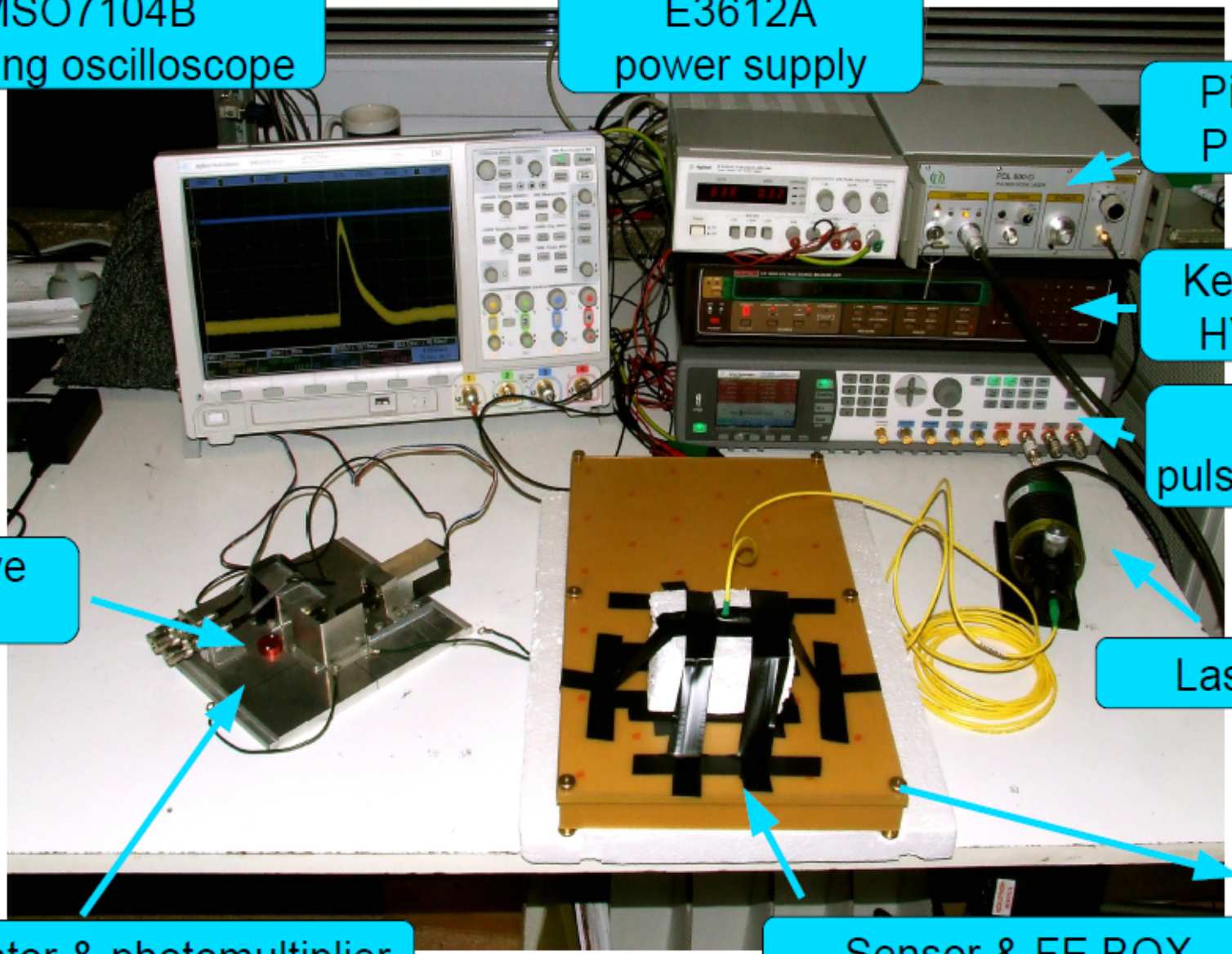


Standard Silicon sensor :

- Thickness 300um
- Capacitance ~ 5 – 25 pF / channel
- Leakage current ~ 5nA / channel

See more : M. Idzik, Sz. Kulis, D. Przyborowski "Development of front-end electronics for the luminoisty detector at ILC" Nucl. Instr. and Meth. A 608 (2009) pp.169-174

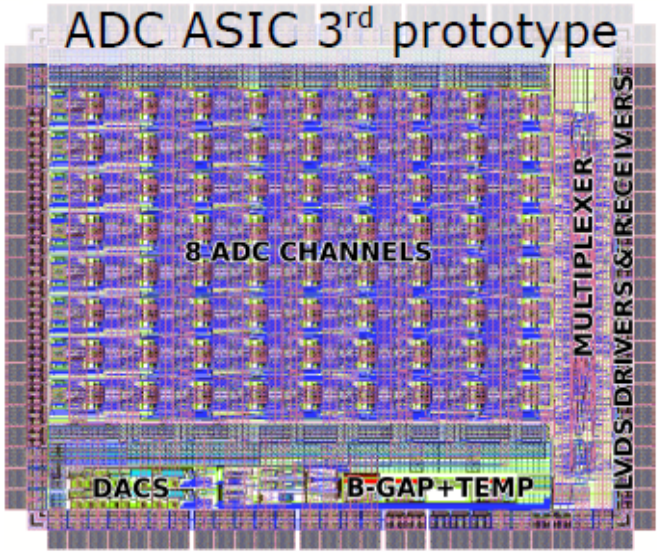
Photograph of Measurement Setup



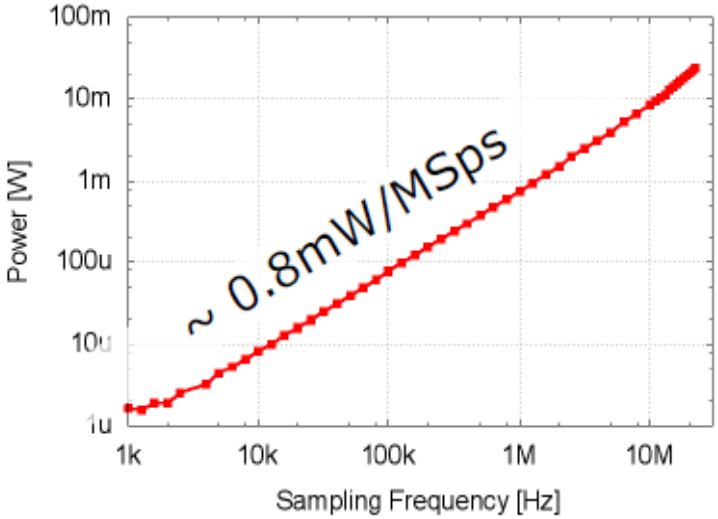
Very soon scope digitizer will be replaced by our new Multichannel ADC SoC ASIC

- **8 channels of 10 bit pipeline ADC** (verified to work up to **50Msps**)
- Power scales linearly with f_{smp}
- Power switching on/off mechanism
- Cross talk < -70dB
- Digital multiplexer/serializer:
  - Serial mode (max f_{smp} ~ 4 MSps)
  - Parallel mode (max f_{smp} ~ 30MSps)
  - Test mode (single channel readout)
- High speed LVDS drivers (~1GHz)
- Low power DAC control references
- Precise BandGap reference source
- Temperature sensor
- Die size ~ 2 x 3 mm

ADC ASIC 3rd prototype



ADC Core Power Consumption

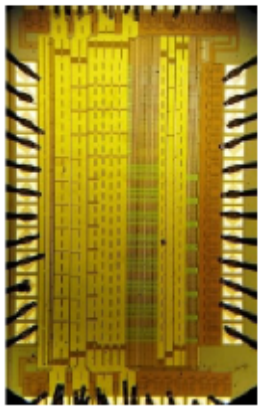


ADC ASIC 2rd prototype

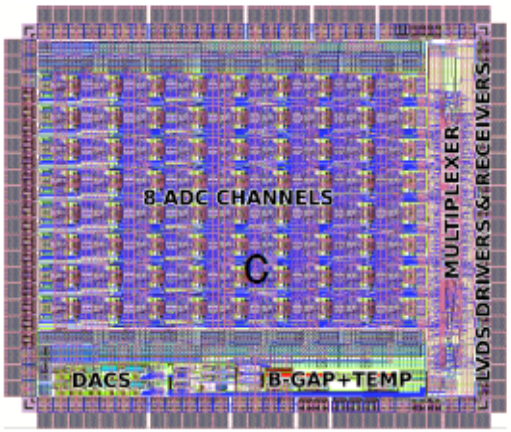
Future plans – short term

- Extend our prototype system (~8-32 channels) by replacing external ADC with our multichannel ADC SoC and possibly add FPGA based deconvolution DSP

- Verify such triggerless system on testbeam



LumiCal Front-end ASIC
(Front-end with different Shaping time may be used)



Multichannel ADC
(System on Chip)

Xilinx FPGA
(Reading ADC and performing on-line deconvolution)

Future plans ...

- Work in progress on extending the analyses (and measurements if possible) of deconvolution performance on:
  - optimization of power consumption, sampling time, shaping time for given specifications
  - precise calculation of correlated noise for given shaping/sampling
  - implementation of higher order shaping like CR-RC^n
  - study ADC quantization effects
  - study pileup effects
- For multichannel systems requiring sampling rates of tens of MS/s power consumption of our ADC SoC (~0.8 mW/MHz) may be too high for multichannel systems

We have started the design of ADC in 130nm technology with the goal of obtaining power consumption much below 0.1 mW/MHz

Discussion points

- front-end ?
- possibility to work on ToPix for strips
- GBT-chipset:
  - option
  - connection – data and slow control
- "estimate" cooling requirements

Discussion points

- Cooling:
- Power to dissipate → 1 W per front-end chip
- Power per area → 2 W/cm^2, assuming FE with 0.5 cm^2
- Power/stave, power/disk section → Thomas
- Total Power to dissipate /volume → Thomas
- Final acceptable temperature → ?
- Routing of cooling pipes at barrel and disks level, position and scheme.
- System description: use of carbon foam?, contact type-glue?,....
- Particular requests for electronics or other things