Module-Controller design for the MVD silicon strip sensors

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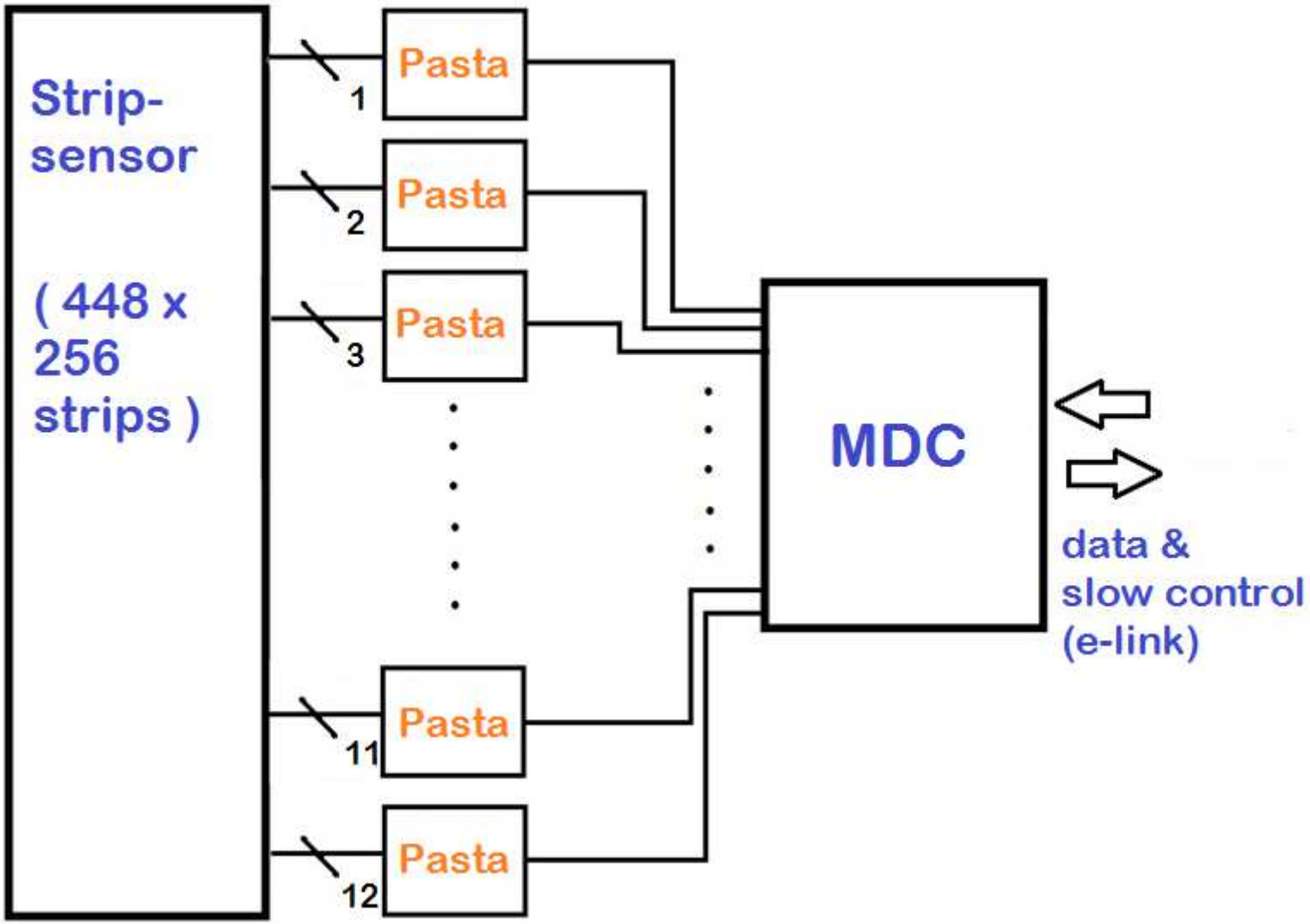
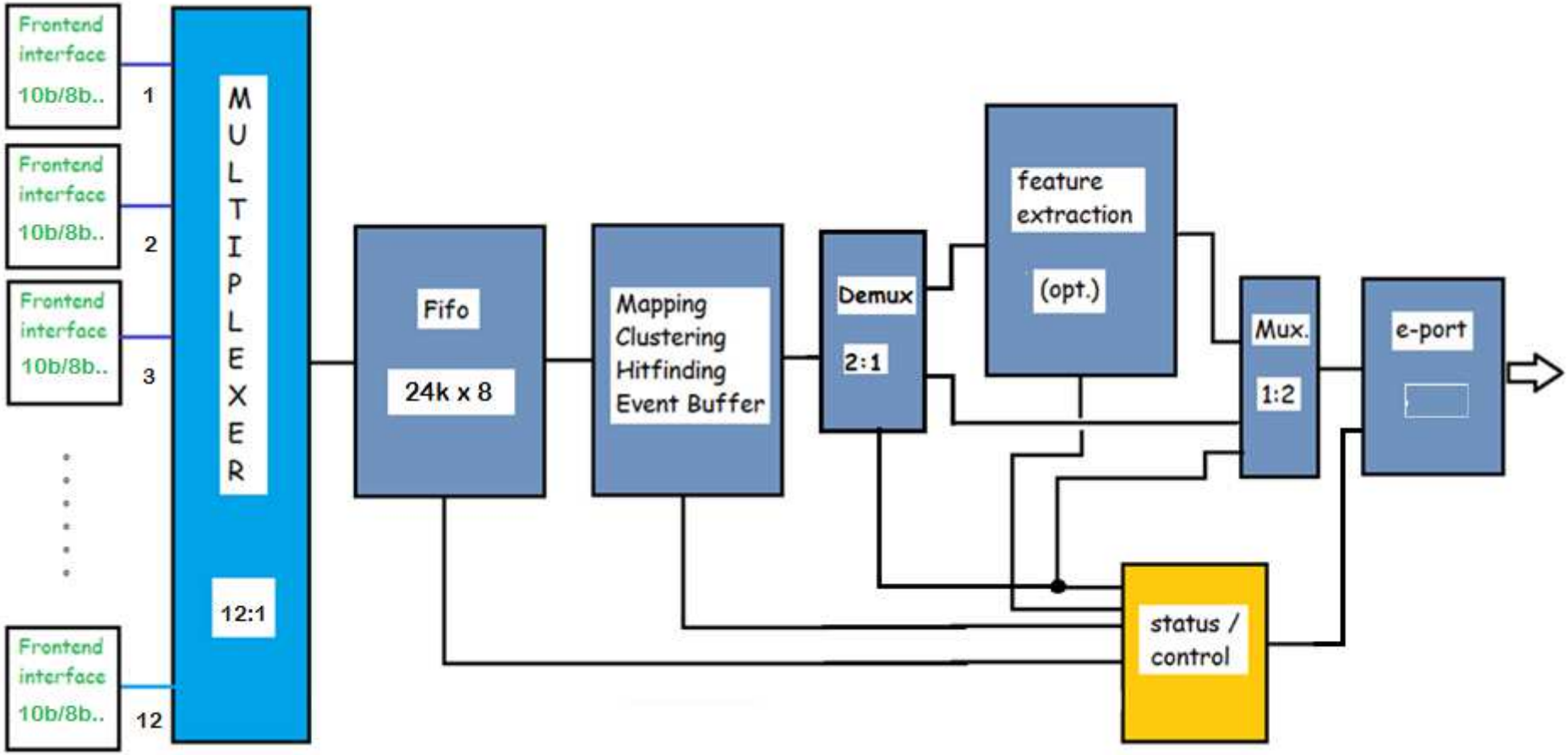
- strip sensor module read-out : Pasta (64 channels)
- 12 FE-chips maximum per sensor module
- one module-controller (MDC) per module
- one E-link per MDC for data transfer and slow control


Strip-
sensor
(448 x
256
strips)
1
2
3
11
12
Pasta
Pasta
Pasta
Pasta
Pasta
MDC
data &
slow control
(e-link)

Module controller internals



I/O's / Pads

12x Pasta (SLVS)	96
Slow Control (SLVS)	8
E-Link (SLVS)	6
V_{DD}, V_{CC}	8
Total	118

Power estimation

Basic Design	68 mW	
Full Design	200 mW	
SLVS-I/O's	93 mW	
Total Basic	161 mW	0,21 mW/Ch.
Total Full	293 mW	0,38 mW/Ch.

Chip size estimation

Memory plus Logic : $\approx$ 5 M Gates
Size: 22 mm^2 @ 230k gates per mm^2
144 Pads @ 0,01" pitch (or smaller)

Status November 2015:

design versions: with / without feature extraction

design & simulation of FPGA prototype (VHDL-based) is finished for: 12:1 multiplexer, fifo, frontend-inteface, 10b/8b-decoding, triple redundancy

under simulation: triple redundancy

under design/simulation: clustering/hitfinding

to be done : status and control,e-link, slow control