

# ToASt status report

Gianni Mazza

INFN sez. di Torino

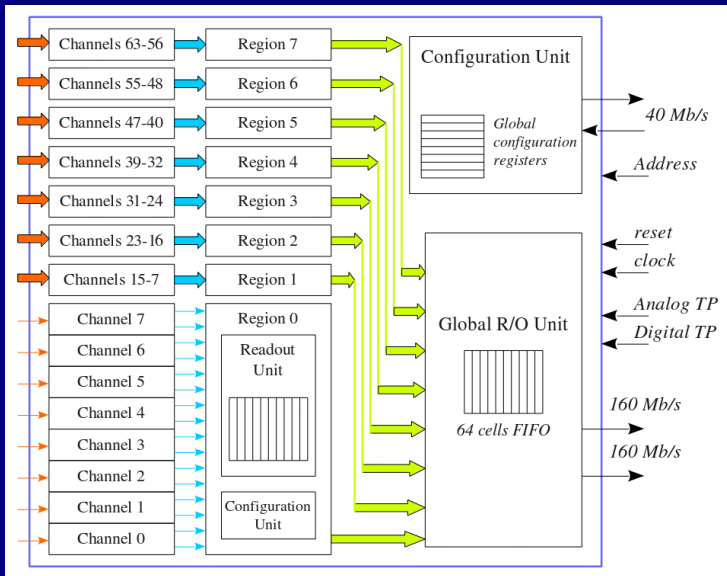
*mazza@to.infn.it*

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# Specifications

<b>Specification</b>	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e <sup>-</sup>
Preamp peaking time	50	100 (?)	ns
Channels per chip	64		
Reference clock	160		MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.2 × 3.5		mm <sup>2</sup>
Pads position	On two sides only		

# ToASt architecture



# ToASt preliminary pinout

Pin name	Direction	Description
in[63:0]	In	Analog inputs
SyncReset	Rx	Synchronous reset
ChipAddr[6:0]	In	Chip address
TestPulse	In	Digital test pulse
Analog_TP	In	Analogue test pulse (tbc)
CfgRx	Rx	Configuration receiver
CfgTx	Tx	Configuration transmitter
TxOut_0	Tx	Data serial output 0
TxOut_1	Tx	Data serial output 1

# Channel configuration - *Preliminary*

Register	Bits	Function
0	11:8	<i>Reserved for future use</i>
0	7	Channel mask
0	6	Delay enable
0	5	Calibration enable
0	4:0	ToT discharge current calibration DAC
1	11:10	<i>Reserved for future use</i>
1	9:5	Energy threshold calibration DAC
1	4:0	Time threshold calibration DAC

**WARNING ! This is not the final assignment - Work in progress...**

# Global configuration - *Preliminary*

Register	Name	Function
0	11	<i>Reserved for future use</i>
0	10	detector polarity
0	9	leading edge-only mode
0	8	single threshold mode
0	7:6	<i>Reserved for future use</i>
0	5	T <sub>x</sub> 1 enable
0	4	T <sub>x</sub> 0 enable
0	3:2	<i>Reserved for future use</i>
0	1	Time stamp counter Gray mode
0	0	Time stamp counter enable
1	11:8	<i>Reserved for future use</i>
1	7:0	Region disable

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# What has been done

- VHDL code of the channel logic
- VHDL code of the region logic
- VHDL code of the chip readout logic
- VHDL code of the chip configuration logic (write only)
- VHDL code of the TMR protected serializers
- SEU protection of registers, counters and FIFOs

# Missing items

- SEU protection for FSM
- VHDL code of the chip configuration logic (read part)
- Header and trailer insertion with CRC calculation
- Synthesis and P&R



# Simulation files - Barrel, sensor 190

Chip #	0	1	2	3	4	5	6	7	8
# of events	343	361	313	242	341	373	6	0	0
Events above 40 fC	20	26	6	0	24	12	0	0	0
Avg charge [fC]	13.26	20.44	9.30	10.10	14.89	15.09	7.10	0	0
Max charge [fC]	149.93	343.46	138.15	38.04	14.89	15.09	11.49	0	0
Avg ToT [ns]	530.6	817.6	372.1	404.0	595.5	603.5	283.8	0	0
Max ToT [ $\mu$ s]	6.0	13.7	5.5	1.5	13.4	13.7	0.5	0	0
Rate per channel [kHz]	4.33	4.56	3.95	3.06	4.31	4.71	0.08	0	0

- 128 channel per chip are assumed
- No events on chips 7,8 (barrel), 8 (forward)
- Rate < 5 kHz (maximum expected is 40 kHz)
- Max charge above 300 fC (i.e. ToT > 12  $\mu$ s w/o clipping)
- Most hits are on more than one strip

*Note : ToT Gain 40 ns/fC in the simulations (to have 1.6  $\mu$ s at 40 fC)*

# Simulation files - Barrel, sensor 190

Chip n.	Channel range	Input events	Output events	Lost events	Synch words
0	0-63	208	206	2	4200
0	64-127	135	133	2	4335
1	0-63	192	192	0	4126
1	64-127	169	165	4	4294
2	0-63	164	164	0	4277
2	64-127	145	149	4	4299
3	0-63	140	133	7	4314
3	64-127	102	102	0	4309
4	0-63	179	179	0	4287
4	64-127	162	162	0	4287
5	0-63	207	196	11	4255
5	64-127	166	165	1	4241
6	0-63	6	6	0	4324
6	64-127	0	0	0	627

*Event loss still under investigation...*

# Lost events example : Barrel, sensor 190, chip 0

Channel 9 :  $\Delta T = 1$  ns

```
164791 190 4 5 0.000221017
164791 190 4 4 0.000221017
164791 190 4 5 0.000221017
165206 190 0 9 0.000151042
165206 190 0 8 0.000151042
165206 190 5 15 0.000151042
165206 190 5 16 0.000151042
165206 190 5 17 0.000151042
165206 190 5 18 0.000151042
165206 190 5 19 0.000151042
165207 190 0 9 0.000137269
165207 190 0 10 0.000137269
165207 190 5 103 0.000137269
165207 190 5 104 0.000137269
```

Channel 27 :  $\Delta T = 0$  ns

```
372854 190 2 86 0.00023847
372854 190 2 87 0.00023847
372854 190 2 88 0.00023847
372854 190 2 89 0.00023847
372854 190 4 3 0.00023847
374957 190 0 27 0.000170951
374957 190 0 28 0.000170951
374957 190 0 29 0.000170951
374957 190 0 30 0.000170951
374957 190 0 31 0.000170951
374957 190 4 2 0.000170951
374957 190 4 3 0.000170951
374957 190 4 4 0.000170951
374957 190 0 27 0.000176699
374957 190 0 23 0.000176699
374957 190 0 24 0.000176699
374957 190 0 25 0.000176699
374957 190 0 26 0.000176699
374957 190 4 81 0.000176699
374957 190 4 82 0.000176699
```

Channels 66-67 :  $\Delta T = 0$  ns

```
22296.1 190 5 23 0.000434277
22296.1 190 0 66 0.000253243
22296.1 190 0 67 0.000253243
22296.1 190 5 31 0.000253243
22296.1 190 5 32 0.000253243
22296.1 190 0 68 0.000253243
22296.1 190 0 69 0.000253243
22296.1 190 0 70 0.000253243
22296.1 190 5 30 0.000253243
22296.1 190 0 66 7.99529e-06
22296.1 190 0 67 7.99529e-06
22296.1 190 5 31 7.99529e-06
22296.1 190 5 32 7.99529e-06
```

# Conclusions

- First release of the ToASt digital logic completed
  - Some features still missing
  - Pre-sintesi code
- Simulations with realistic data ongoing
  - Barrel sensor 190 has been studied
  - Event loss of the order of few %
  - Probably related to superimposed events
- Update on the analogue part in the next meeting (Jonhatan)