JUSTUS-LIEBIG-
UNIVERSITÄT
GIESSEN

READOUT ASIC for the MVD STRIPS

Status of the design

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NEW

BLOCKS	BIAS	DAC	SCHEMATIC	LAYOUT	SCH. SIM	POST LAY. SIM
TP INJECTION		6 bit				
PREAMP		5 bit				
FEEDBACK NETWORK N/P		5 bit				
SHAPER		5 bit				
CURRENT BUFFER		5 bit				
BASELINE HOLDER		LOCAL				
TOT AMPLIFIER		LOCAL				
DISCRIMINATOR						

- **The next step is the check of the behaviour of more channels which share the same bias cells.**

Calibration circuit of PASTA

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From User Guide of PASTA pg. 8

The **Write global test configuration** command is used to access the calibration circuit controlling the amplitude of the pulse and the channel to test (Table 6).

Position	Description	Default
13:8	Channel address which is connected to the probing pads	000000
7	Enable the probing of key signals going from selected channel to the output pads	0
6:1	DAC settings for the pulse amplitude	XXXXXX
0	Enable the calibration circuit	0

Table 6: Default value for the Write global test configuration

The global calibration circuit of PASTA is enabled when this is 1