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GIESSEN

READOUT ASIC for the MVD STRIPS

Design of the new analog front-end

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The analog readout architecture

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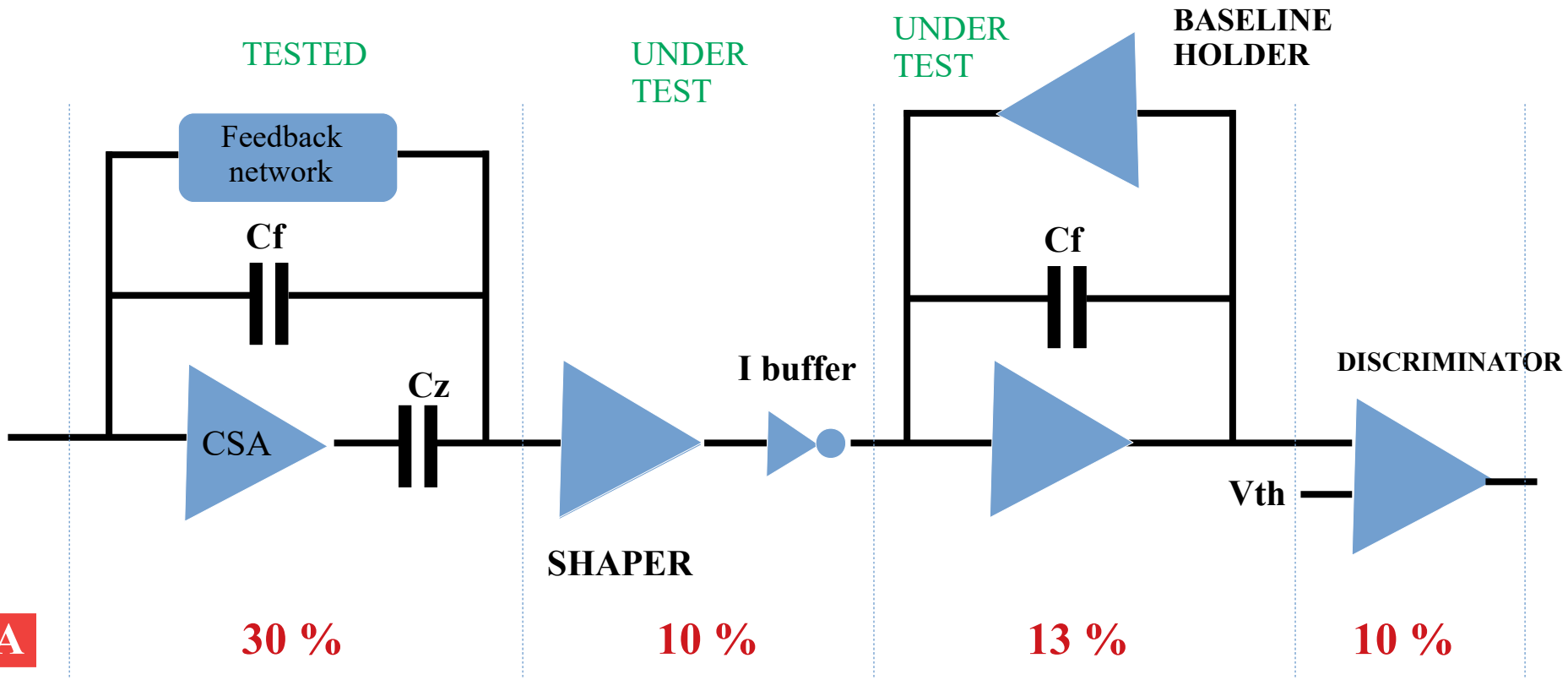
The design is based on the same architecture of PASTA



Others blocks: Filters (17%), Delay line (9 %), Internal pulser (3%), others

The Charge Sensitive Amplifier

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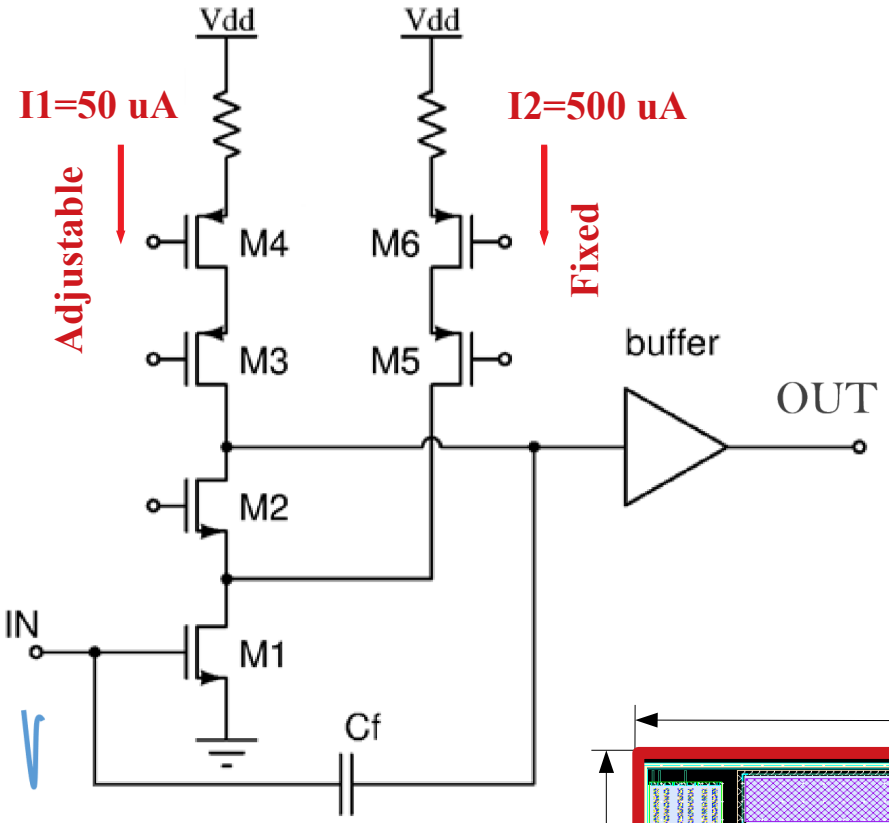
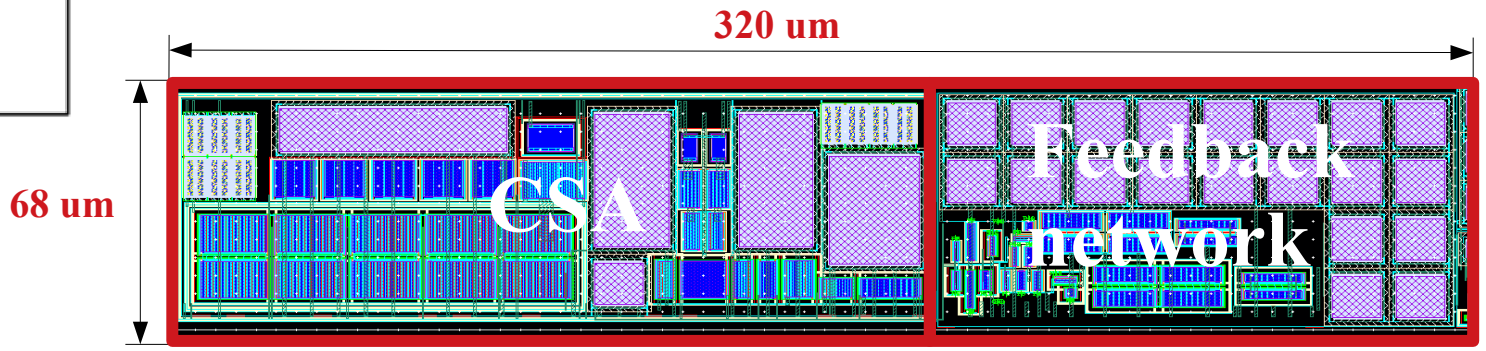
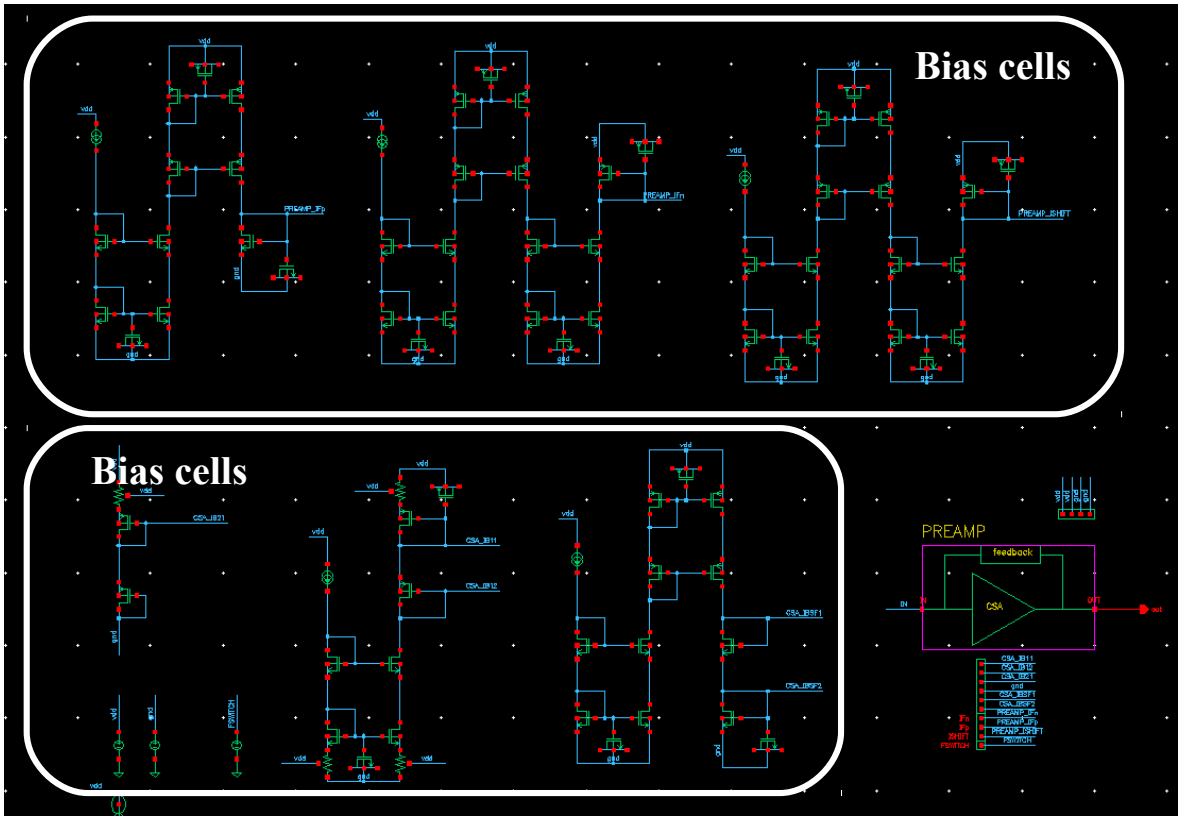


- The biggest contribution in terms of current comes from I2 which is the second branch. This current is FIXED in PASTA and so it cannot be regulated at all.
- I1 is adjustable through a global DAC.
- The block is very compact but contains caps which can be resized if needed due to area constraints.



SIMULATIONS



- Only real bias cells are used.
- No DACs are used at this level. This is the best way to decide the optimal range for voltages/currents. We can change them if needed (threshold)
- The simulations are at schematic level
- The input charge is generated with an ideal source

CSA: sim results

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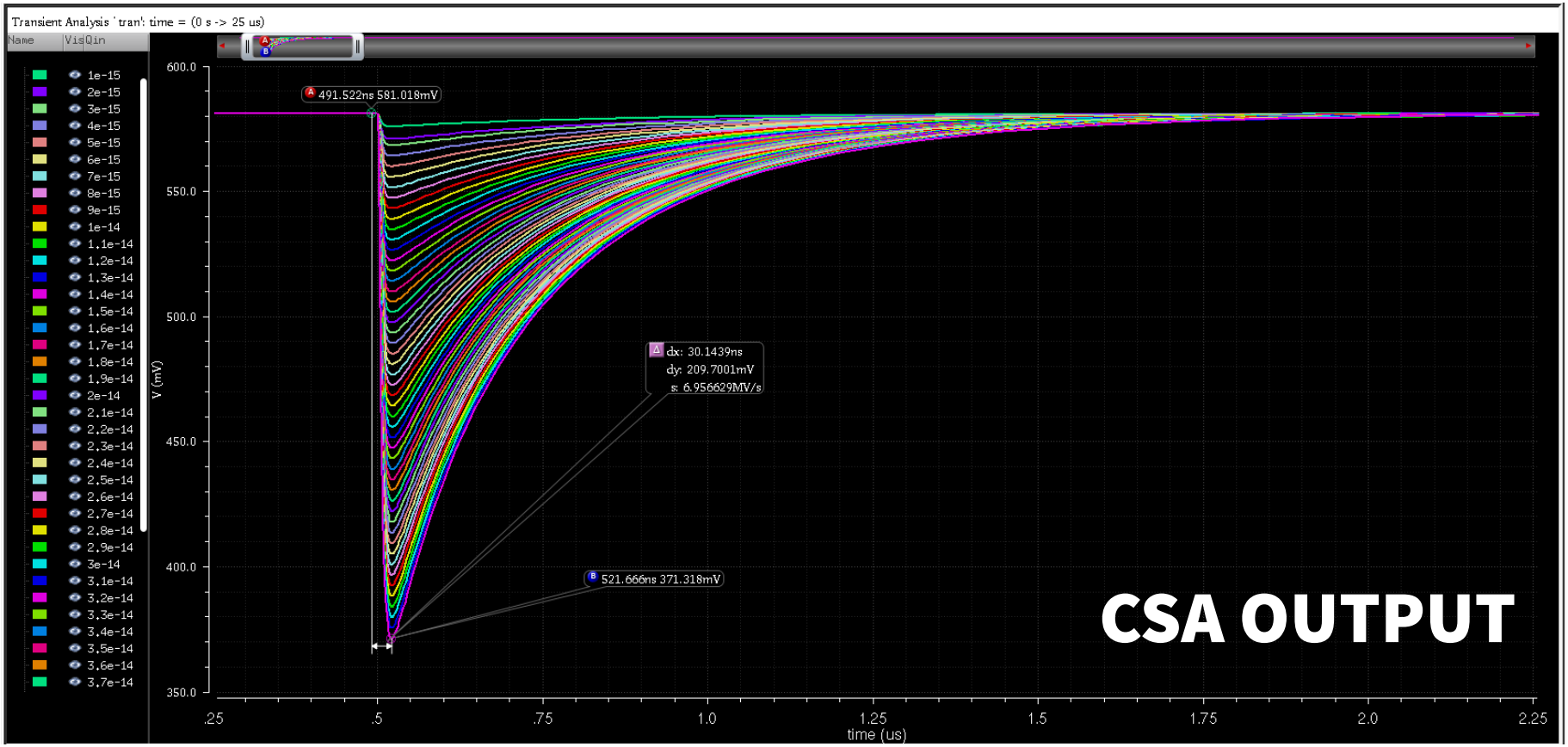
Charge sweep from 1 fC to 50 fC



CSA: sim results

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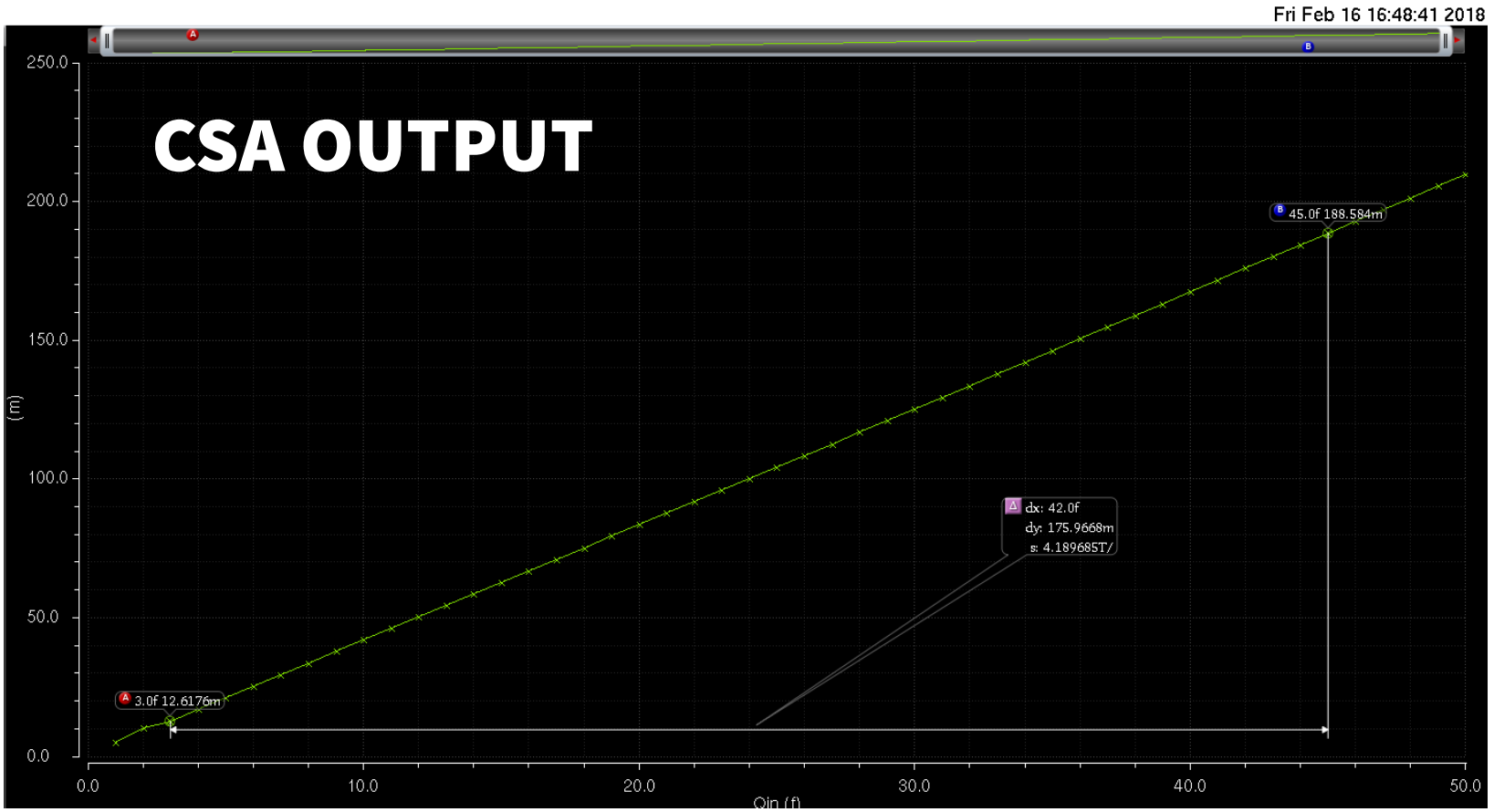
Charge sweep from 1 fC to 50 fC



CSA: sim results

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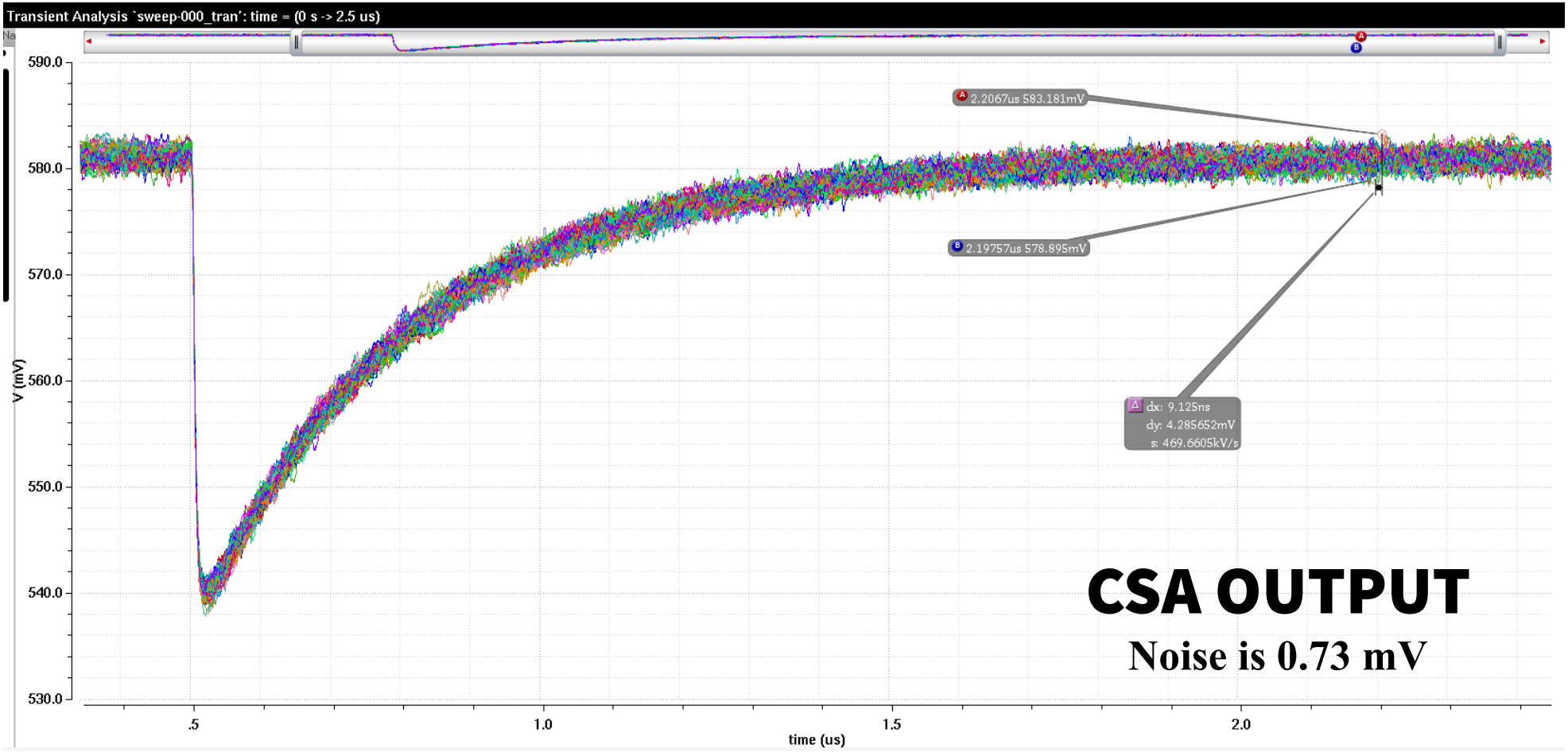
Transient noise with 20 fC input charge



The Shaper: peaking time adjustment

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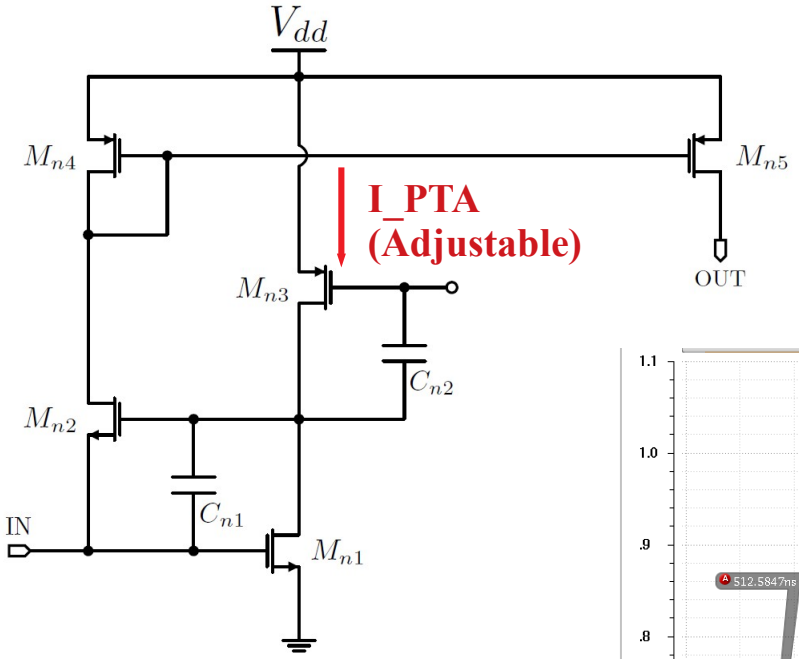
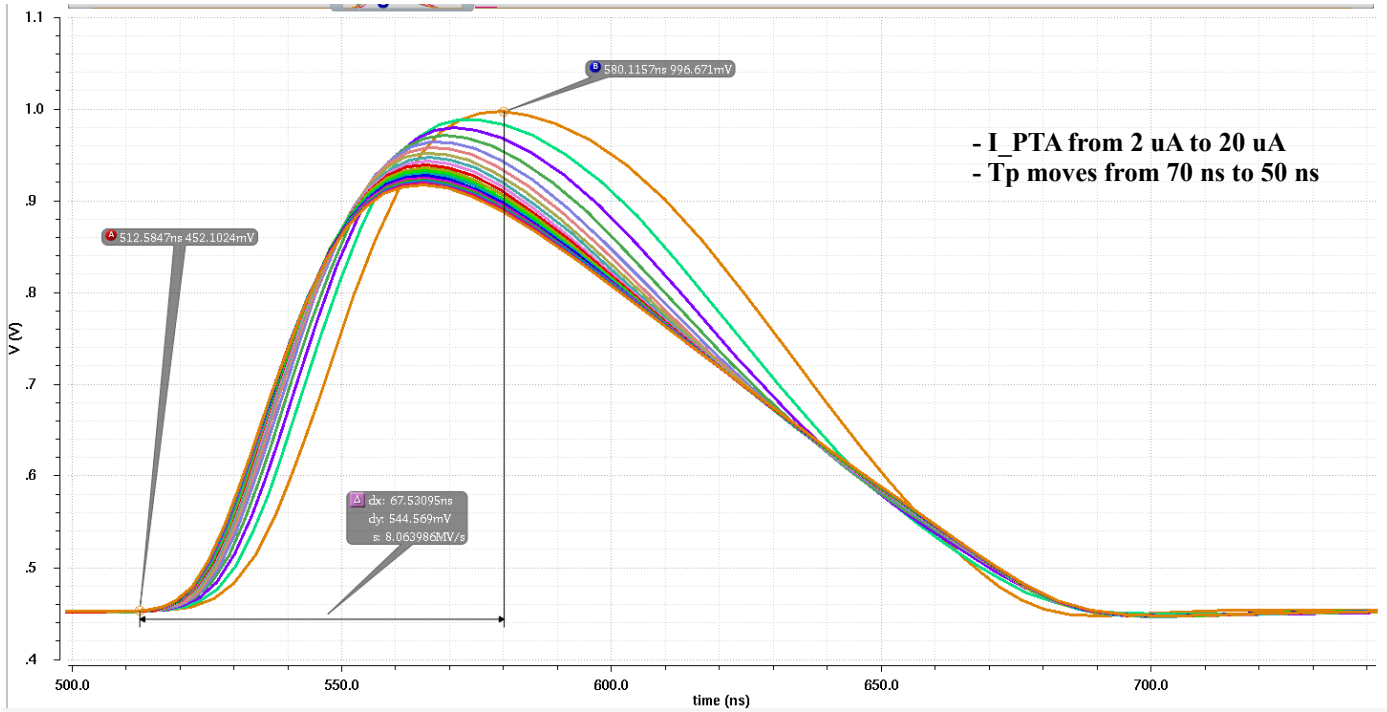


$$\frac{I_{out}}{I_{in}} = -\frac{g_{mn5}}{g_{mn4}} \frac{1}{1+s\tau_n}$$

Transfer function

$$\tau_n = C_{1n}/g_{mn2}.$$

Peaking time



If we need Tp between 200 ns and 50 ns this is not the best way to tune this parameter.

The Shaper: peaking time adjustment

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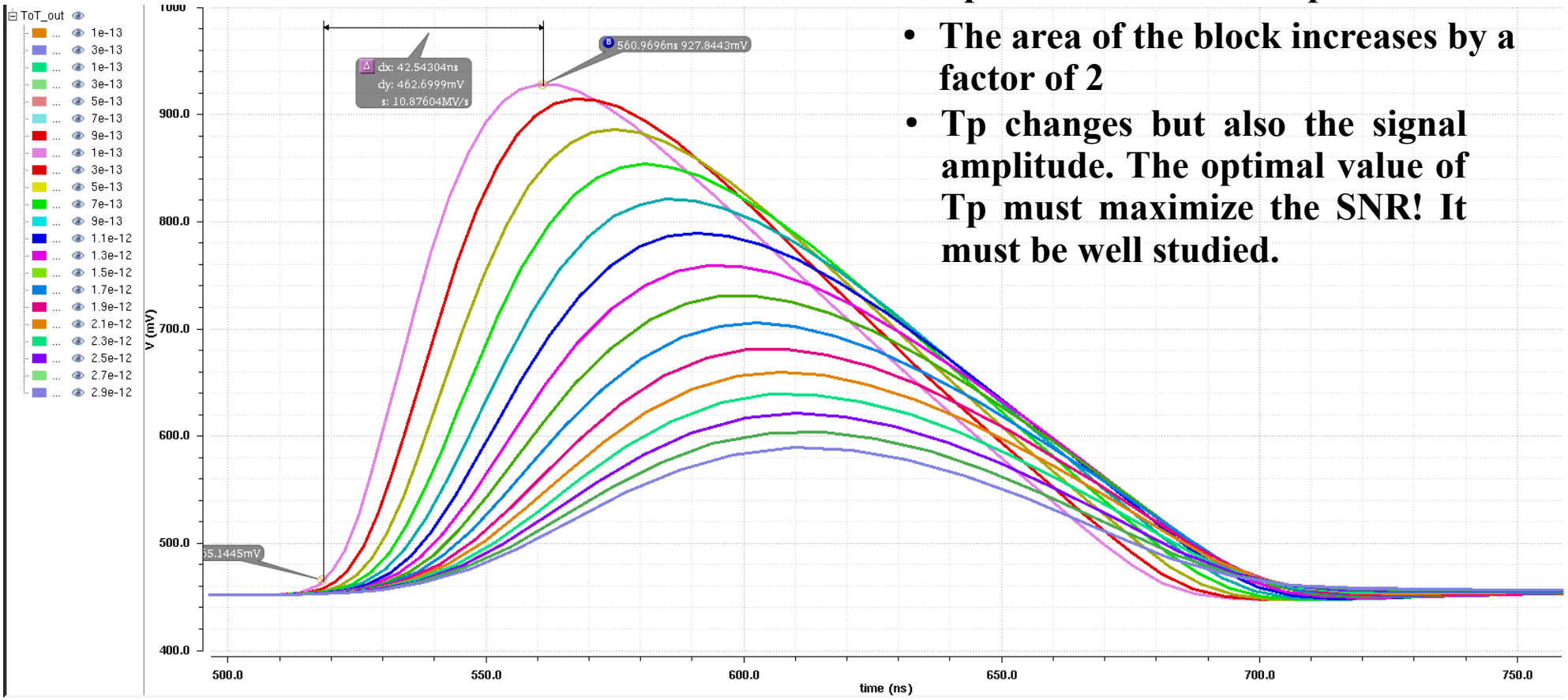
C1n: sweep from 200 fF to 3 pF



- Tp moves from 40 ns up to 100 ns
- The area of the block increases by a factor of 2
- Tp changes but also the signal amplitude. The optimal value of Tp must maximize the SNR! It must be well studied.

Full chain: sim results

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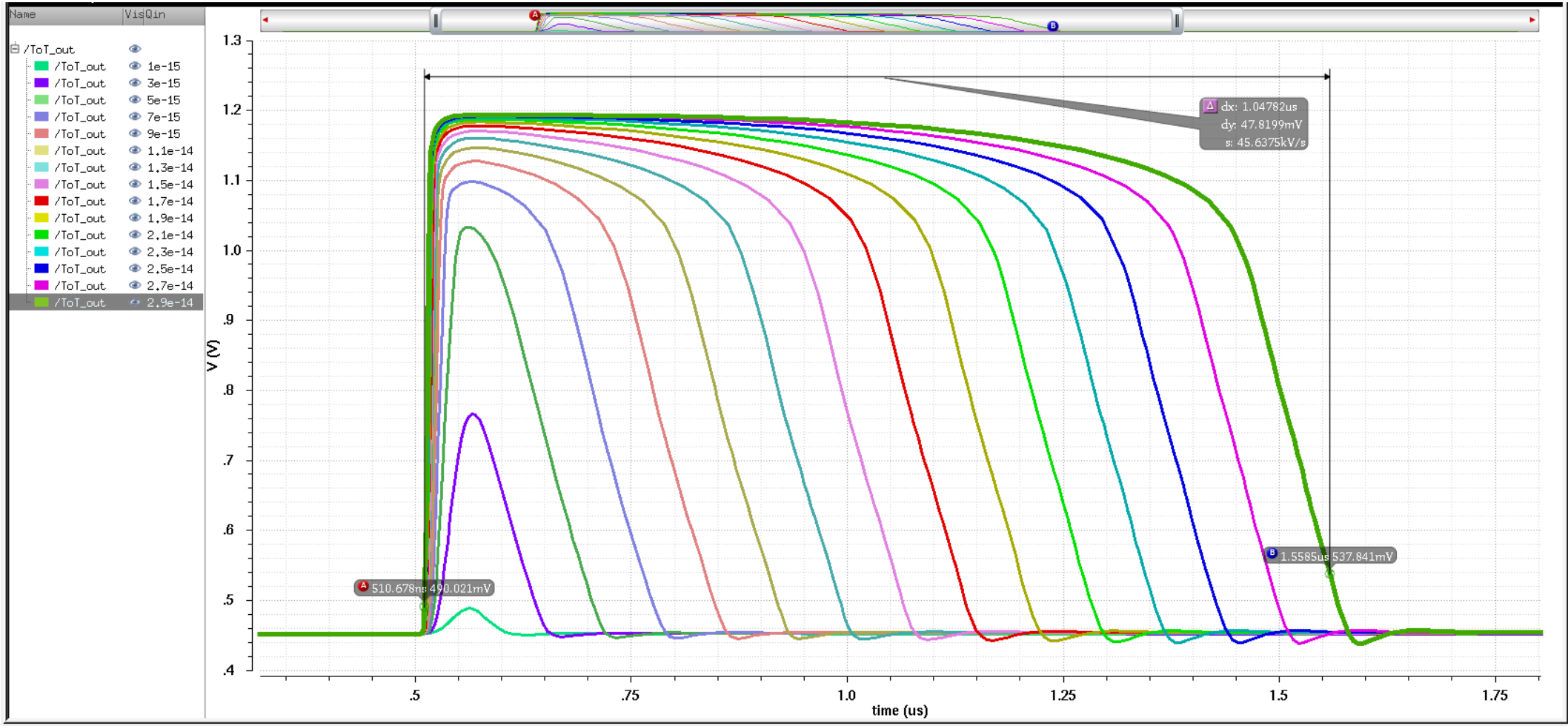
Charge sweep from 1 fC to 30 fC



Results

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- **The tested blocks (CSA, shaper, Buffer current) work as expected. Keep in mind that the simulations are still in the ideal case (schematic level + ideal currents)**
- **We have to find a good solution to adjust the peaking time (if feasible) to balance the effect of leakage current. This was not foreseen in PASTA.**

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so what's next?

- **Study the optimal peaking time to maximize the SNR**
- **Continue the simulations (at schematic level) with the other blocks (baseline holder, ToT amplifier and Disc)**
- **Check the bias cells and the global/local DACs**
- **Test more channels connected to the same bias cells. Crosstalk?**
- **Move to the post-layout verification.**