Module Controller for Strip Detector - report as of Nov. 10, 2015

- manpower after middle of November 2015: H. Sohlbach app. 10 h per week until July 2018 plus support from Giessen Group
- final goal: VHDL-based FPGA-design ready to be transfered into an digtal ASIC
- status: see status report from March 2015, for first tests with Pasta 1 -version the following test benches are in preparation:
  - pasta input, multipexing and raw data transport
  - pasta input, multipexing, basic clustering and cluster data transfer
- test benches for Pasta 1 - testing are ready until the end of 2015
- further steps / milestones will be fixed in December 2015