Istituto Nazionale di Fisica Nucleare
SEZIONE DI TORINO

READOUT ASIC for STRIPS of the MVD

Future steps for the design of the new ASIC

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The readout architecture of PASTA

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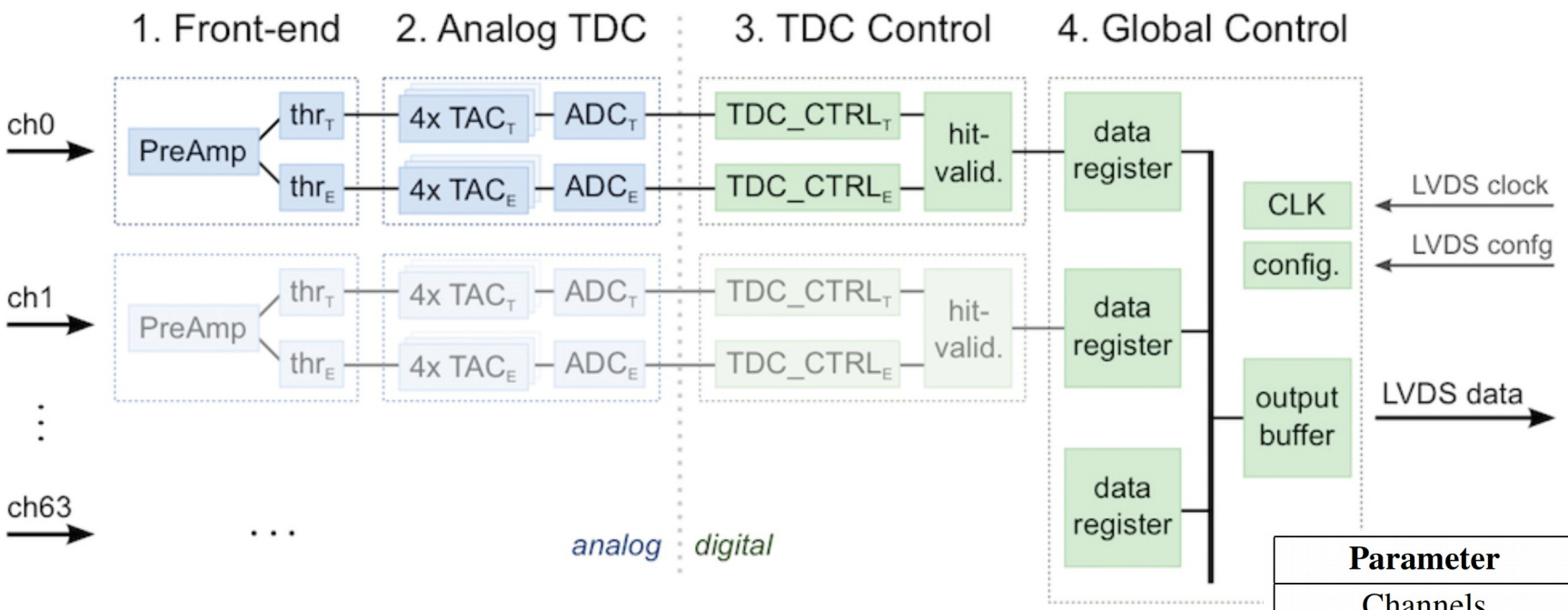

Parameter	Value
Channels	64
Input pitch	63 μm
Rate capability	100 kHz/channel
Power consumption	4 mW/channel
Front-end noise	< 600 e^-
Time bin width	50–400 ps
Charge resolution	8 bit (dyn. range)
Radiation tolerance	100 kGy

The readout architecture of PASTA

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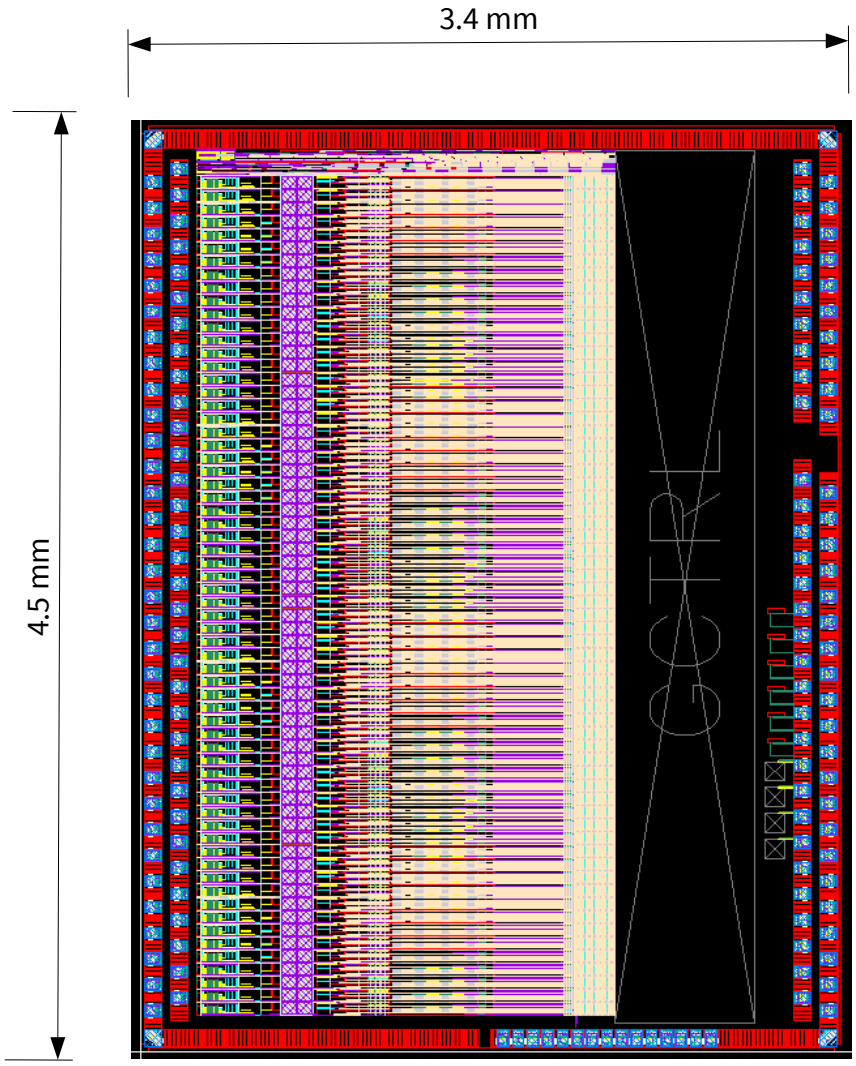

- The database of PASTA is available in Torino but some blocks are missing (last version of the Global Controller)
- I will join to the first design phase of the new readout ASIC for the strips.
- Probably most part of analog blocks can be reused with some modifications where needed.
- For the digital part the plan is to use one of the back-end digital logic under development in Torino for parallel projects or use some logic already developed for other applications.

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PARAMETER	VALUE (PASTA)	NEW VALUE	COMMENTS
CHANNELS	64	64	-
RATE CAPABILITY	100 kHz	50 kHz	Is it enough for the requirements of the MVD
Pitch	63 um	63 um	-
Power consumption	4 mW/channel	-	Is it the maximum??
Front-end noise	600 e	600 e	
Charge resolution	8 bit	-	
Time bin width	50 ps – 400 ps	-	Do we really need this time resolution?
Number of Threshold	2	-	

Design approach for the analog circuitry

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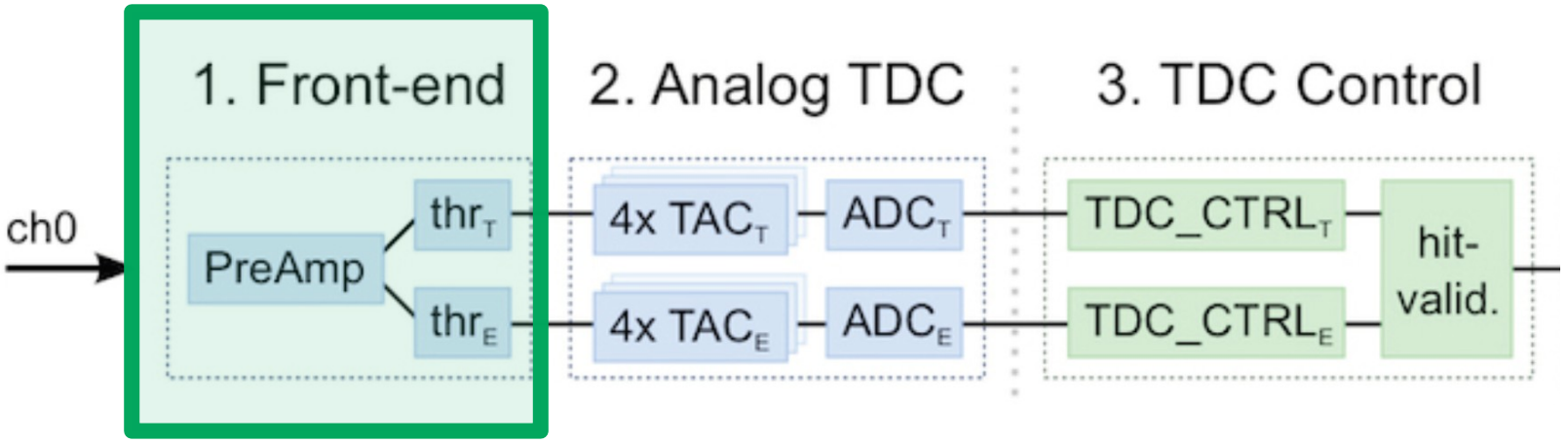

- **The very front-end can be based on the analog front-end of PASTA with modifications where needed (maybe in the DISC).**
- **The use of the TDC, depends on:**
  - The required time stamp resolution for the MVD
  - The radiation tolerance of the TDCs used in PASTA

Double threshold Discriminator

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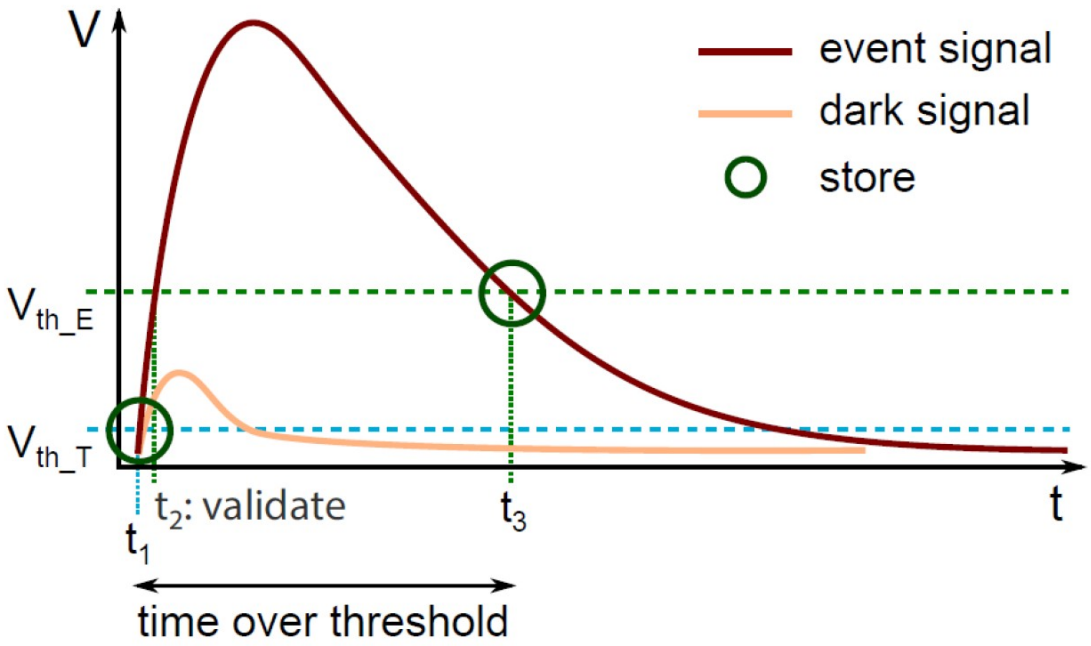

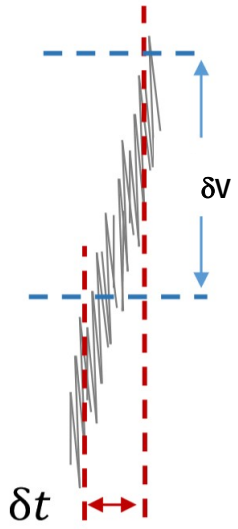

$\delta T = \delta v / SR$

- The double threshold is used to reduce the jitter of the timestamp. Do we really need it? Does anybody find problems with this second threshold?
- The experience of those who has taken part to the characterization is important at this phase to identify possible problems of those blocks

Checks on the PASTA chip

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- Check of the DC operations points of the analog blocks in the most realistic case (post layout simulations + very realistic bias + inductance introduced by wire bonding).
- Check of the bias network to study if we can use it or if we need something new.

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