

The PASTA Readout System

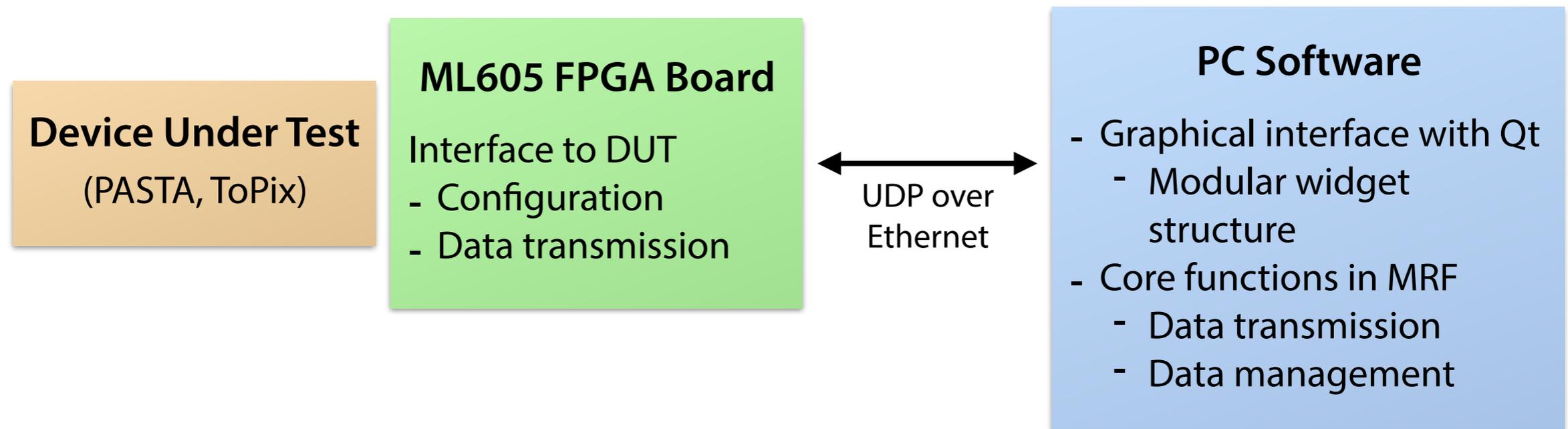
Current Status

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MVD SeeVogh Group Meeting

General Structure:



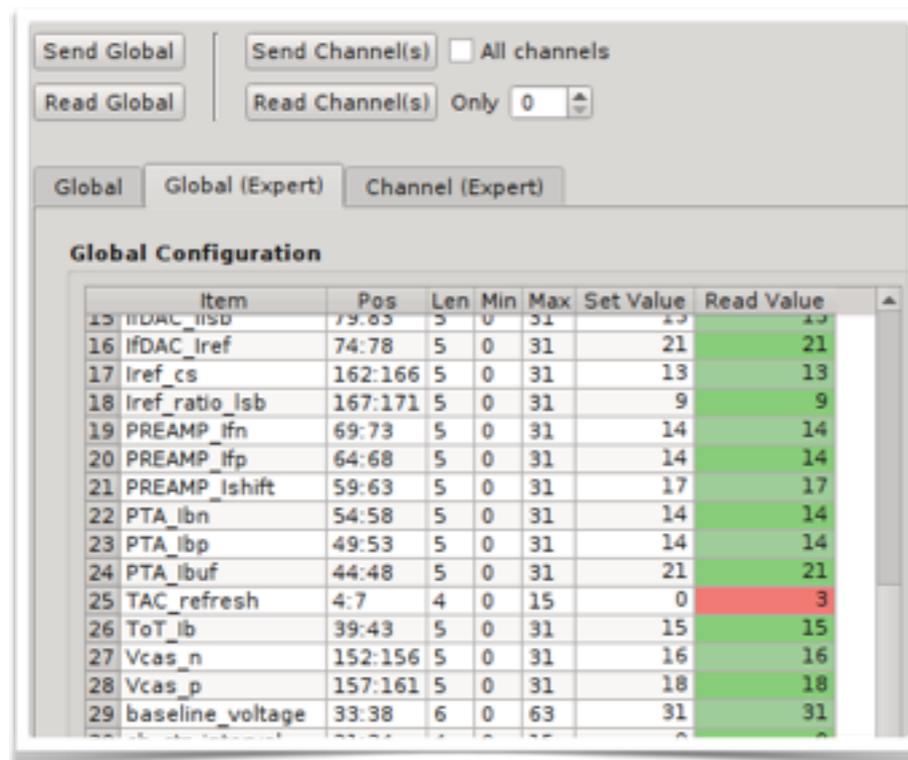
- Paradigms for the system:
 - Avoid overhead by staying as close to hardware as reasonable
 - Modular structure to »easily« adjust for new devices

Current Status Concerning PASTA

- Core system: **ready**
 - Improved register access and signal management (on FPGA)
 - Communication stable, also for high clock rates (160 MHz)
 - Benchmarks with counter data stable well above 200 MHz (*core firmware*)
 - Repository structure to enable shared development

Current Status Concerning PASTA

- Core system: **ready**
- Configuration: mostly **ready**
 - Global and channel, both send and read implemented
 - Tested with dummy response module on FPGA
 - Not yet done: enable PASTA internal test pulse configuration



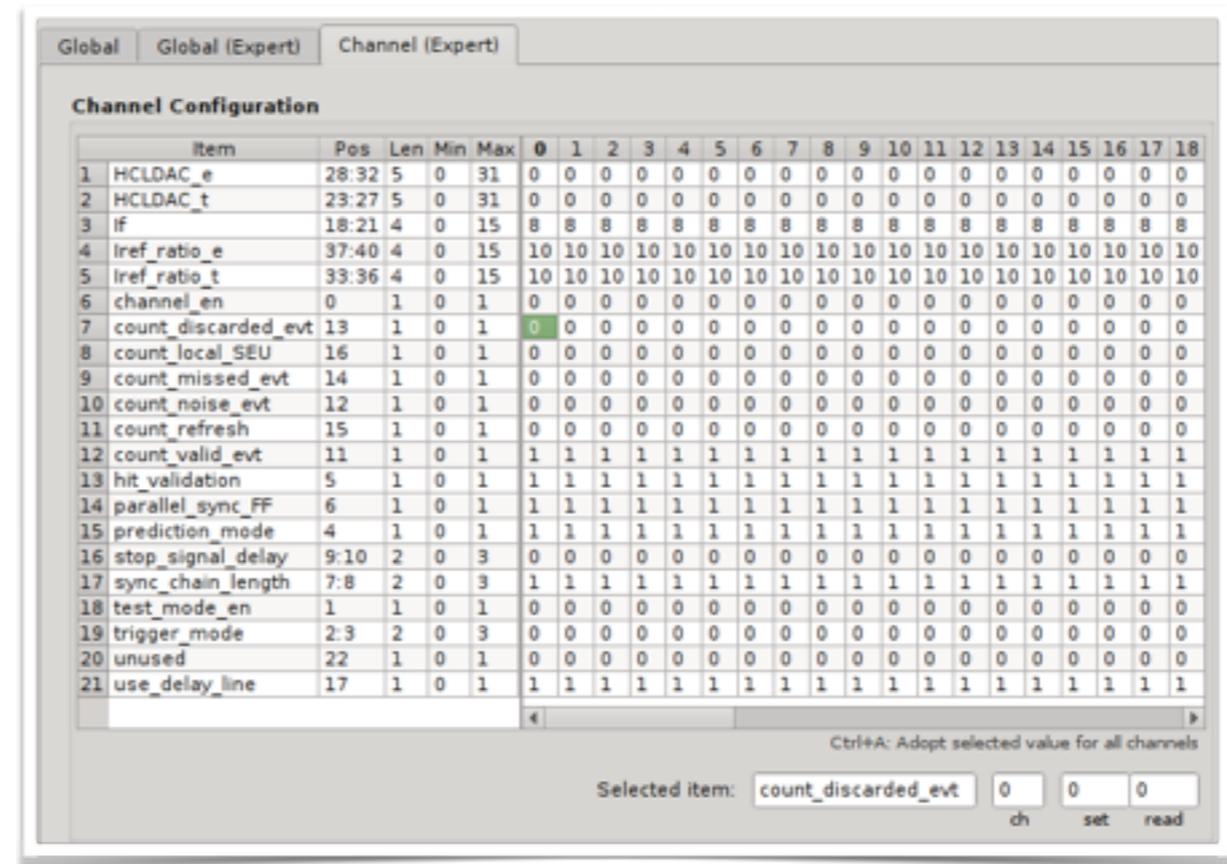
Send Global | Send Channel(s) All channels
Read Global | Read Channel(s) Only 0

Global | Global (Expert) | Channel (Expert)

Global Configuration

Item	Pos	Len	Min	Max	Set Value	Read Value
15 HCLDAC_ifsb	79:83	5	0	31	29	29
16 HCLDAC_lref	74:78	5	0	31	21	21
17 lref_cs	162:166	5	0	31	13	13
18 lref_ratio_lsb	167:171	5	0	31	9	9
19 PREAMP_ifn	69:73	5	0	31	14	14
20 PREAMP_ifp	64:68	5	0	31	14	14
21 PREAMP_ishift	59:63	5	0	31	17	17
22 PTA_lbn	54:58	5	0	31	14	14
23 PTA_lbp	49:53	5	0	31	14	14
24 PTA_lbuf	44:48	5	0	31	21	21
25 TAC_refresh	4:7	4	0	15	0	3
26 ToT_lb	39:43	5	0	31	15	15
27 Vcas_n	152:156	5	0	31	16	16
28 Vcas_p	157:161	5	0	31	18	18
29 baseline_voltage	33:38	6	0	63	31	31

Global configuration with read configuration



Global | Global (Expert) | Channel (Expert)

Channel Configuration

Item	Pos	Len	Min	Max	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1 HCLDAC_e	28:32	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2 HCLDAC_t	23:27	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3 If	18:21	4	0	15	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
4 lref_ratio_e	97:40	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
5 lref_ratio_t	33:36	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
6 channel_en	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7 count_discarded_evt	13	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8 count_local_SEU	16	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9 count_missed_evt	14	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10 count_noise_evt	12	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11 count_refresh	15	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12 count_valid_evt	11	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13 hit_validation	5	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14 parallel_sync_FF	6	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15 prediction_mode	4	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16 stop_signal_delay	9:10	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17 sync_chain_length	7:8	2	0	3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18 test_mode_en	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19 trigger_mode	2:3	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20 unused	22	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21 use_delay_line	17	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Ctrl+A: Adopt selected value for all channels

Selected item: count_discarded_evt 0 0 0
ch set read

Channel configuration

Current Status Concerning PASTA

- Core system: **ready**
- Configuration: mostly **ready**
- Event data: **under development**
 - Test data input
 - Testbench to simulate ASIC
 - Bit stream output to file, loaded in GUI
 - Send to and store in FPGA
 - FPGA data handling
 - Synchronize and decode 10b/8b
 - Buffer data in FIFO
 - Software data handling
 - Request data from FIFO
 - Store raw data in file
 - Convert data stream to usable objects

Raw data output from the 10b/8b decoder

```
Words to read: 150 Read Clear Output
Result: 150 words read
013: 0x00000001bc
014: 0x00000001bc
015: 0x00000001bc
016: 0x000000013c
017: 0x0000000004
018: 0x0000000000
019: 0x0000000000
020: 0x0000000000
021: 0x0000000001
022: 0x0000000079
023: 0x00000000dd
024: 0x0000000014
025: 0x0000000064
026: 0x0000000003
```

Legend:

- inter frame comma words
- # data words
- frame counter
- 1st event
- 2nd event

- Many improvements in the JDRS towards usability for the developer → *see also notes from Alessandra*
- Core **PASTA readout** capability **almost finished**
 - Configuration done
 - Test data capability done
 - Data receiving on the way (*until end of November*)
- Documentation / notes for developers (*until end of November*)
- **Outlook**
 - I'll **leave IKP in December**, back for **three weeks in March**
 - Connect PASTA to verify proper data handling (for me only possible in March, not before and after)