The PASTA Readout System

Current Status

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MVD SeeVogh Group Meeting

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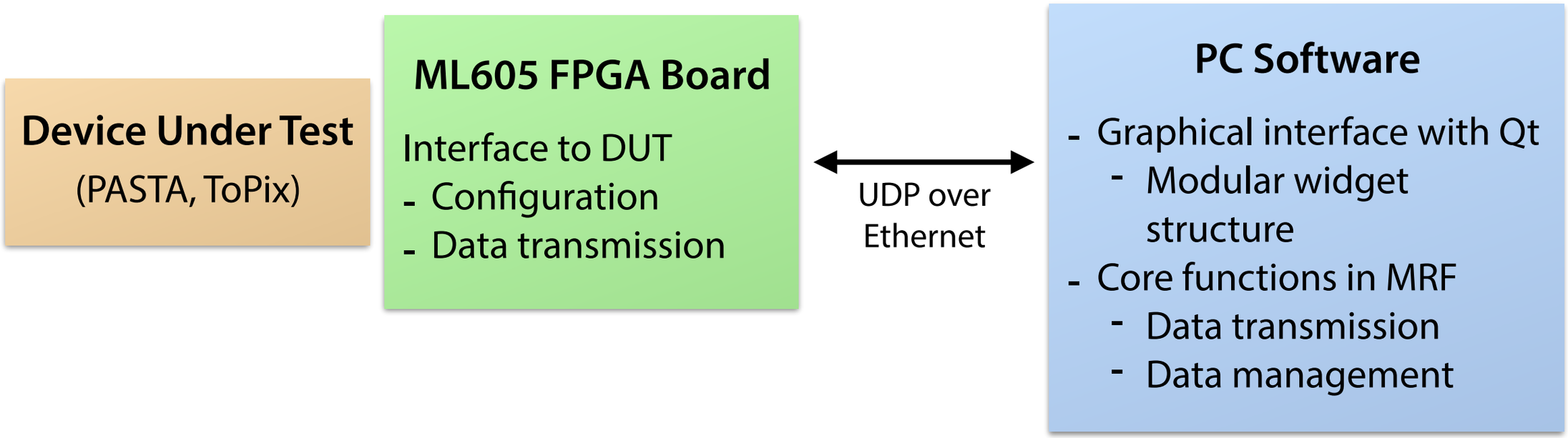
Jülich Digital Readout System

General Structure:



- Paradigms for the system:
  - Avoid overhead by staying as close to hardware as reasonable
  - Modular structure to »easily« adjust for new devices

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Current Status Concerning PASTA

- Core system: **ready**
  - Improved register access and signal management (on FPGA)
  - Communication stable, also for high clock rates (160 MHz)
    - Benchmarks with counter data stable well above 200 MHz (*core firmware*)
  - Repository structure to enable shared development

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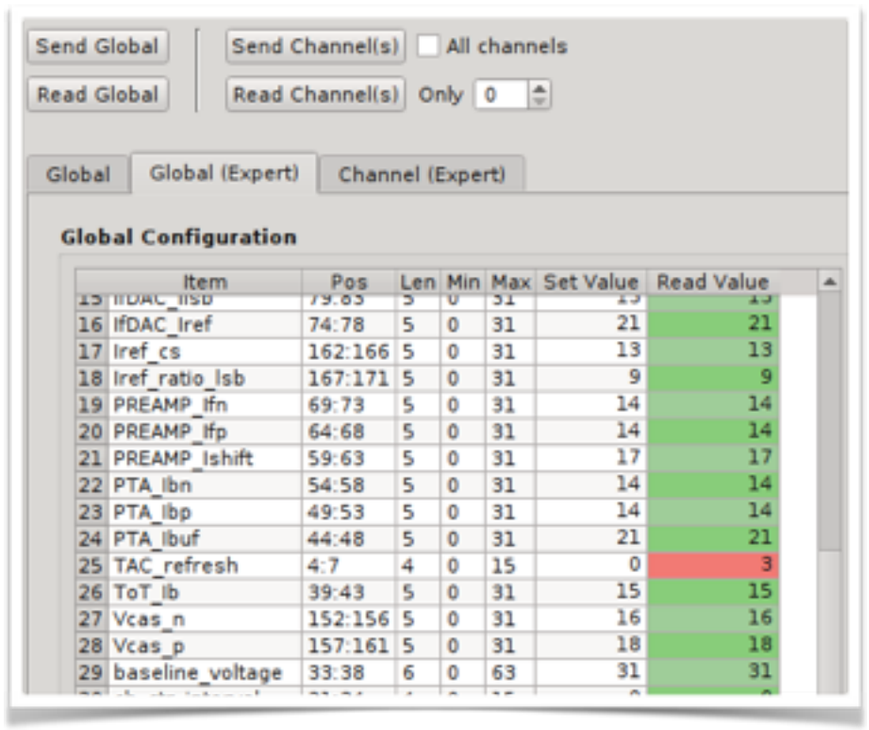
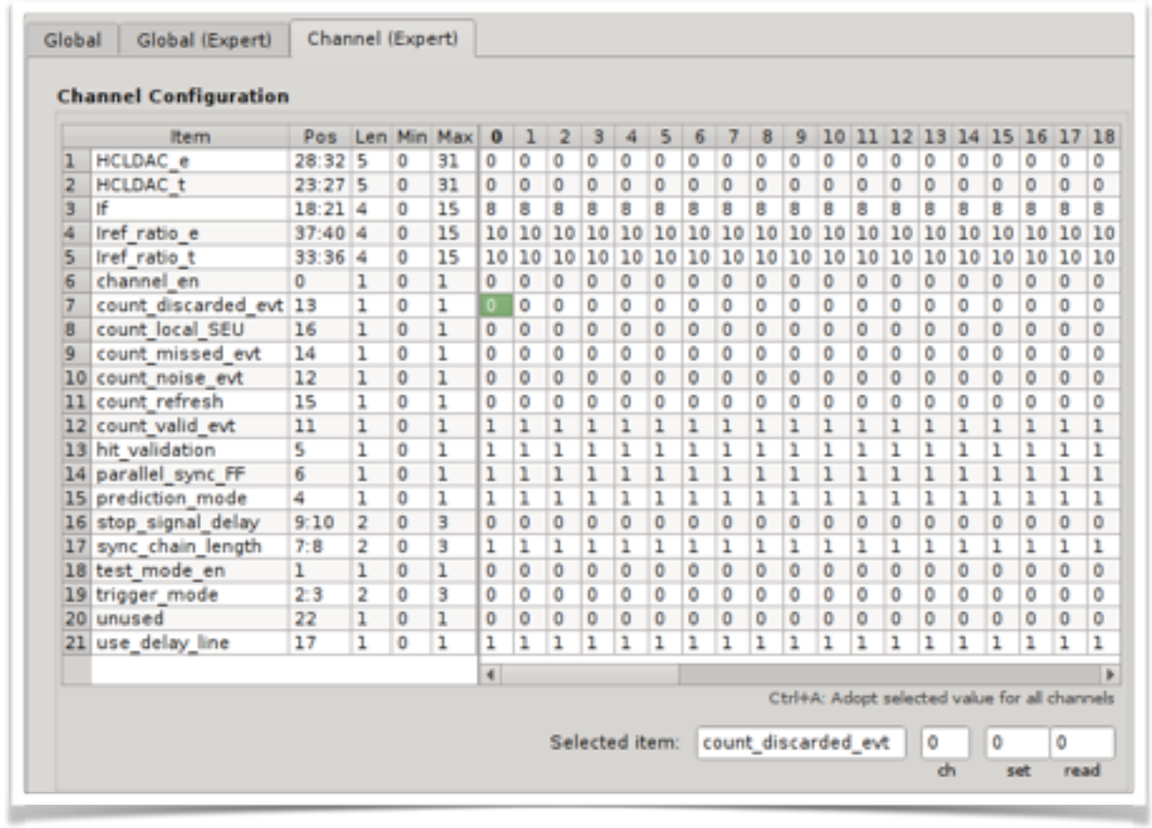
Current Status Concerning PASTA

- Core system: **ready**

- Configuration: mostly **ready**
  - Global and channel, both send and read implemented
  - Tested with dummy response module on FPGA
  - Not yet done: enable PASTA internal test pulse configuration



Global configuration with read configuration



Channel configuration

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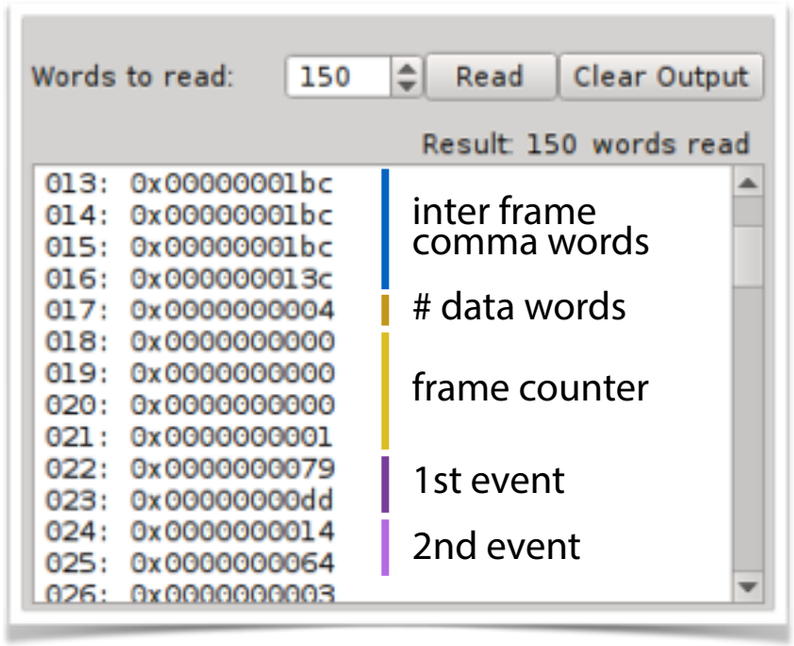
Current Status Concerning PASTA

- Core system: ready
- Configuration: mostly ready
- Event data: under development
  - Test data input
    - Testbench to simulate ASIC
    - Bit stream output to file, loaded in GUI
    - Send to and store in FPGA
  - FPGA data handling
    - Synchronize and decode 10b/8b
    - Buffer data in FIFO
  - Software data handling
    - Request data from FIFO
    - Store raw data in file
    - Convert data stream to usable objects

Raw data output from the 10b/8b decoder



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Conclusion & Outlook

- Many improvements in the JDRS towards usability for the developer → *see also notes from Alessandra*
- Core PASTA readout capability almost finished
  - Configuration done
  - Test data capability done
  - Data receiving on the way (*until end of November*)
- Documentation / notes for developers (*until end of November*)

- **Outlook**
  - I'll leave IKP in December, back for three weeks in March
  - Connect PASTA to verify proper data handling
    (for me only possible in March, not before and after)

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