JÜLICH
FORSCHUNGSZENTRUM

Developments for the PANDA STT at Forschungszentrum Jülich

- Situation analysis
- Readout system for pulse form analysis and feature extraction
- Developments for a possible final system with MicroTCA
- Readout system and results with MSGCROC

19. April 2011 | ZEL + IKP, Forschungszentrum Jülich; IFJ PAN Krakow

What is the situation now?

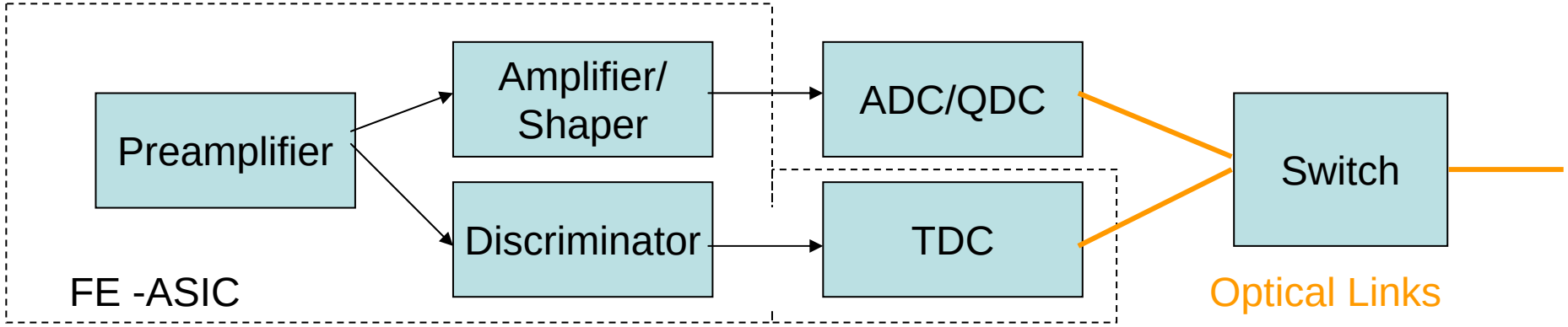
- Still no decision between STT and TPC for PANDA central tracker

=> STT team has to prove 2 things:

1. “Physics aspect”: It is possible to measure drift time **and** energy loss (dE/dx) with straw tubes (using “Lab electronics”)
2. “Engineering aspect”: It is possible to build reasonable electronics, that fulfills 1.

- Time is pressing => three parallel activities using existing electronics
  1. JU Krakow: Measure time over threshold with HADES electronics (TRB)
  2. FZ Jülich + IFJ PAN Krakow: Analysis of pulse form + feature extraction with sampling ADCs + TDCs from WASA (P. Kulessa paper)
  3. FZ Jülich: Feasibility study with AGH-MSGCROC ASIC (charge measurement & time stamping)
- AGH Krakow supports these acitivities by FE ASIC development

What has to be done in future



- Define (and develop?) FE-ASIC
  - MSGCROC or “New AGH ASIC” (Przyborowski,Idzik)
- Define a feasible readout system (e.g. Hades electronics + improvements + extensions)
- Think (internally!!!) about an optimized final system (ATCA, MicroTCA,…???)
- Start collecting requirements regarding cabling, mechanics, cooling, radiation hardness,……

Readout electronics for pulse analysis / feature extraction

- Unclear pulse forms (cluster structure)
- Charge information sufficient for dE/dx?

=> use fast sampling ADC in oscilloscope mode; implement QDC and TDC functionality on FPGA. Use additional TDC for comparison

- Improvement of **existing WASA electronics** in cooperation between ZEL and University of Uppsala
- **But: WASA electronics will definitely not be used in the final system**
- Measurements and pulse form analysis by IKP and IFJ PAN Krakow

=> paper by Pawel Kulessa

WASA electronics: Crate standard + Optical Uplink

- Proprietary Backplane
- Physical layer: SCSI
  - LVDS
  - ERmet ZD connectors
- 8 address bits
- 16 data bits
- 40 MHz

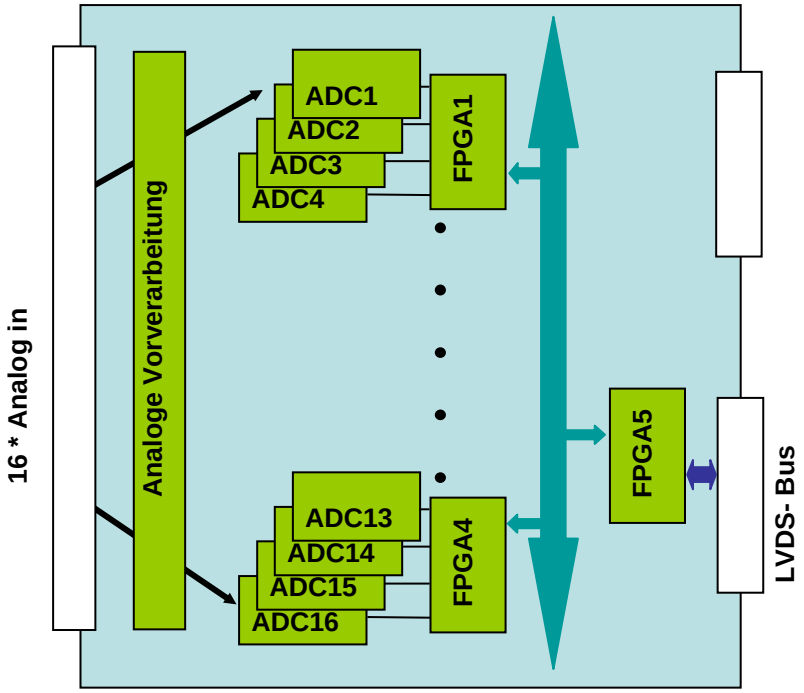
=> block transfer: 80 Mbytes/s

- Single master system:

  Crate Controller with Optical Uplink
  - Up to 2 * 2 GBit/s

WASA QDC electronics

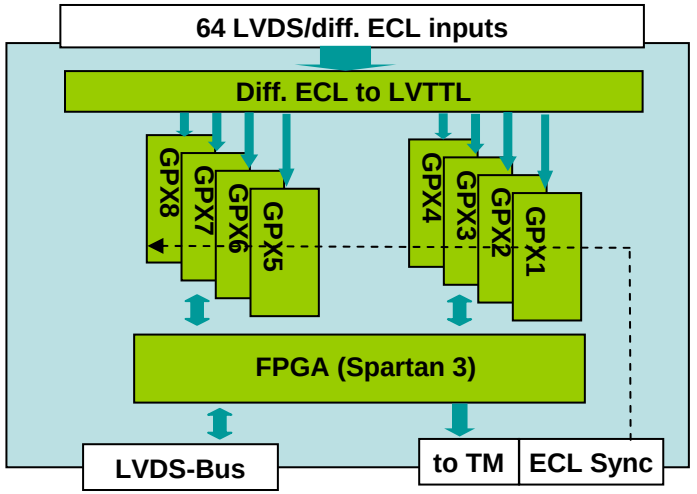
- Free-running sampling ADCs (12 Bits)
- Three versions: 80 MHz, 160 MHz, 240 MHz
- History Buffer: 12 µs
- FPGAs – massively parallel computational power in hardware:
  - Integration
  - Time stamping
  - Baseline-Subtraction,
  - Pileup-Detection
- list mode option

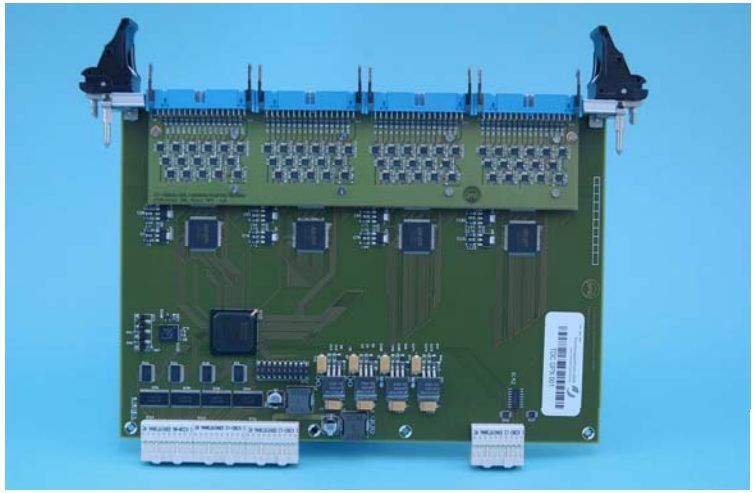


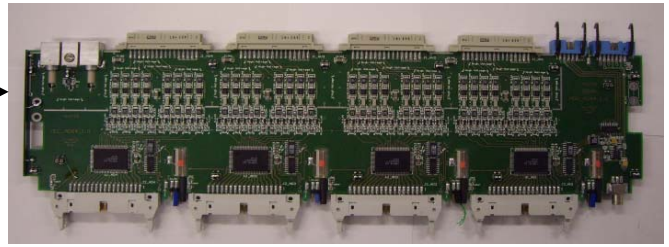
Discrete preamp from Krakow used during straw tests

WASA TDC electronics

- Old version based on F1 ASIC , new version based on GPX ASIC from *accam messelectronic gmbh in I-Mode:*
  - 8 channels, LVTTL Inputs
  - 81 ps resolution (typ.)
  - Double pulse resolution: 5,5 ns
  - Depth of Hit-Fifo: 32
  - Continuous rate/channel: 10 MHz
- Trigger matching unit in FPGA
- 8 ASICs => 64 channels (ECL or LVDS)
- FE-Electronics based on CMP16 (developed in Krakow?)







MicroTCA developments for the PANDA STT

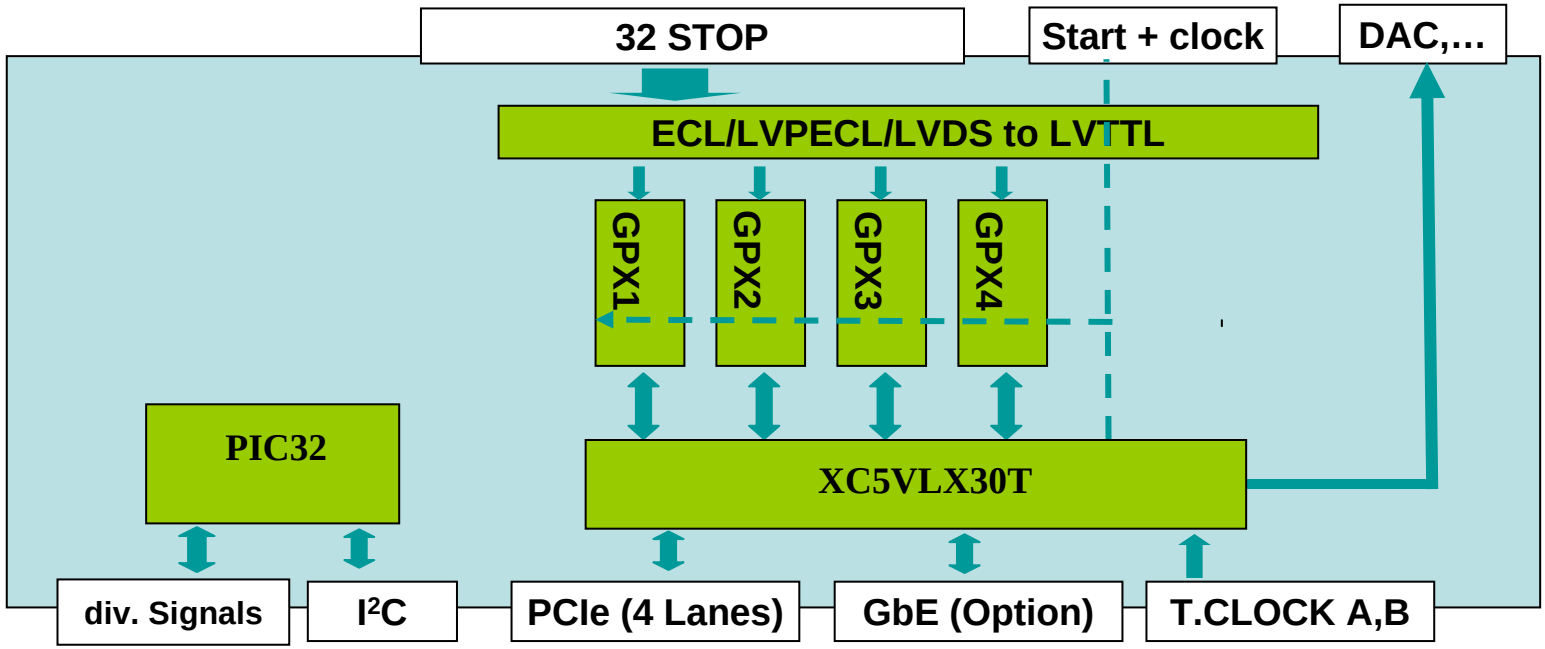
- Implementation Option: FE-Electronics inside detector, connected by cables to QDC and TDC boards outside detector (number/size of boards,……)
- MicroTCA + ATCA: scalable architecture based on modern technologies (high speed serial links on backplane, management,….)
- Pragmatic Approach: Start PANDA developments with MicroTCA to get a smooth start
  - „low cost“ lab and test systems
  - Development results directly usable for ATCA

- Investment in MicroTCA pilot installation
  - Development environment
  - Mulitivendor test system
  - Crates, CPUs, MCHs, storage modules, graphics modules, peripheral boards from different vendors

Development of a MicroTCA TDC Module

- Use the GPX ASIC (well known from WASA developments)
- FPGA: Xilinx XC5VLX30T with FF665 package
- Start with a moderate channel number: 32 chanels
- Double width, compact size module
- Implement AMC.1
  - Implementation of 4 lane PCIe using the „embedded PCIe endpoint“
  - Connect AMC ports 4 – 7 to Virtex 5 GTP_Dual_Tiles X0Y3 und X0Y2. Use FCLKA as reference clock.
- Additionally: Connect AMC port 0 to GTP_Dual_Tile X0Y0
  - ⇨ GbE possible by using the „embedded MAC core“
- No private rear IO ⇨ DAC control only via front connector
- Clock und start signals from front connector
- Use card edge connector instead of commercial connector (Harting,..)

Module architecture



- Implementation of MMC (Module Management Controller) on Microchip PIC32MX460F512L microcontroller with 2 integrated I^2C interfaces
- Open Source ***www.coreipm.com*** is used

Status

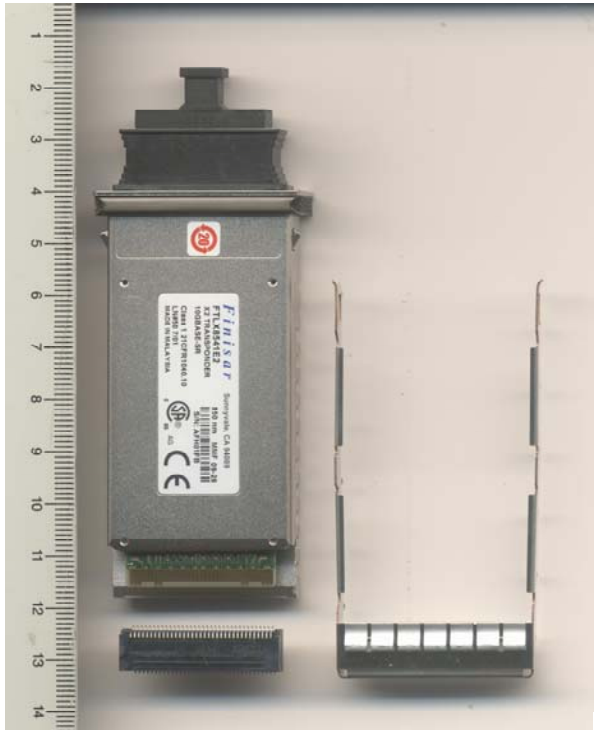
- HW-Test
  - Microcontroller part works
- MMC software:
  - under development
- Still open:
  - FPGA code
- Future: CERN HPTDC under discussion for WASA DIRC => Later module version with HPTDC possible

Development of Optical Uplink-Module

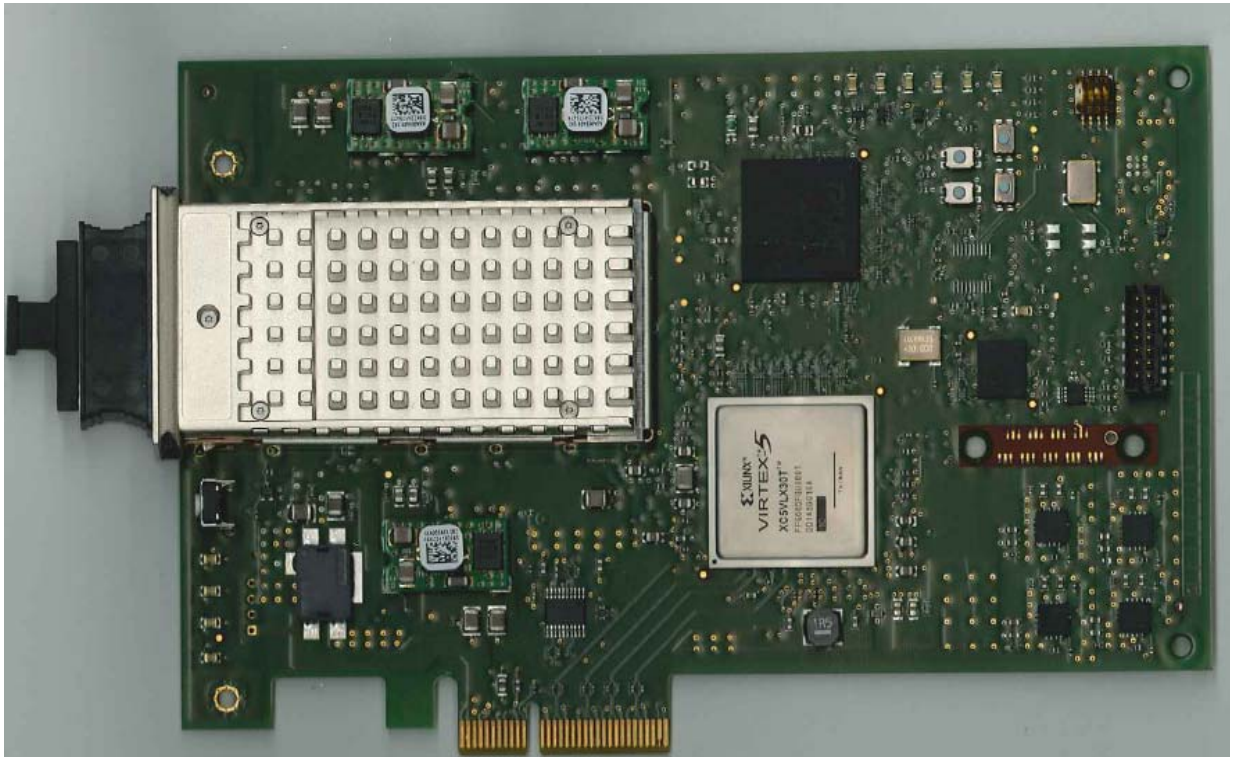
- Nominal bandwidth per MicroTCA slot: 8 Gigabit/s (4 PCIe lanes)

=> Requirement for uplink: 10 Gbit/s

- Reuse management, backplane interface and FPGA from TDC module
- Avoid 10 GigaBit/s on PCB (8B/10B-Codierung => 12,5 GHz)
  - ⇨ Use **XAUI interface** (4 * 2,5 GBit/s)
  - ⇨ Use X2 transceiver Modul **FTLX8541E2**
- Synchronization of Vertex5 MGT-Ports?
  - ⇨ USE Parallel-to-XAUI SERDES:
    PM8358 , well known from QPACE project
    (QCD-machine based on cell processor)

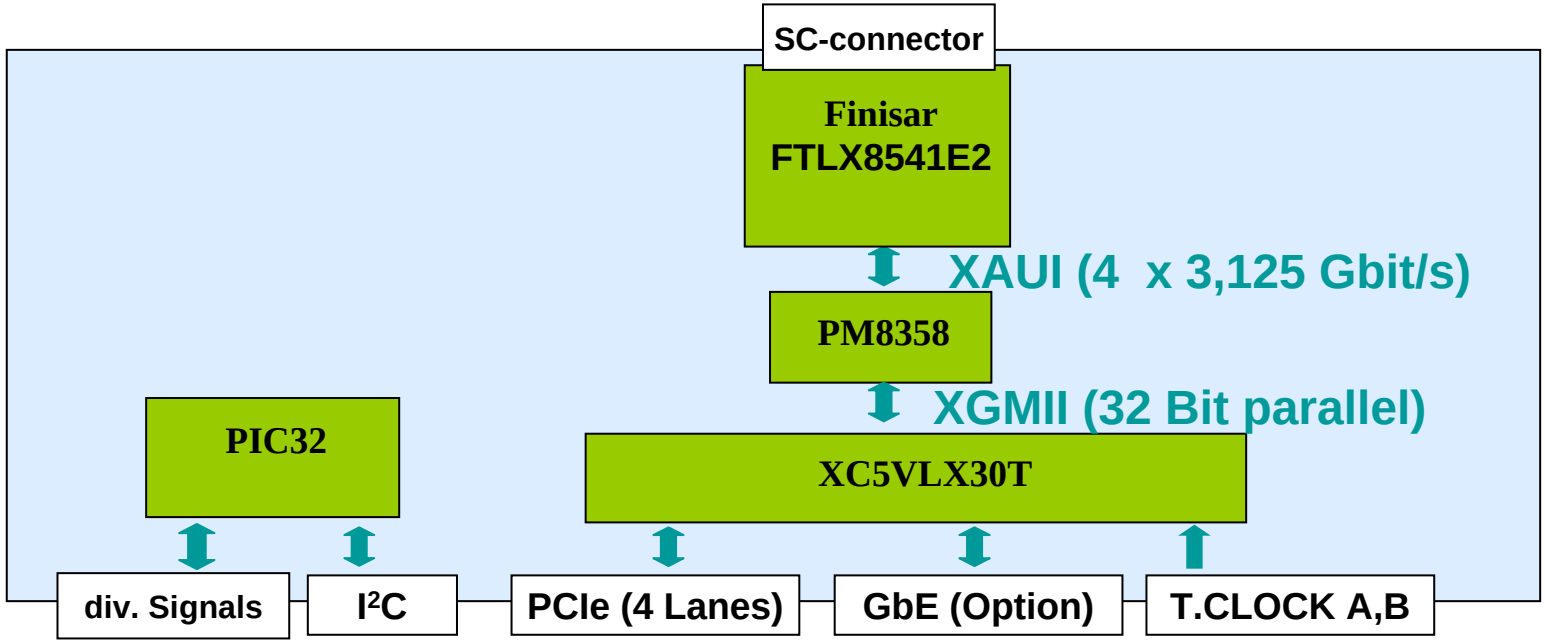


PCIe board for the 10G optical uplink



- Status:
  - First Protoype available
  - No hardware tests
  - No FPGA code

MicroTCA Board for the 10G optical uplink



- Status: schematics almost complete
- Can also be used in the new modular version of the Compute Node

Future activities regarding MicroTCA

- Decision for STT and the general concept required
- Developments only make sense for the “New AGH ASIC”
- QDC board has to be developed
- New version of TDC board (more channels, HPTDC?)
- Performance considerations => system partitioning?
- Still a long way to the final system
- Sharing of development effort?