Concepts for Pre-Assembly Data Acquisition for the $\overline{\text{P}}$ANDA Experiment

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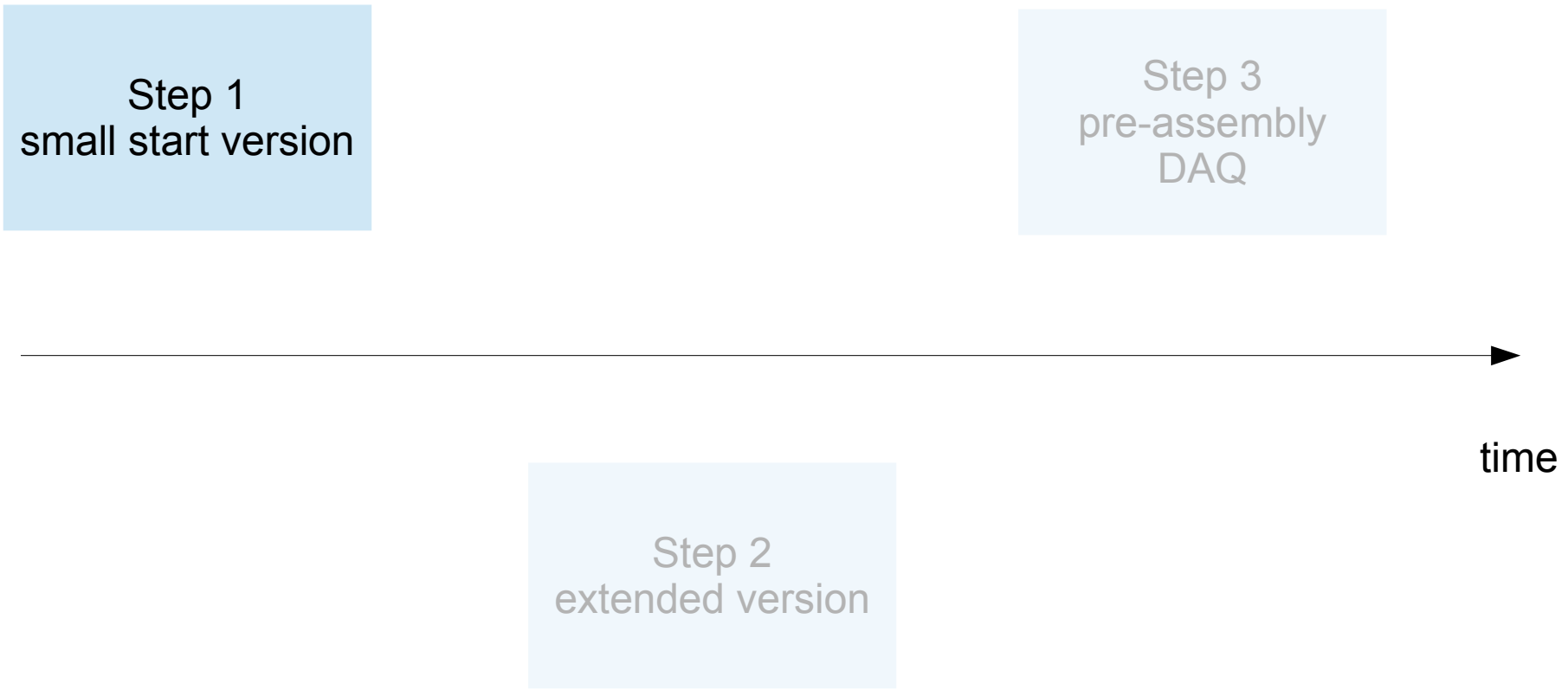
What We want to Achieve?

- Full pre-assembly data acquisition
  - Similar hardware to $\overline{\text{P}}$ANDA DAQ
  - Full functionality
    - Online event reconstruction
    - Online event building
    - Software triggering

Three Steps Concept



First Step

- Small but scalable start version
- Parts of the functionalities
- Similar hardware

Prototype Trigger-less Data Acquisition (PTDAQ)

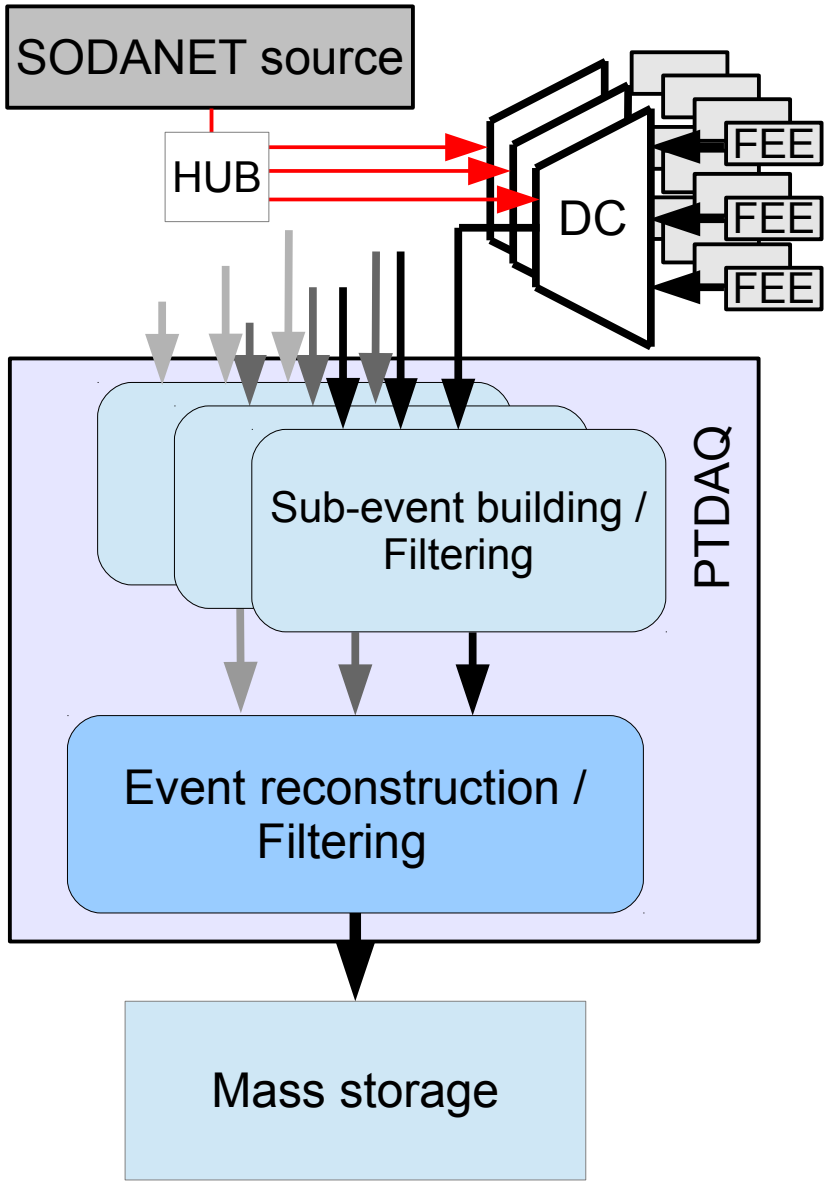
Used for testing:

- Synchronization of data acquisition (SODANET)
- Sub detector prototypes
- Reconstruction algorithms
  - Yutie Liang
    - FPGA Helix Tracking Algorithm for $\overline{\text{P}}$ANDA
- Current hardware

Differences to the $\overline{\text{P}}$ANDA DAQ:

- No connection between sub-event building boards via backplane
- Smaller interaction / data rate

PTDAQ Concept

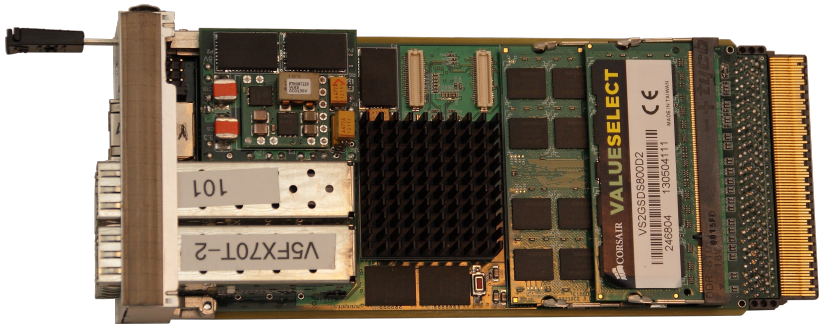


Functionality:

- Digitalized data front end electronic synchronized at data concentrator
- Sub-event building and first filter algorithm
- Event reconstruction and second stage of filter algorithm

Data concentrator (DC)
Front end electronic (FEE)

PTDAQ Setup

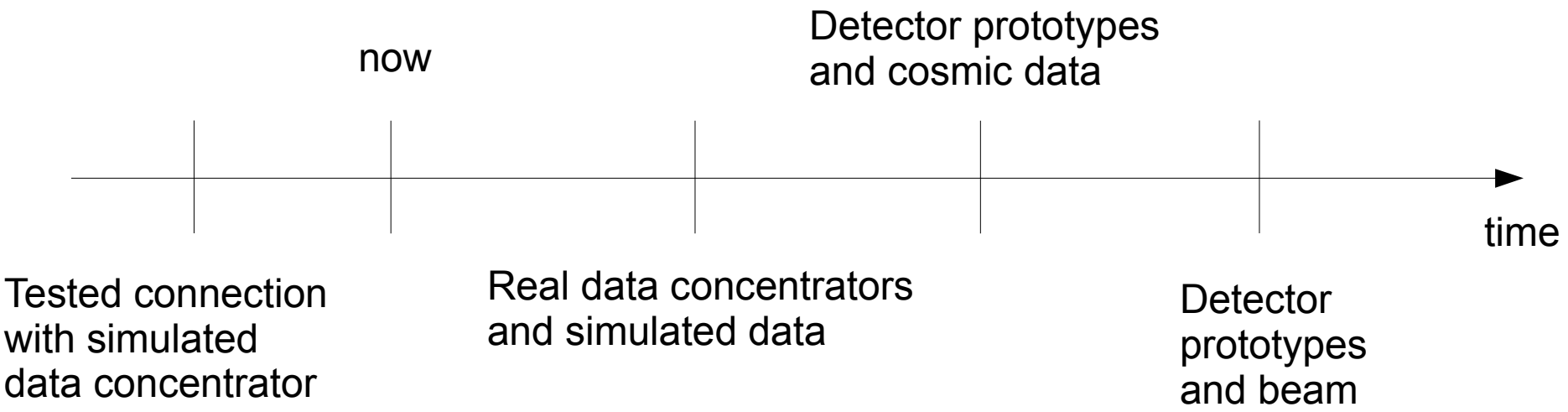


xTCA compliant board:

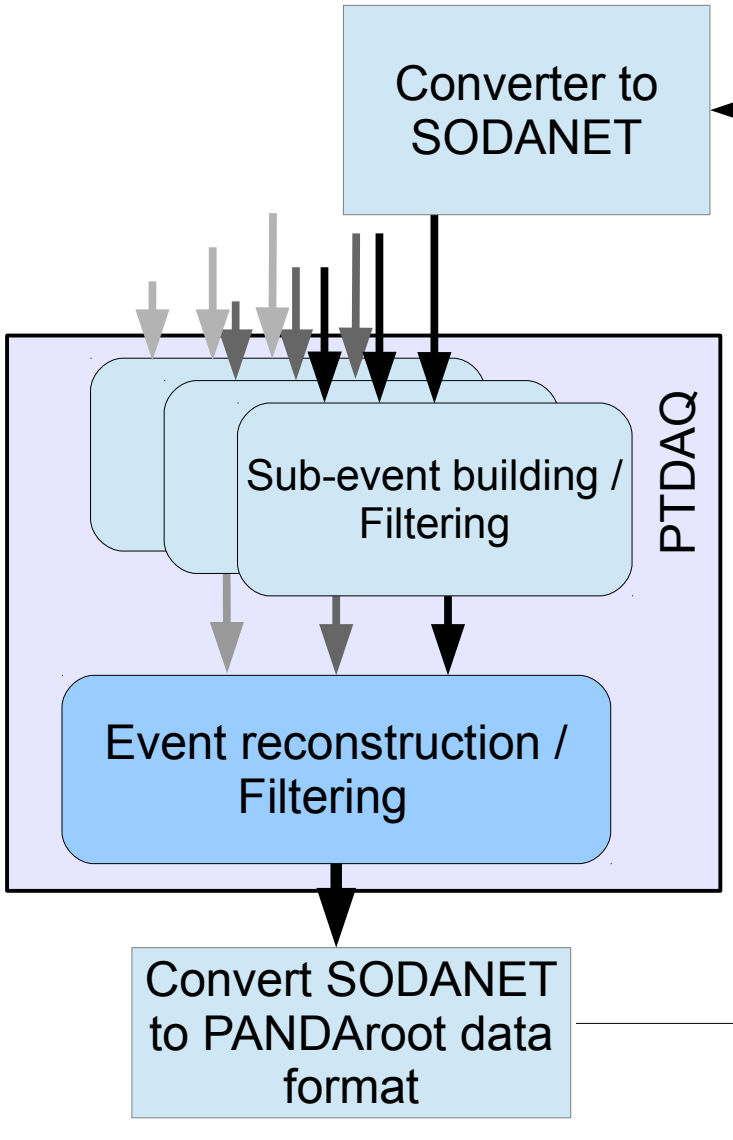
- AMC form factor
- Xilinx Virtex 5FX70T-2
- 2 x 2 GB DDR2
- 4 SFP+ interfaces
  - 6.25 Gbit optical
- 1 Gb Ethernet

- Micro TCA shelf:
  - Up to 4 x xTCA compliant boards
  - Up to 9 x data concentrators

PTDAQ Time Line

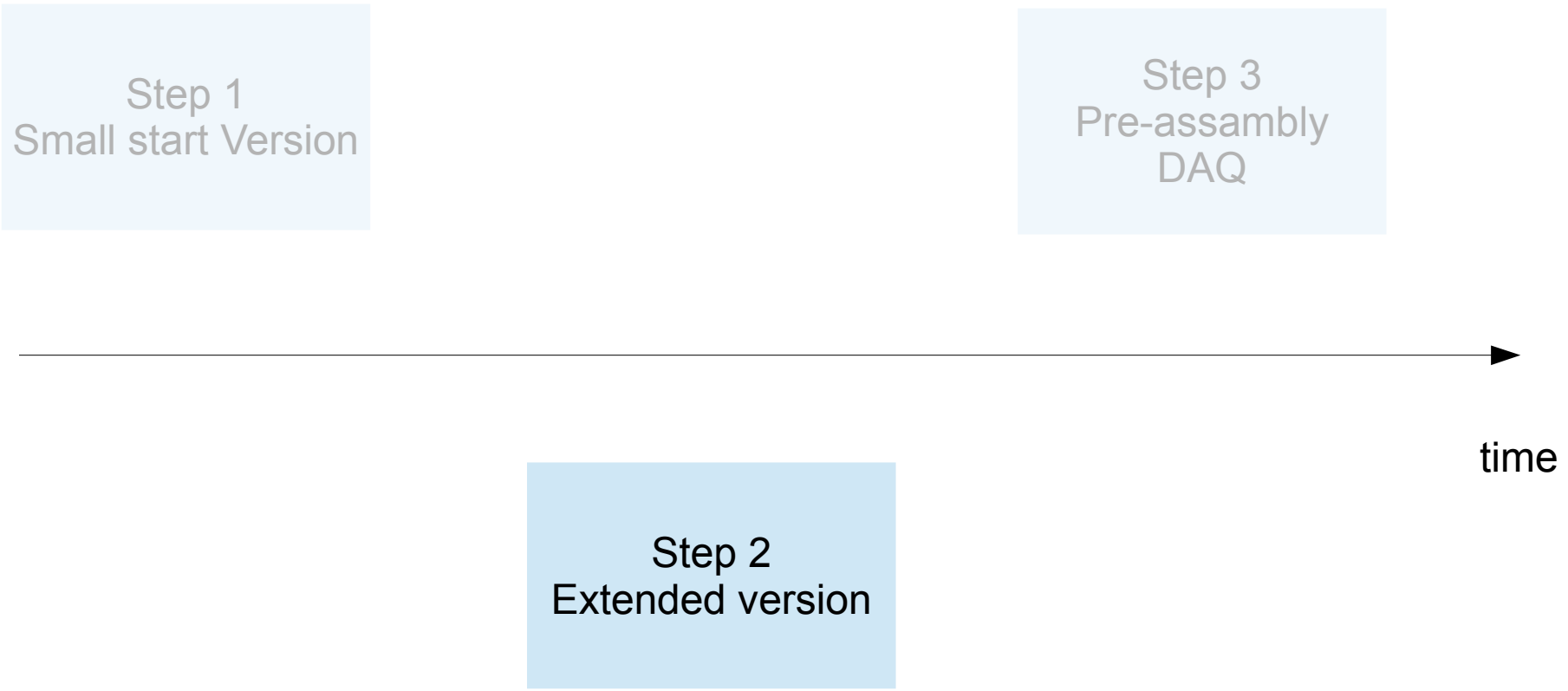


PTDAQ Test System



- Reading PANDA Root data and building into SODANET data format (Christopher Hahn)
- Reading SODANET data format and converting in into root data files (Sören Fleischer)

Three Steps Concept



Second Step

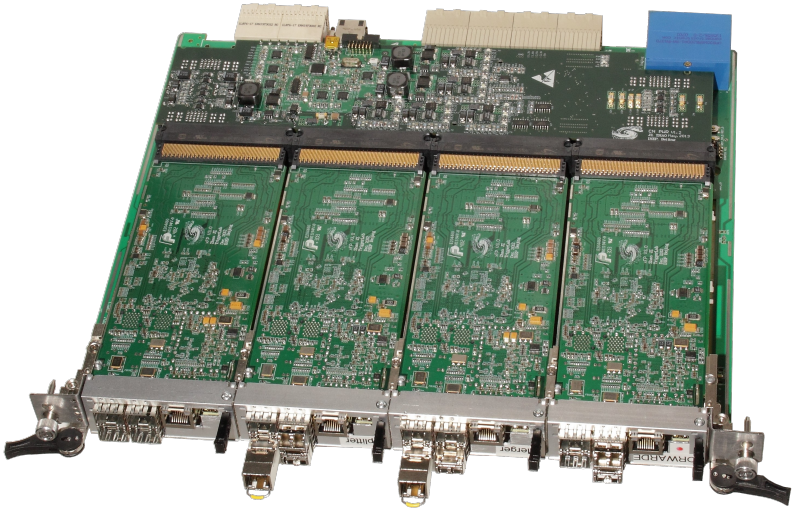
- MicroTCA shelf → Compute Node
- Include connection between sub-event building boards

  → Increasing the number of data concentrators

  → Include the data transport mechanism

  (Sören Fleischer)

Compute Node (CN)

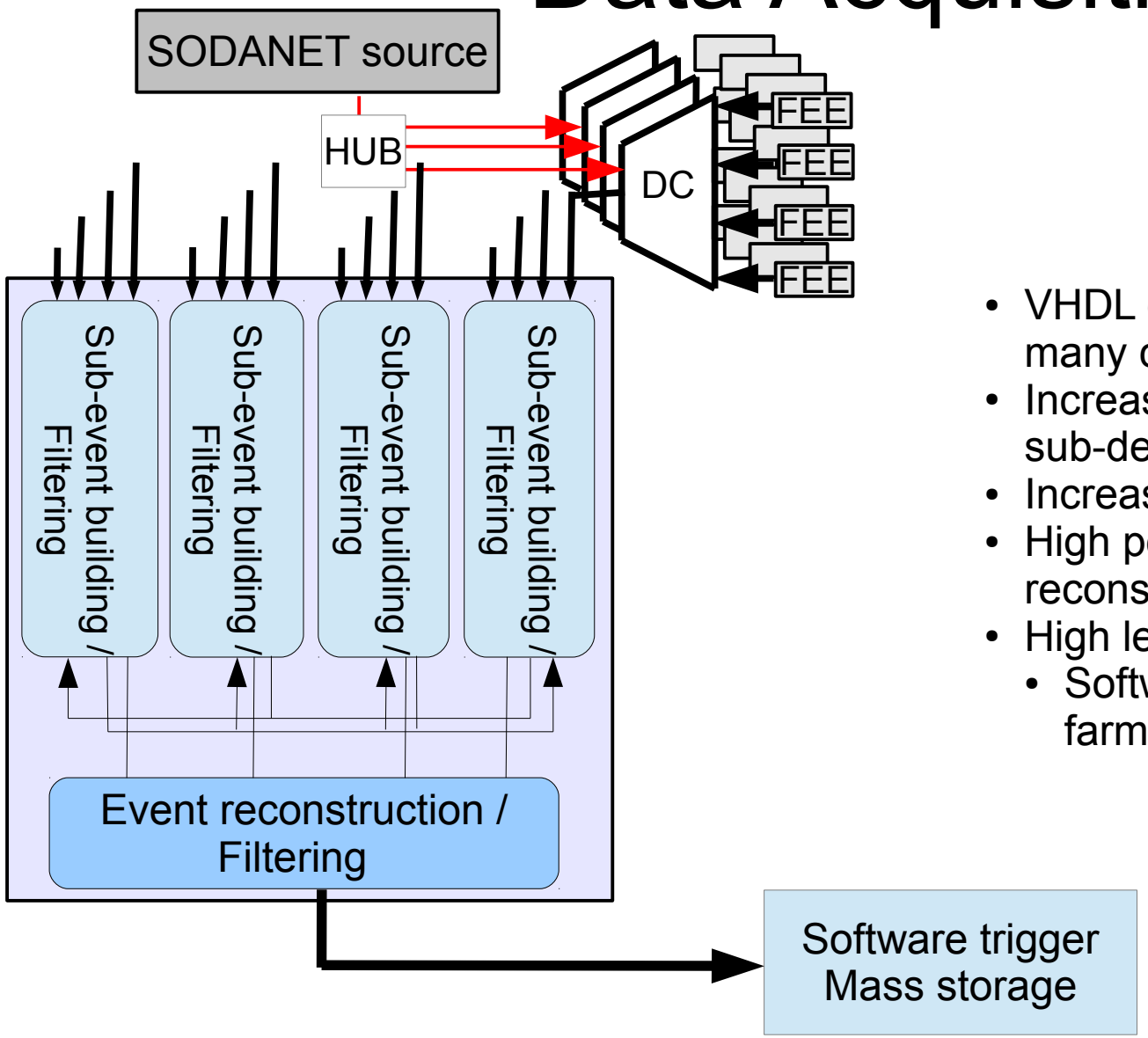


Compute Node prototype

Compute Node rev. 3:

- ATCA based carrier board
- Xilinx Virtex 4FX60
- Carries up to 4 AMC cards
- Supplies direct high speed interconnection between all 4 AMCs
- Connects all 4 AMC cards via a switch FPGA to the ATCA backplane

Extended Trigger-less Data Acquisition

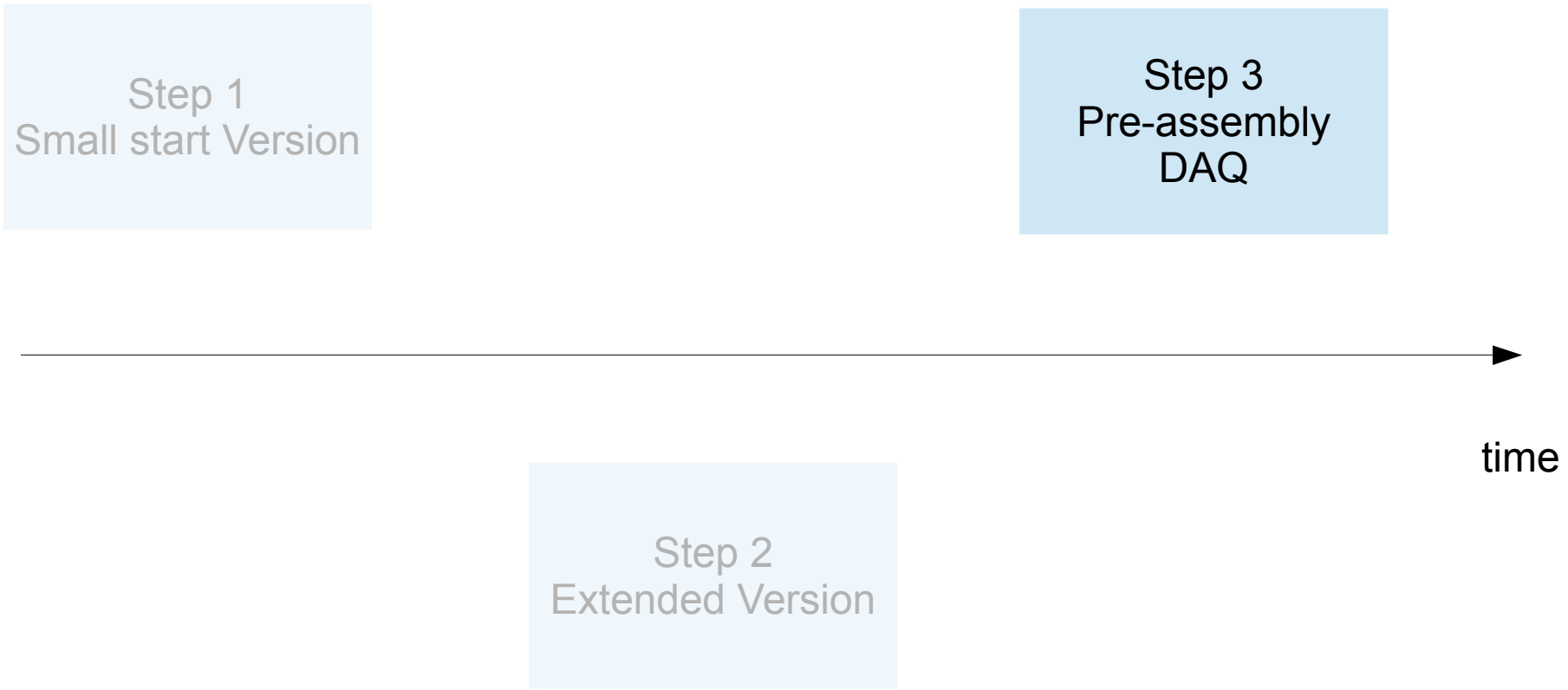


- VHDL code can be used without many changes
- Increased number of inputs per sub-detector
- Increase the possible data rate
- High performance event reconstruction
- High level event filtering
  - Software trigger on a sever farm or GPUs

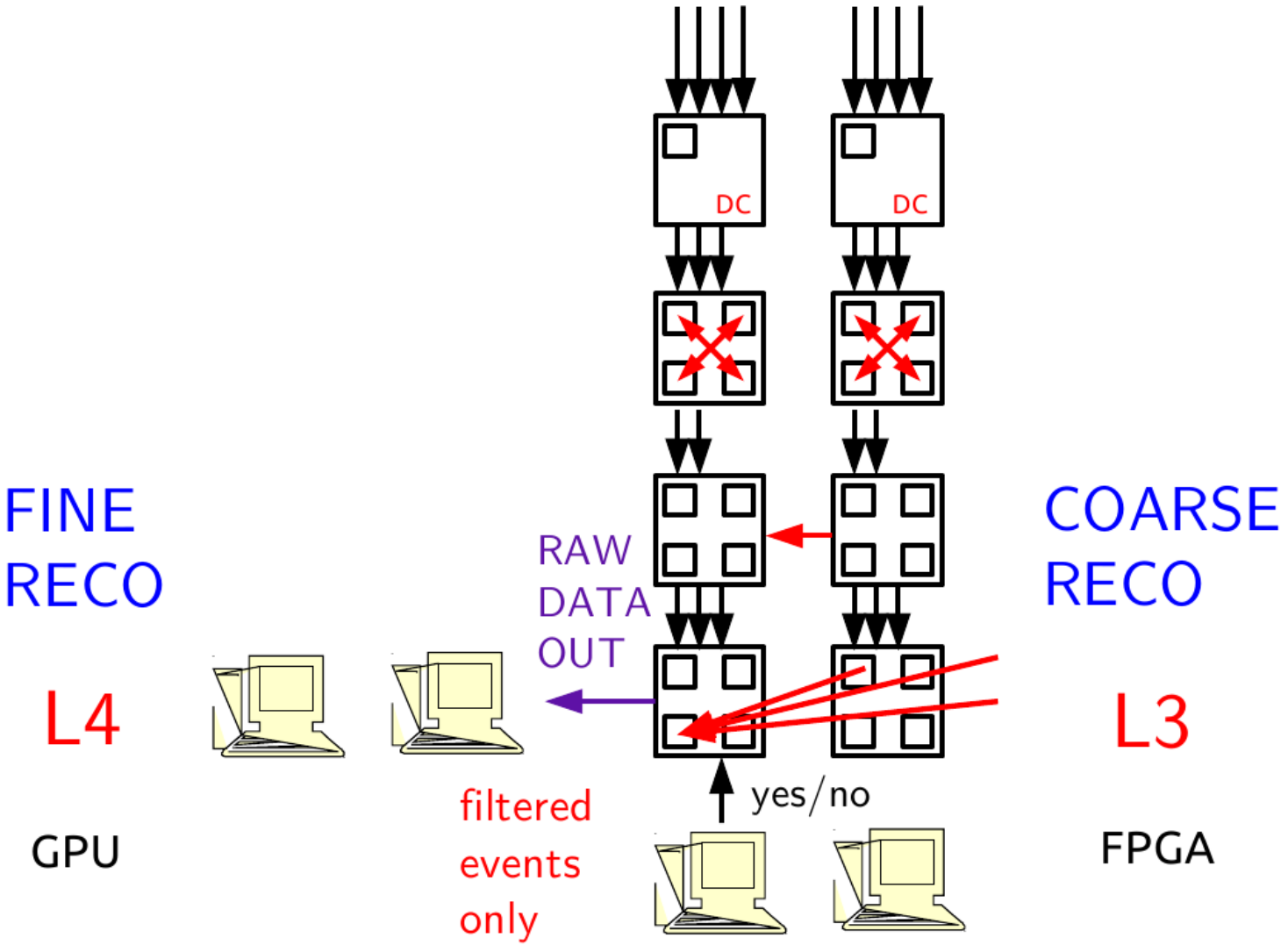
Extended Trigger-less DAQ Setup

- ATCA shelf
- 1 or 2 Compute Nodes (start version)
- 4 to 8 xTCA compliant boards
- Server farm
  - Mass storage
  - Software trigger

Three Steps Concept



Final Version



Status and Outlook

Status:

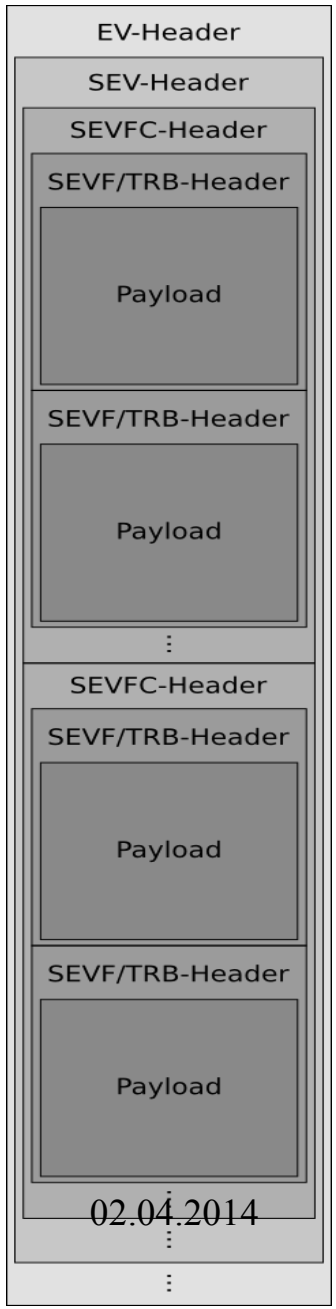
- One board setup
  - Connection of up to 4 DCs
  - Tested with simulated DCs

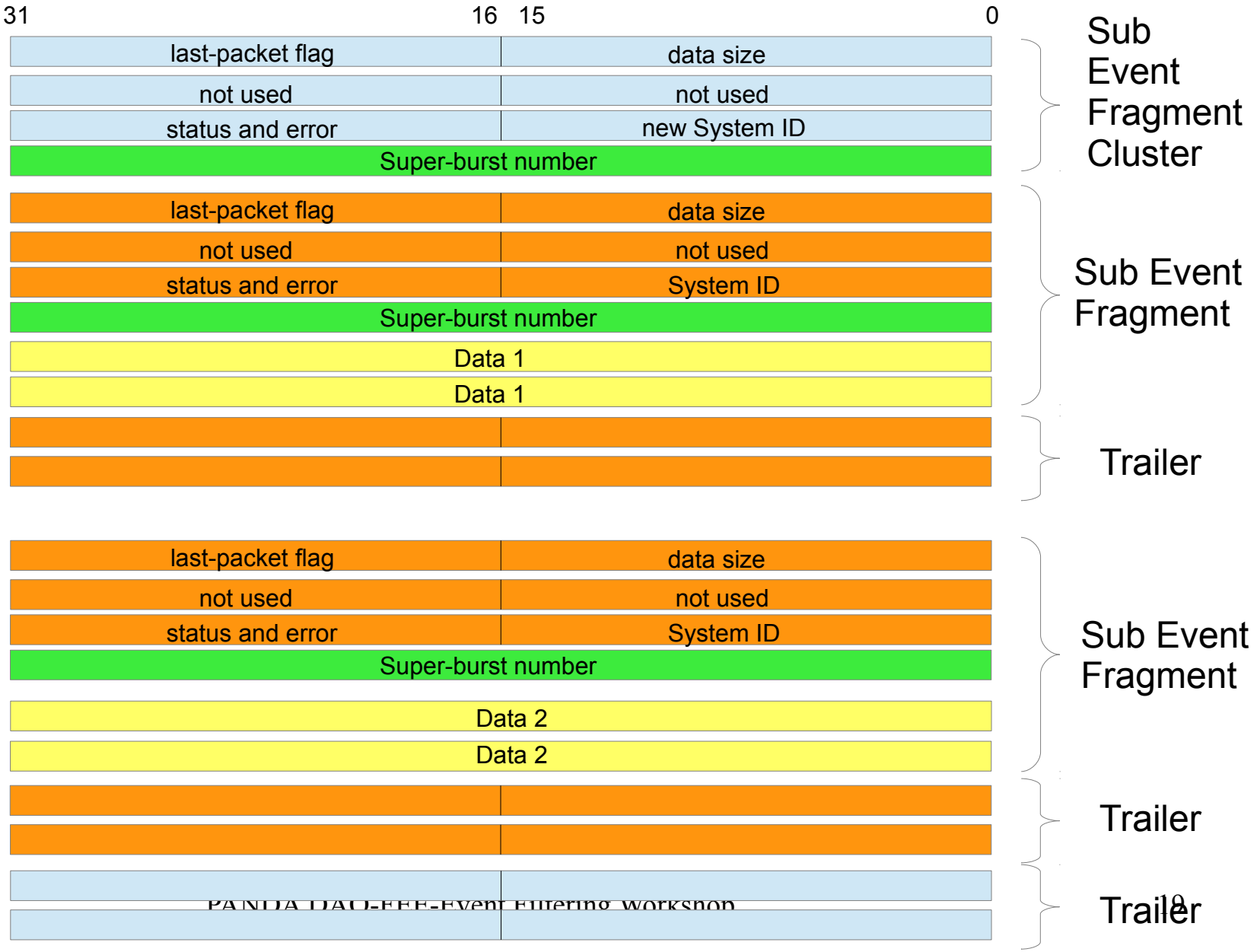
Outlook

- Tests with different kinds of DCs
- Different test with different kinds of detectors
- Upgrade to CN based DAQ

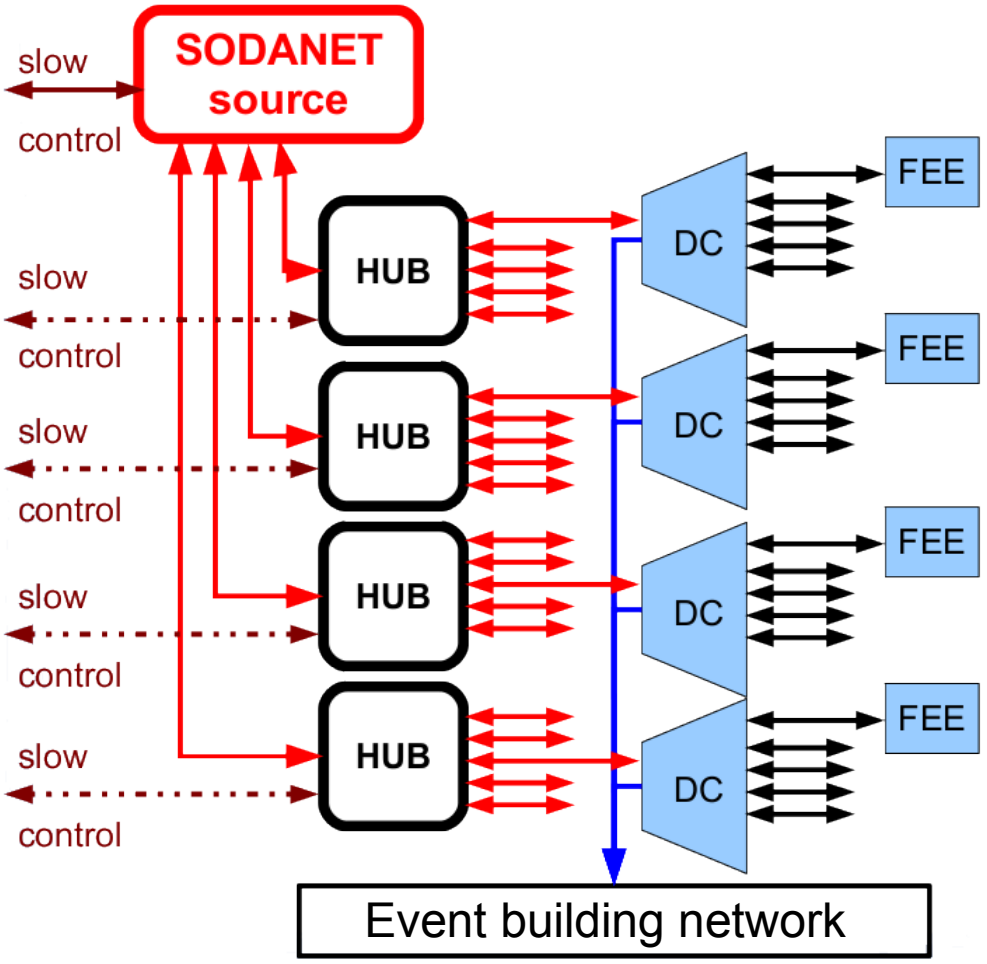
Thanks for your attention

SODANET Data Format





Synchronization of Data Acquisition (SODANET)



Functionality:

- Distribution of clock
  - Time stamp
- Distribution of synchronization commands
  - Start, stop, calibration
- Signal distributed over optical fiber
- Measurement of a signal propagation time
- Distribution of detector configuration data
- Slow control

SODANET link:

- Bidirectional
  - Source → data concentrator:
    - Synchronization
    - Front end electronic configuration
  - Data concentrator → source:
    - Slow control, used for time calibration

Data concentrator (DC)
Front end electronic (FEE)