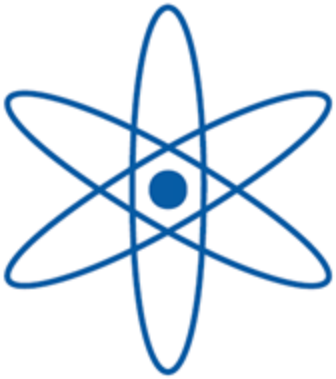

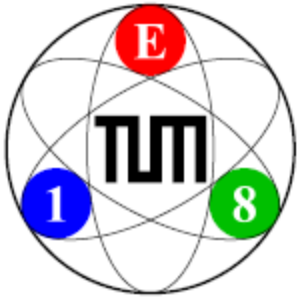

SODA system for users

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Output signals

- 155.52 MHz LVDS@2.5V
  - Fulfills jitter requirements
- Signals synchronous to SODA clock, LVTTL@2.5V
  - Global Reset
  - Burst, '1'- Burst ON
  - Run Active, '1' – Run Active
  - Super Burst, pulse at start of new SBurst
  - Destination Enable, '1' - enable
  - Trigger, pulse signal(optional signal)
  - JTAG (optional)
  - 6 reserved
- Data delivered via high speed serial link, Aurora protocol:
  - Burst Time Tag,8 bits, time within one burst
  - Burst Number, 8 bits, burst number within SBurst
  - SBurst Number, 24(32) bits, SBurst number within Run

Options for SODA receiver

1. Recommended: piggyback module
   - Has to be done a s demonstrator
   - Independent development
   - Parallel development
   - Clear splits responsibilities

2. Not Recommended: integration into existing FPGA at destination
   - SODA requirements for layout and schematic
   - Constrains problems
   - Fixed FPGA type

Piggyback SODA receiver interface

Signals to SFP+

- RX+, RX-
- TX+, TX-
- LOS
- TxDisable
- TXFault

Interface to Destination Logic

- 155.52 MHz clock LVDS
- 16 IO LVTTL signals @2.5V
- High Speed Duplex Interface 1.55Gb/s