SODA: Time Distribution System for the PANDA Experiment

I. Konorov[1], H. Angerer[1], A. Mann[1], S. Paul[1]

***Abstract*—The PANDA data acquisition system will operate in trigger-less mode and collect about 100 GBytes of data per second from more than a thousand front-end modules. The information from all detectors is combined into data blocks, every block corresponds to 500 microseconds of beam.**
The SODA (Synchronization Of Data Acquisition) project aims to develop a versatile optical network system which is, first of all, able to provide a common reference time with a precision better than 20 ps R.M.S.. In addition, the system synchronizes data taking with the burst structure and performs monitoring of data acquisition modules. Furthermore, it takes responsibility for data flow control. The core of the system is a point-to-multipoint bidirectional optical link which is able to broadcast information from a master module to few hundred destinations and to acquire information from the destination modules via a passive optical fiber network.
The first prototype system has been built and tested. The architecture of the SODA system, the hardware implementation and the performance parameters of the prototype system are discussed.

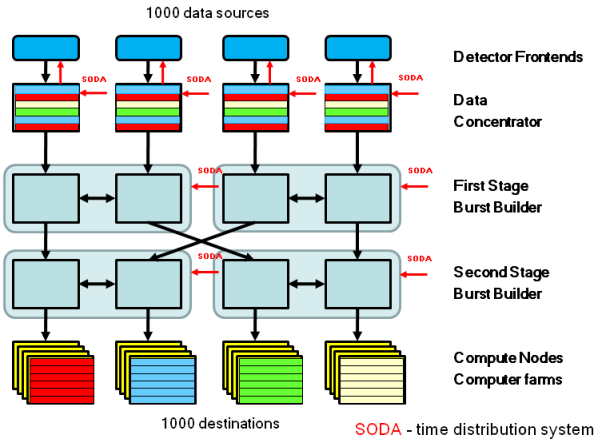

Fig. 1. PANDA Data Acquisition System. The continuous data streams, generated by the detector frontends, are chopped into the data blocks of 500μs and then fed into the switched network, where the data from different detectors are assembled into a complete burst packet.

I. Introduction

THE PANDA experiment [1] at the new FAIR facility in Darmstadt, Germany will be investigating unresolved questions of non-perturbative QCD (via precision spectroscopy of charmonium and open charm states), the search for exotic objects such as glueballs and hybrids, and more. The investigation will be done with a high intensity antiproton beam and hydrogen target at the High Energy Storage Ring. Due to the very high interaction rate of 2×10^7 s^{-1} and very wide physics objectives with different event selection criteria, it was decided to build a trigger less data acquisition system, where event selection will be done after event building in programmable computer units. The synchronization of data from different detectors and precise time measurements can be achieved by distributing a precise common clock to the front-end modules from which the time tag for every hit is derived. The trigger less data acquisition works without an event definition, instead, the data belonging to a certain period of time are grouped in blocks. In PANDA, one data block corresponds to 500 μs of beam and is called a burst. The architecture of the PANDA DAQ is shown in Figure 1.

The SODA system distributes common clock together with control signals to the data concentrator modules, from where the clock and the control signals are retransmitted to the front-ends. The front-end electronics detects hit signals, assigns time tags to them and sends this information together with the unique channel ID to the concentrator module. The concentrator module sorts hits in a time ordered manner and combines hits, belonging to one burst, into a single block. As soon as the block is complete the concentrator module sends it to a compute node via the burst building switch. At the output of the switch all data blocks belonging to the same burst are collected in one compute node where they are processed.

II. SODA architecture

The concept of the SODA time distribution system is based on the TTC (Time Trigger Control) [2] and the TCS (Trigger Control System) [3], which perform similar functions and were developed for the LHC and for the COMPASS experiment accordingly. The SODA system employs a point-to-multipoint optical network but in contrast to the TTC system the interface is a bidirectional link. The speed of the serial link is not fixed and the functionality of the system does not depend on the serial link speed. The prototype system has been developed to operate at the fixed frequency of 1250 MHz.

The SODA system consists of a controller module, passive optical splitters and receivers. The controller module can broadcast information using the full bandwidth of the serial link. The receiver modules share the bandwidth in a time-division-multiplex manner and the time slot for every receiver

This research was supported in part by the EU Integrated Infrastructure Initiative Hadron Physics project under contract number RII3-CT-2004-506078, the BMBF, the Maier-Leibnitz-Labor Garching and the Cluster of Excellence Exc153

[1] Technische Universität München, Physik Department, Garching, Germany

can be assigned dynamically by the master module. The SODA system architecture is shown in Figure 2.

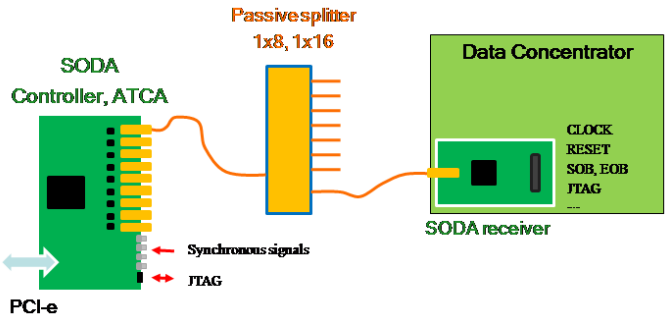

Fig. 2. SODA, architecture of the Time Distribution System.

The controller module will be built as a full size ATCA module. The module includes 32 optical transceivers, each capable to drive 16 receivers via a passive splitter, and LEMO input signals. The control and interface functions are performed by FPGAs with built-in high speed SERDES cores. A list of control signals can be:

- Reset signal - resets control logic and data buffers, defines an absolute time zero;
- Start Of Burst;
- End of Burst;
- Trigger signal for testbeams.

The passive optical splitter provides an optical interface between the master module and 16 receiver modules. The insertion losses of the signals are about 12 dBm in both directions.

The SODA receiver will be a mezzanine card similar to the prototype module which is discussed later. The receiver consists of an FPGA, a fiber transceiver and a connector. The card is mounted on a destination module which can be either a concentrator or a DAQ module. The receiver provides the common clock signal, the control signals, a JTAG interface and a high speed bidirectional serial link for monitoring and data flow control messages. The receiver carries a unique ID so it can be addressed and configured individually by the controller module.

A. SODA network interface and data encoding

The SODA is a point-multipoint system in the direction from the controller module to the destination modules and a point-to-point connection for the backward link. In order to use only one set of optical elements, SODA transmitts an information via a single fiber, using so called BIDI transceivers with wavelengths of 1310/1490 nm.

The information is encoded byte wise with standard 8b/10b encoding. The packets have a variable length from four bytes up to one kilobyte and there are at least two comma symbols in between packets.

Each command is encoded in a single packet. The master sends synchronous commands with fixed latency and asynchronous commands with an undefined latency. There is only one synchronous command, and it is reserved for the control and JTAG signals. In order to guarantee the fixed latency in the case of overlapping of the synchronous command with a packet, the synchronous command is inserted into the packet together with one comma symbol before and after, see Figure 3. The interrupted packed is continued without a data loss.

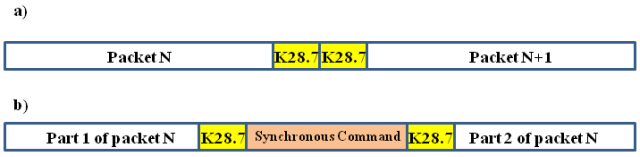

Fig. 3. SODA serial interface: a) two consecutive packets are separated by two comma symbols; b) the synchronous command insertion into a packet: the packet transmission is interrupted and the synchronous command is inserted with one comma symbol before and after, the packet transmission continues without data loss.

B. SERDES synchronization

One of the features of modern deserializers is an undefined data latency and an undefined recovered clock phase after a power up or a resynchronization. The latency changes between few bits and 10 bits in case of 8b/10b encoding depending on the particular circuit design. In the Lattice ECP2M FPGA family the deserializer latency has an uncertainty of 10 bits i.e. the clock has ten possible phase positions corresponding to ten bits of an encoded data byte.

For the SODA prototype a new method to fix the recovered clock phase has been developed and successfully tested.

The method utilizes two deserializers for the incoming data stream, as shown in Figure 4. The first deserializer locks to the incoming data after power up or loss of lock and initiates a synchronization procedure implemented in a finite-state machine in the same FPGA. The state machine measures the phase relation between the recovered clocks of the two deserializers by measuring the time difference ΔT between two enable signals which accompany every decoded synchronous word. The syncronous words are broadcasted by the SODA controller regular with a frequency of few kiloherz. The enable signal of the first deserializer is used as a reference and the second deserializer is reseted after the phase relation measurement is completed. After every reset signal the second deserializer locks to one of the ten possible phase positions randomly and the time relation between clocks is measured again. The state machine repeats the reset-measurement procedure until all ten phase positions are found. At this point the state machine continues the reset-measurement procedure in order to put the clock phase to the earliest position respectively to the first deserializer. This corresponds to the maximum possible positive value of ΔT, see Figure 4.

After this procedure the clock phase of the second deserializer is in a fixed time relation to the master clock of the SODA controller.

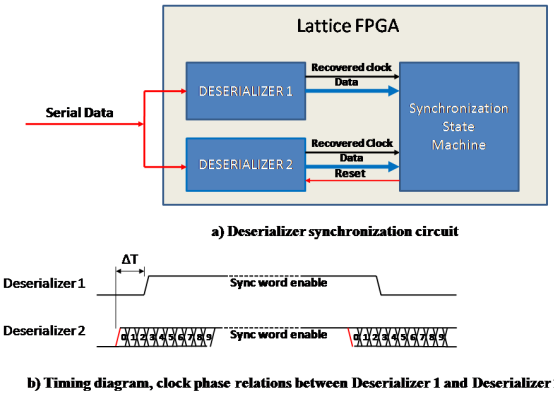

Fig. 4. a) The synchronization circuit to provide a fixed clock phase, b) the timing diagram showing all ten possible phase relations between the two enable signals. By maximizing ΔT a fixed time relation to the master clock of the SODA controller is achieved for the second deserializer.

III. SODA System Prototype and Performance Measurements

For testing the performance of the FPGA based time distribution system a SODA receiver prototype module was developed and produced, the photo of the module shown in Figure 5. The prototype module is equipped with a Lattice ECP2M35 FPGA, a flash memory to store configuration data, a 125 MHz crystal oscillator and a BIDI transceiver.
The functionality of the SODA controller were implemented in the Lattice ECP2M50 SERDES Evaluation Board.

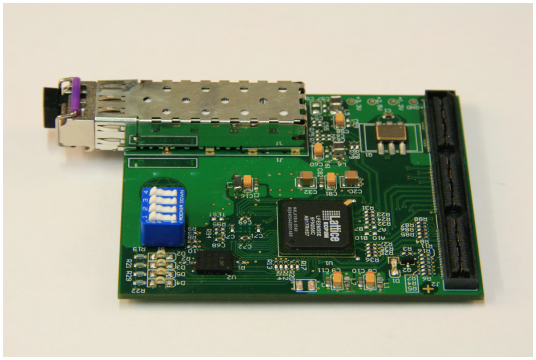

Fig. 5. SODA receiver module prototype.

The test bench to measure the clock jitter between recovered clock and the master clock is shown in Figure 6. It includes the SODA controller, the SODA receiver and the 1x8 optical splitter.

During the jitter measurement the SODA controller was sending packets with pseudo random data, spaced by four comma symbols. One of the random bytes was interpreted as a synchronous symbol. The jitter measurement were performed with a LeCroy SDA6000A Serial Data Analyzer with 6 GHz bandwidth and 20 Gsamples per second sampling rate. The clock relation between the recovered clock and the master clock is shown in Figure 7. The jitter of the clock was

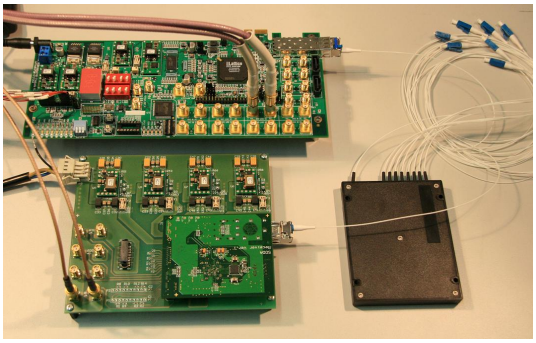

Fig. 6. Test setup for clock jitter measurements.

measured to be 15 ps RMS. The measurements were repeated many times for verification of the phase relation stability and every time the system recovered the clock to the same position.

IV. Conclusions

The tests of the prototype system have proved that the method, invented to synchronize the clock phases, allows to overcome the latency uncertainty problem of the Lattice FPGA deserializer. It was also demonstrated that the Lattice ECP2M FPGA family allows to build a time distribution system with the performance parameters according to the requirements of the PANDA experiment. The jitter of the recovered clock respectevely to the master clock was below 20 ps RMS.

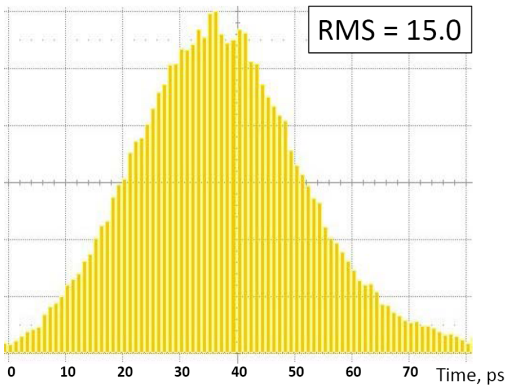

Fig. 7. Clock jitter: the SODA receiver clock jitter respectevely to the master clock.

References

[1] PANDA Collaboration, "$\bar{P}$ANDA: Technical progress report", GSI FAIR, Tech.Rep., 2005.

[2] 1997 Status Report on the RD-12 Project, CERN/LHCC 97-29, 30 April 1997.

[3] The COMPASS experiment at CERN, NIMA 577 (2007)455-518.