SODA: Synchronization Of Data Acquisition

I.Konorov

- Requirements
- Architecture
- System components
- Performance
- Conclusions and outlook

Requirements & Functions

Requirements

Provision of absolute time at Front-end electronics
Precision 20 ps for ToF and >50 ps for all other detectors
Synchronization with operation of HESR
Synchronization with Target

Implementation :

Time reference

- ➢ single clock to all front-ends via optical network – 125MHz (100-155.52)

Absolute Time

- ➢ RESET SIGNAL
  - sets local time counters to ZERO
  - issued at start of run

Start/End of data block

- ➢ Heart Bit – Start of Block/End Of Block signals

  HESR beam structure : 2us beam & 400 ns no beam

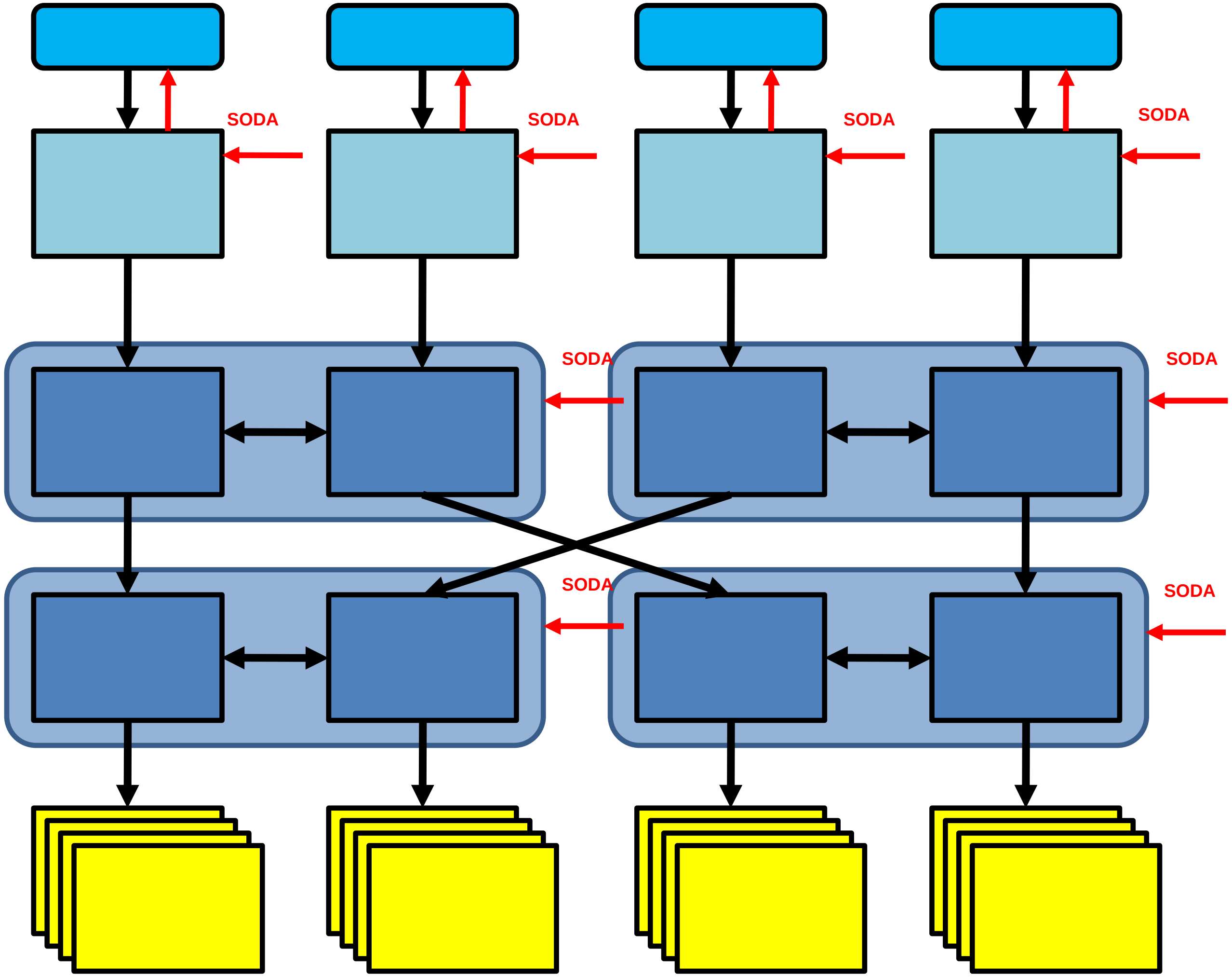
Enable/Disable Data

- ➢ data throttling

Extra functions :

Data flow control
calibration, tests …

DAQ Architecture



Detector Frontends

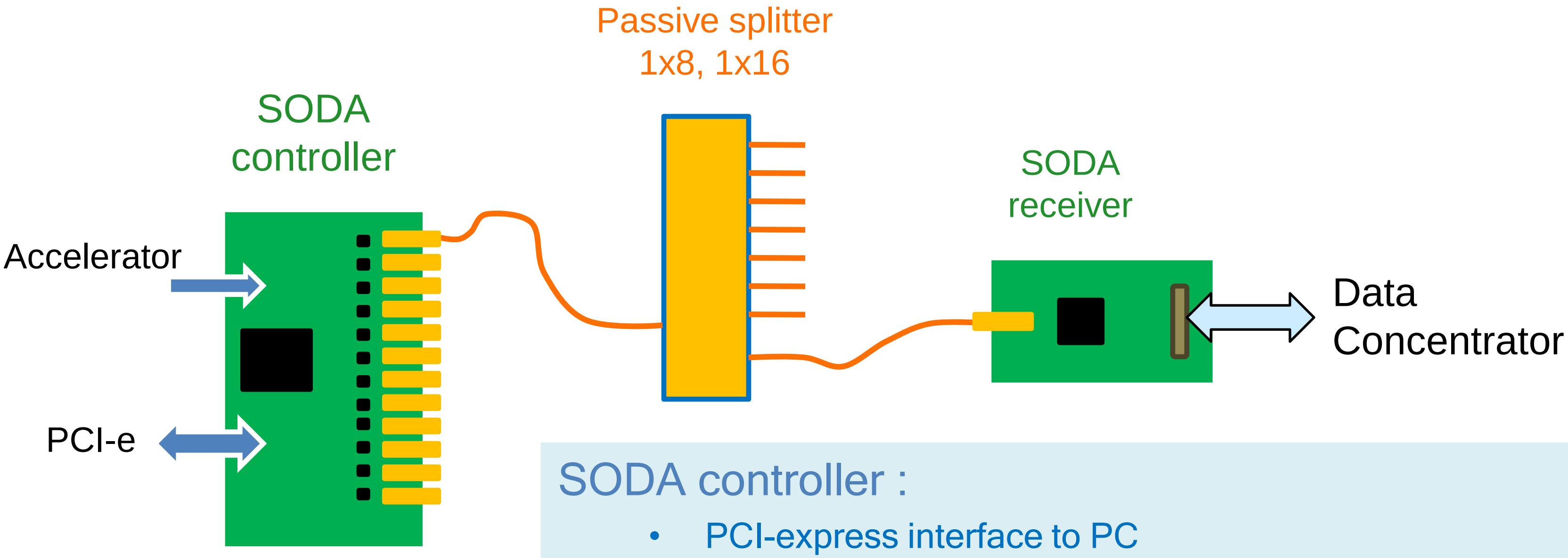
Data Concentrator

First Stage "Event" Builder

Second Stage "Event" Builder

Compute Node

SODA architecture



SODA controller :

- PCI-express interface to PC
- N - optical transceivers, BIDI transceiver - 1310/1490nm
- Lattice ECP2M FPGA with SERDES: Controller -> Receiver
- Texas Instrument TLK1221 SERDES: Receiver->Controller
  - fast Relock Times less than 256 ns

Optical splitter :

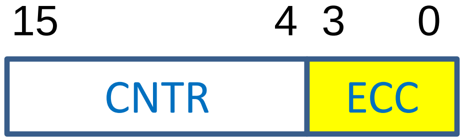
- Single mode fiber
- Insertion losses
  - 1x8; 1x16; 1x32

SODA receiver:

- Mounted directly on Data Concentrator module
- Lattice ECP2M FPGA SERDES
- Optical transceiver BIDI 1490/1310nm

Data frames

Synchronous with fixed latency

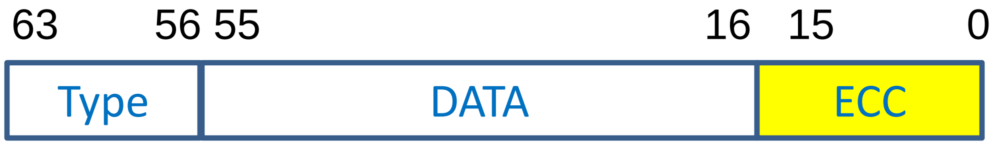


15 4 3 0

CNTR ECC

CNTR bits - START, STOP, RESET, Burst START, Burst STOP, Calibration Pulse,…

Asynchronous, high priority

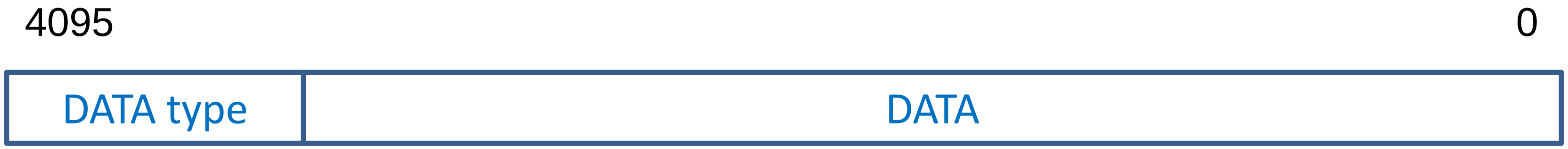


63 56 55 16 15 0

Type DATA ECC

DATA - Time Tag 40 bits, 2 hours of data taking

Asynchronous, low priority

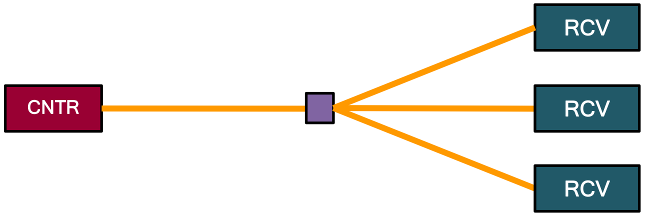


4095 0

DATA type DATA

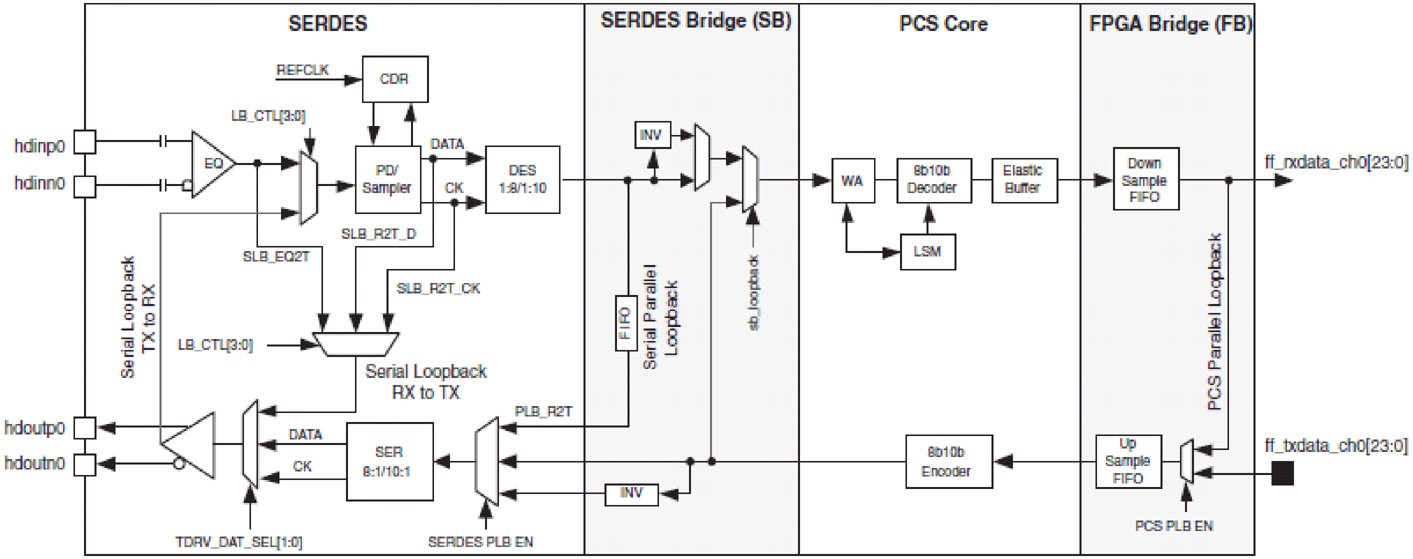
SODA serial interface

- 125 MHz or 1.25 Gb/s now, in future may go up to 2.5Gb/s
- Bidirectional link :
  - Controller -> Receivers full bandwidth of 125 MB/s
    - Broadcast synchronous commands with fixed latency, 32 bit long:
      - RESET, Start/Stop data taking, Start/End of burst
    - Asynchronous commands , 32 bit long
      - Scanning connected modules
      - Control
    - Packets up to 1kB



  - Receivers -> Controller
    - Time sharing principle, similar to common bus
    - Only one receiver can send data at a time
    - Controller schedules Receivers access
    - Switching from one receiver to another takes 400 ns
      - Laser OFF - Laser On - Relock SERDES to new receiver
    - Heartbeat packet
    - Status packet

FPGA SERDES, Lattice ECP2M



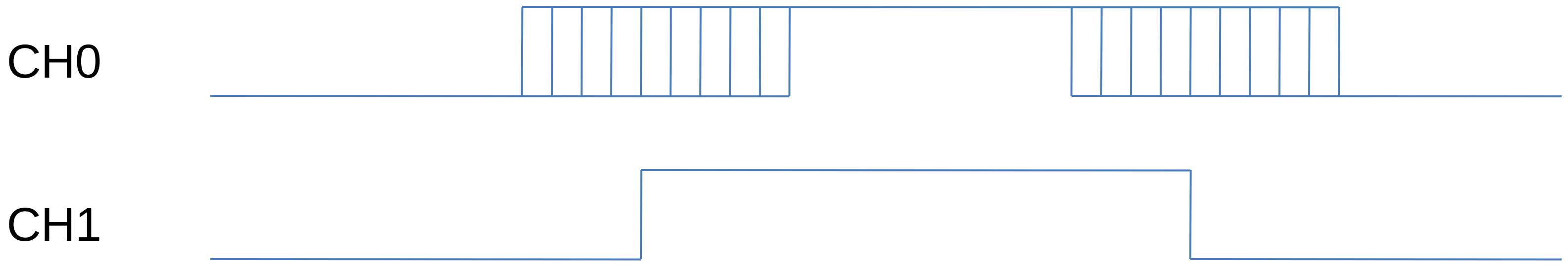
Two clocks domain

SERDES Recovered Clock Jitter

FPGA’s SERDES locking sequence

- Locking CLOCK
- Lock byte boundaries

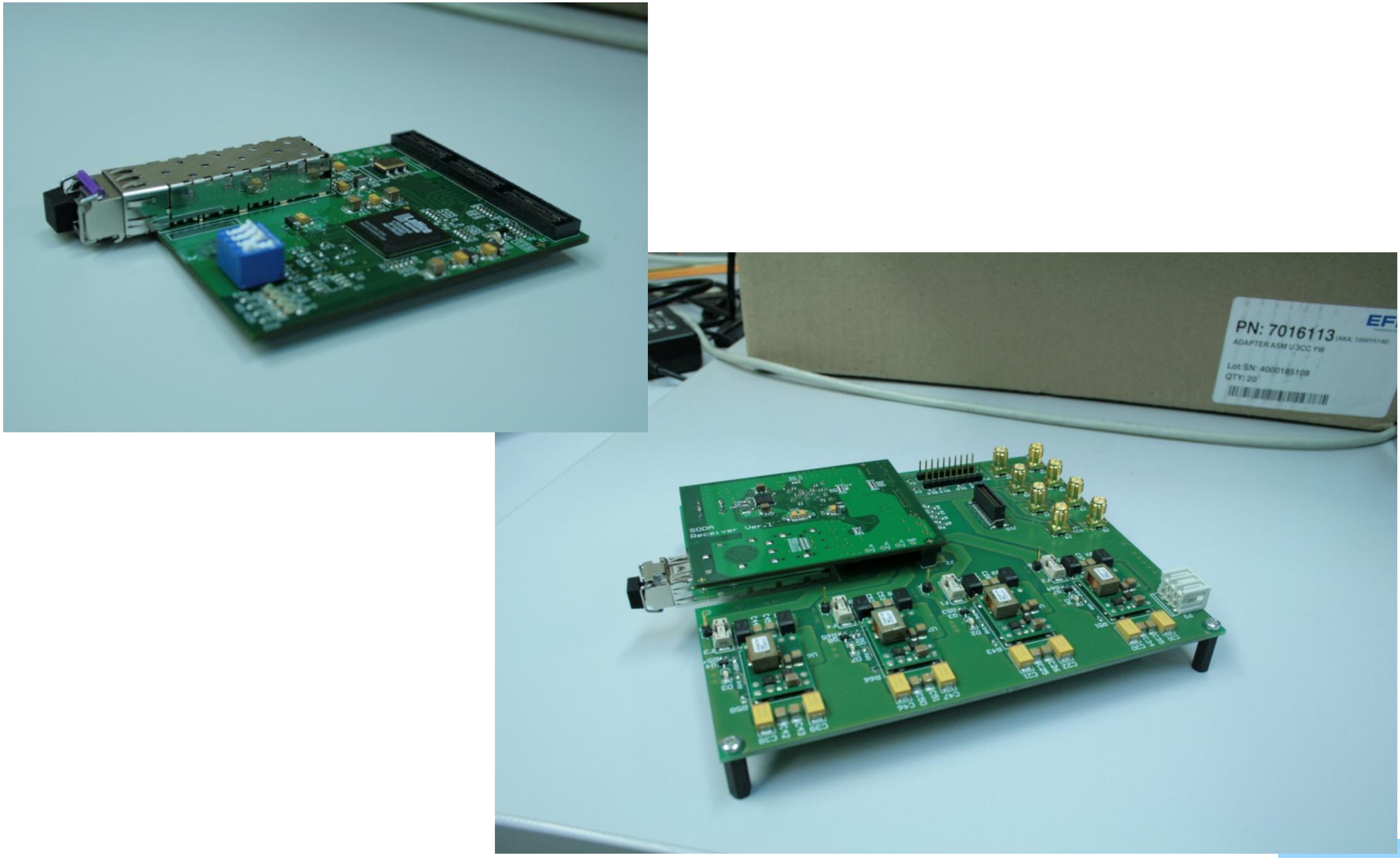
Recovered clock jitter = one period



Solution:

- Use two Deserializes + FPGA based TDC
- First deserialize - reference
- Second - reset second RX until Latency is minimum

SODA Receiver

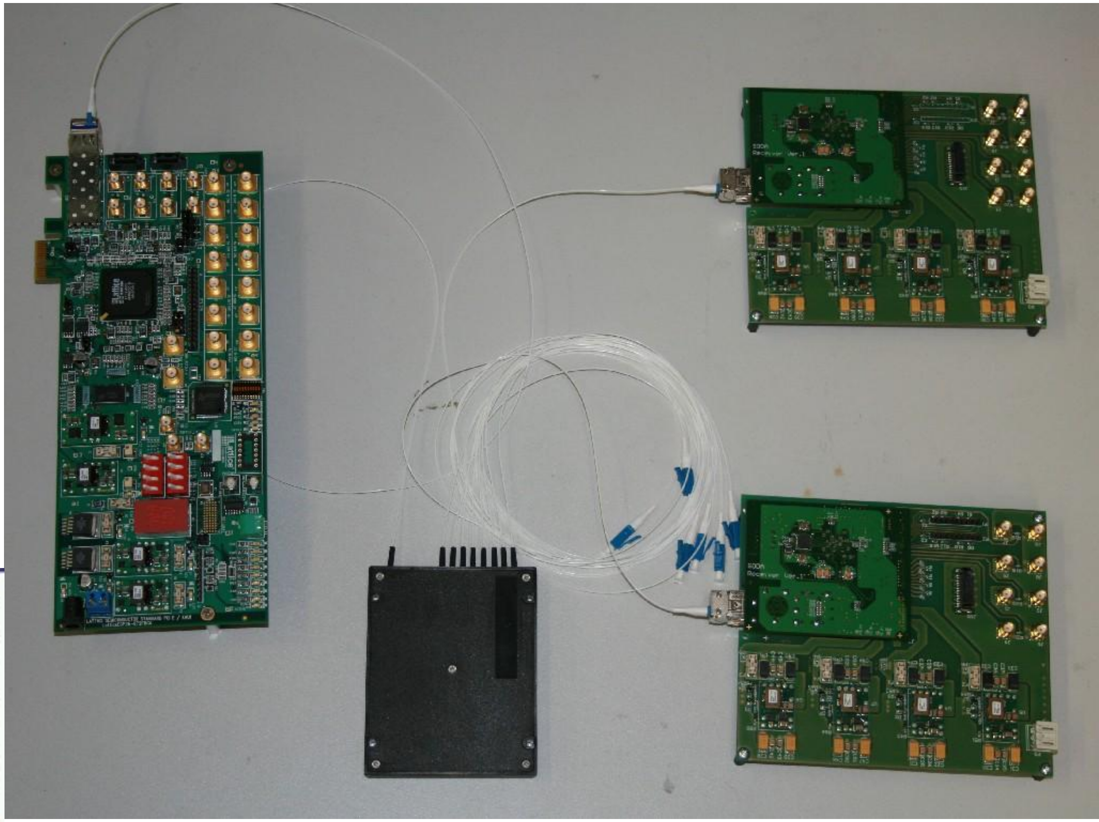


SODA Receiver connector

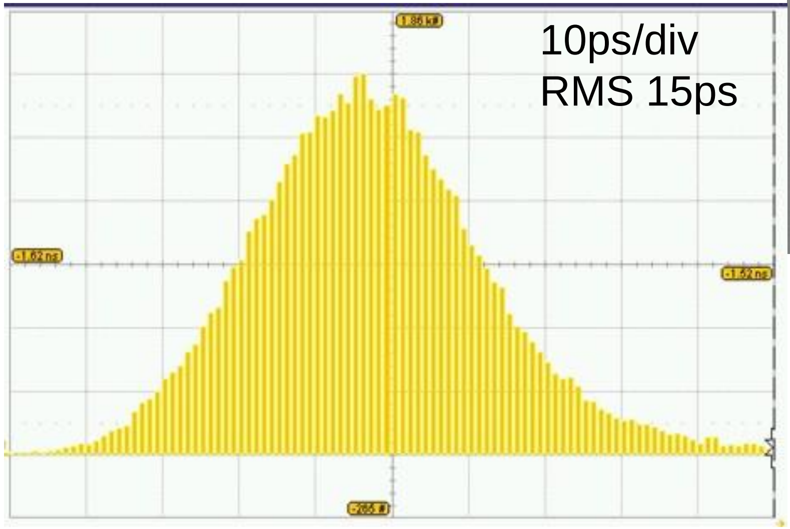
- 125 MHz CLK , LVDS
- High speed serial link
- JTAG interface - SODA Receiver Master
- JTAG interface – Carrier card Master
- 16 LVDS line for debugging and user reqiurements

Test setup

Lattice PCI-e evaluation card
Optical splitter 1:8
2x SODA receivers mounted on evaluation cards



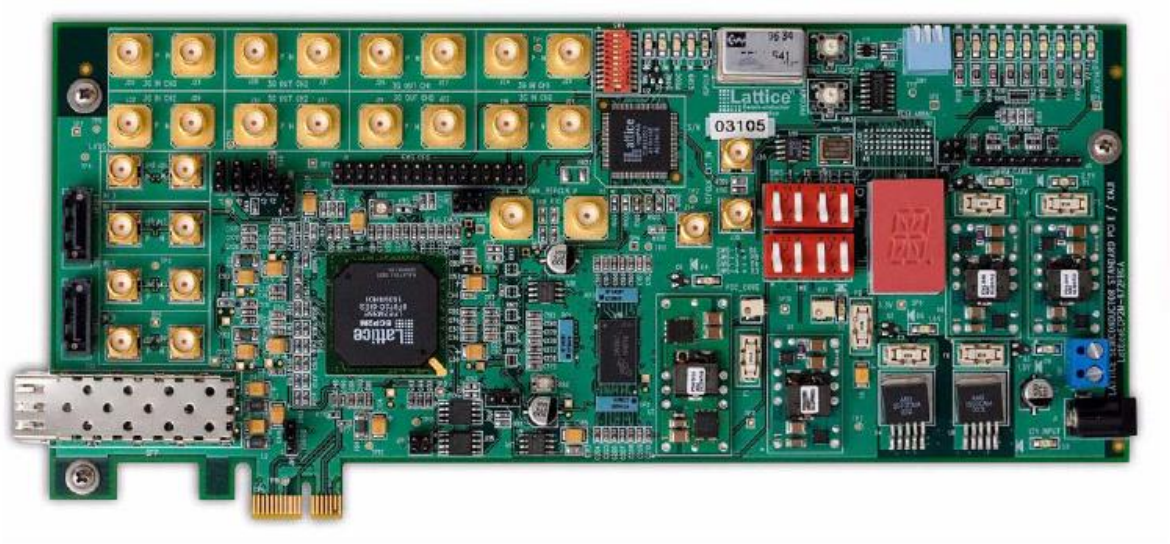
Reference Clock vs Recovered Rx Clock



10ps/div
RMS 15ps

SODA controller and receiver

Lattice SC PCIe evaluation card - SODA controller prototype



SODA receiver

- AMC card
- Lattice ECP2M35 256FBGA
- To be delivered this week

Conclusions and outlook

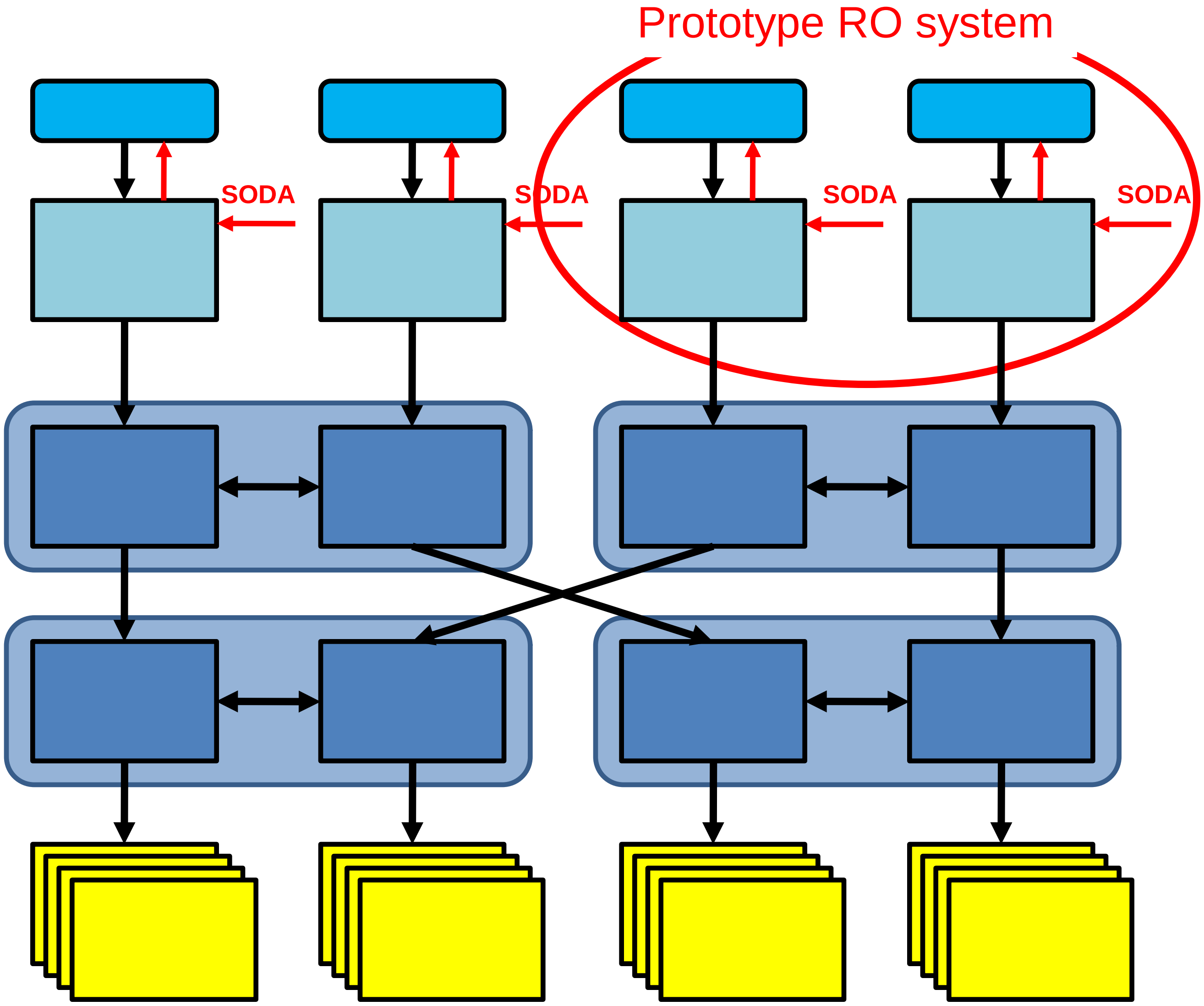
- System components been validated
  - FPGA SERDES validated - clock jitter < 20 ps
  - Fibre transceivers
  - Passive optical splitters

- Next step
  - Implement data transmission protocols with minimum functionality

- Develop new optical splitter with asymmetrical insertion losses

- Define first application !!

DAQ Architecture



Detector Frontends

Data Multiplexer

ATCA based Sub “Event” Builder

ATCA based “Event” Builder

Compute Nodes