UNI
BASEL

PHYSICS BASEL
ELECTRONIC LAB 2.17
KLINGELBERGSTR. 82
CH-4056 BASEL

SWITZERLAND

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DISCRETE PREAMPLIFIER FOR VPT READOUT

LNP-PREAMPLIFIER VERSION SP 883A01

1. OVERVIEW

The Low Noise / Low Power Charge Preamplifier (LNP-Preamp) is a discrete charge preamplifier which has an excellent noise performance in combination with low power consumption. The preamplifier is adapted for the readout of Vacuum Photo Triodes (VPTs); it was originally designed for the readout of Large Area Avalanche Photo-Diodes (LAAPDs). VPTs will be used as photo detectors in the forward endcap of the Panda electromagnetic calorimeter (EMC). They are attached to the end face of the lead tungstate scintillating crystals (PWO-II) which have a typical geometry of (200 x 25 x 25) mm^3. Due to the higher event rates and large photon energies in the forward endcap with respect to the barrel, the APDs would suffer from radiation damage (increased noise) and from nuclear counter effect. Therefore APDs are not suitable at that position of the EMC. The VPT is a sort of a single stage photomultiplier with only one dynode which can also be operated in a strong magnetic field without loosing too much gain. The VPT translates the scintillating light of the PWO-II crystals into an electrical charge which is linearly converted by the LNP-Preamp to a positive voltage pulse; this output pulse is then transmitted via a 50 Ohm line to the subsequent electronics.

1.1. POWER CONSUMPTION

Since the complete forward endcap, together with the VPTs and the preamplifiers, will be cooled to low temperatures (to increase the light-yield of the PWO-II crystals), the power dissipation of the preamplifier has to be minimized. Low power dissipation leads to a smaller cooling unit and thinner cooling tubes; it also helps to achieve a uniform temperature distribution over the length of the crystals. The LNP-Preamp has a quiescent power consumption of 45 mW. The power dissipation is dependent on the event rate and the photon energy; at very high rates combined with the maximum photon energy, the power consumption is increased up to 90 mW.

1.2. VPT AND NOISE

To reach the required low detection threshold of only several MeV, the noise performance of the preamplifier is crucial. The VPTs have an outside diameter of 25 mm and a typical photocathode with a diameter of 18.5 mm, resulting in an active area of circa 268 mm^2. Compared to the active area of the LAAPD (100 mm^2) this is an increase of a factor 2.7. The VPT anode capacitance is around 22 pF which is more than ten times lower than the capacitance of the LAAPD; this results in a much lower noise from the LNP-Preamp. Thus, the shielded cable between the VPT and the LNP-Preamp has a significant impact on the total detector capacitance; it must be kept as short as possible.

The dark current of the VPT is significant lower than the one from the LAAPD; 1 nA compared to 50 nA, both measured at a room temperature. On the other hand the quantum efficiency (QE) of the VPT is only about 20%, compared to 70% of the LAAPD. Further the internal gain (M) of the VPT is only around ten, which is five times lower than the LAAPD.

The noise floor of the LNP-Preamp at –25°C loaded with an input capacitance of 22 pF, has a typical equal noise charge (ENC) of 235 e^-_{RMS}. This is measured with an ORTEC 450 shaping filter/amplifier

with a peaking-time of 650 ns. Because the VPT has almost no dark current the noise is not increased due to the leakage current of that photo detector.

Assuming 100 photons/MeV at the end face of the cooled (–25°C) PWO-II crystal would result in 43 photons/MeV on the active area of the VPT. This is coming from the fill factor of 40%: VPT active area of 268 mm^2 with respect to an end face area of about 625 mm^2. Since the end face not covered by the VPT will be masked by highly reflective material, we assume 50 photons/MeV on the VPT. By applying the QE and the internal gain of the VPT, a primary photon with the energy of 1 MeV induces an input charge of 16 aC (100 e^-) to the preamplifier. So an ENC of 235 e^-_{RMS} corresponds to an energy noise level of about 2.4 MeV_{RMS}. This is almost the same energy noise level as achieved under the same conditions in the barrel with the LAAPD readout (2 MeV_{RMS}). At the same photon energy, the signal from LNP-Preamp connected to a VPT is a factor of nine smaller, but also the noise is a factor of more than seven smaller compared with the LAAPD. That's why the signal to noise is in the same order when using a VPT or an LAAPD for the readout of a PWO-II crystal.

All these numbers above are related to the VPT type RIE-FEU-190 used in the CMS ECAL. A new VPT with a significant higher QE combined with a larger internal gain will be developed and produced by the company Photonis. By using this new VPT, the energy noise level will be reduced remarkable. This may also be necessary, because the noise level is increased as the shaping time is decreased. Shorter shaping times are mandatory to cope with the expected high event rates in the endcap. By decreasing the peaking-time from 650 ns (reference values) to 200 ns the noise level is raised by around 25%. So the noise floor with the more realistic shaping with a peaking-time of 200 ns corresponds to 3 MeV_{RMS}.

1.3. EVENT RATE

The expected event rate in the forward endcap is maximum 500 kHz per crystal. The LNP-Preamp has a feedback time constant of 25 µs. This feedback time constant is a trade-off between noise performance and pile-up problematic. Reducing the feedback time constant by a factor of two will increase the noise by about 10%.

For a single pulse (or very low rates) the LNP-Preamp accepts an input charge of up to 4 pC; for a continuous event rate of 500 kHz an input charge of up to 8 pC is allowed. This discrepancy is due to the following reason: A single output pulse starts from zero output voltage and is limited by the positive supply voltage (+6 V) of the LNP-Preamp. At high continuous event rates the output pulses will swing between the negative (–6 V) and the positive (+6 V) supply voltage; therefore the maximum input charge is doubled. If a 500 kHz event rate is applied abruptly (burst) to the LNP-Preamp it takes around one second until a continuous input charge of up to 8 pC is allowed. During that transition period, a maximum input charge of 0.3 pC can be handled. With this charge restriction, the output voltage of the preamplifier stays always in the linear range and is never limited from the power supply voltages. Nevertheless, the electronics after the preamplifier has to perform a good base-line correction, because at higher rates it is likely that one pulse sits on the trailing edge of the previous one.

If a charge of 16 aC/MeV is assumed from the VPT (see section VPT and Noise) the maximum expected photon energy of 10 GeV results in an input charge of only 0.16 pC. Under the worst condition (a 500 kHz burst), the LNP-Preamp will not be restricted due to pile up even with the relative long feedback time constant of 25 µs.

1.4. VPT BIAS VOLTAGES

Because the anode of the VPT will be referenced to ground by the LNP-Preamp, the photo cathode (PC) and the dynode (DY) must be biased with negative high voltages (HV). To have the input of the preamplifier referenced to ground has the advantage that any noise on the HV supply is not directly coupled into the charge sensitive input. The typical bias voltages for the VPT type RIE-FEU-190 are: Photo cathode: V_{PC} = –1'000 V; Dynode: V_{DY} = –250 V.

Even if these bias voltages do not directly couple to the charge input of the preamplifier, they have to be cleaned from external noise by an efficient low pass (LP) filter before they are wired to the VPT. Also if all the VPT are biased with the same two high voltages, each VPT must have their own LP filter to prevent from crosstalk. These LP filters for the two negative bias voltages (V_{PC}, V_{DY}) are not integrated on the preamplifier printed circuit board (PCB). A separate LP filter board has to be used; to minimize the

noise level it is important that the ground of this LP filter board is tightly connected to the ground of the LNP-Preamp. During the prototyping phase it is reasonable that the both bias voltages (V_{PC}, V_{DY}) of the VPT can be adjusted independently. In the final realization a passive voltage divider can be eventually be used to generate the two bias voltages.

At the maximum event rate of 500 kHz with the maximum expected photon energy of 10 GeV (0.16 pC from the VPT) a mean current of 80 nA is flowing trough the VPT. This current is mainly draw from the dynode bias supply (V_{DY}). Since the internal gain (M) of the VPT varies only about 0.1% per volt the voltage drop over the LP filter for the VPT dynode bias is not so critical.

1.5. DYNAMIC RANGE

As explained in the section Event Rate, the LNP-Preamp is designed for a single pulse charge input of maximum 4 pC. With an input charge of 16 aC/MeV coming from the VPT (see section VPT and Noise) this corresponds to a maximum photon energy of 250 GeV. Therefore the dynamic range of the LNP-Preamp is restricted by the noise floor only. That's why the specification of a dynamic range is strongly dependent on the applied shaping filter.

In principle, the energy range of the LNP-Preamp spans from the noise floor of 3 MeV_{RMS} (with a peaking-time of 200 ns, see section VPT and Noise) up to the maximum energy of 250 GeV; this corresponding to a theoretical dynamic range of 83'000. In practice, the typical energy range will start from 6 MeV ($2 * \sigma_{noise}$) and end at 10 GeV which corresponds to a dynamic range of 1'670.

1.6. TRADITIONAL READOUT

If a peak-sensing analog to digital converter (ADCs) is used for the energy readout, the needed base-line correction is performed by the shaping filter/amplifier, which is installed between the preamplifier and the peak-sensing ADC. For our application, a reasonable peaking-time is between 100 ns and 200 ns. Longer peaking-times result in better noise performance, but they suffer from worse double pulse accuracy.

For good timing information a timing amplifier with a peaking-time between 20 ns and 100 ns seems to be suitable in front of a constant fraction discriminator (CFD). With that scheme one can easily reach a timing resolution of better than 2 ns for energies above 300 MeV.

1.7. FADC READOUT

Readout with a flash ADC (FADC) does not need a dedicated shaping and timing amplifier. Only a good anti aliasing low-pass filter/amplifier has to be implemented in front of the FADC. The cut-off frequency of that filter is given by the sampling frequency of the FADC divided by 2.5; this prevents from aliasing effects due to the sampling.

To determine the energy with a high signal to noise ratio the digitized values can be processed by a digital shaping filter followed by a digital peak determination.

The timing information is extracted by processing the digitized values similarly to the traditional signal chain with a fast digital timing filter followed by a digital implemented CFD.

One has to point out, that the processing for the energy- and timing information extraction must be performed in real time. This can be implemented by using programmable digital signal processors (DSPs) or complete in hardware by using field programmable gate arrays (FPGAs). The needed signal throughput at the high sampling frequency (50 MHz - 100 MHz) combined with the complex algorithm will result in a remarkable power dissipation.

2. PERFORMANCE & SPECIFICATIONS

The LNP-Preamp (Version SP 883a01) for the VPT is a further development of the charge preamplifier described in the section 8.5.2 on page 204ff in the "Panda Technical Progress Report, February 2005". Some modifications on the circuit are made and a couple of components are changed to SMD types.

A summary of the LNP-Preamp (Version SP 883a01) performance and specifications is given below:

- J-FET (BF862, NXP Semiconductors) in combination with a low power, high-speed current-feedback operational amplifier (AD8011AR, Analog Devices)
- Supply +6 V@6.3 mA, -6 V@1.2 mA → 45 mW quiescent power consumption
- Rise-time @Cd = 22 pF: 13 ns
- Feedback time-constant: 25 µs
- Gain: 0.5 V/pC at 50 Ohm termination
  - Maximum single pulse input charge: 4 pC
  - Maximum 500 kHz burst input charge: 0.3 pC
  - Maximum continuous 500 kHz input charge: 8 pC
- Single channel LNP-Preamp version: PCB size (48 x 18) mm^2
- Typical noise performance at Cd = 22 pF (see also *Figure 1*)
  - ENC = 235 e^-_{RMS} @ –25 ºC (Shaping with a peaking-time of 650 ns)
  - ENC = 300 e^-_{RMS} @ –25 ºC (Shaping with a peaking-time of 200 ns)

The single ended output of LNP-Preamp is designed to drive a 50 Ohm transmission line. The charge sensitivity is 0.5 V/pC and so the maximum input charge of 4 pC corresponds to a positive output pulse with a peak voltage of 2 V at 50 Ohm.

As an incident photon energy of 100 MeV corresponds to a pulse peak of only 3.2 mV the subsequent electronics has also to be designed with low noise performance. If the following electronics is located far away from the preamplifier, it may be necessary to add an additional amplifier onto the LNP-Preamp printed circuit board. Advantageously an amplifier with a differential output driver should be integrated because differential signals are less sensitive for noise-pickup due to an improper ground system. The differential driver AD8137YR from the company Analog Devices seems to be applicable for an extra gain of five, while capable to drive a 120 Ohm terminated differential line. It has a typical voltage noise density of only 9 nV/sqrt(Hz) at 10 kHz. By using such an additional amplifier/driver, the quiescent power consumption of the preamplifier would increase to around 85 mW and a larger rise time of about 20 ns is expected at a detector capacitance of 22 pF. Also more space on the printed circuit board of the LNP-Preamp would be needed for such an additional amplifier.

The LNP-Preamp (Version SP 883a01) can handle detector capacitances in a range from 0 pF to 250 pF. To reach an optimal rise time, the frequency compensation of the amplifier can be tuned by a capacitor (see *Figure 3*). For different ranges of detector capacitances the frequency compensation must be matched. The actual frequency compensation is suitable for detector capacitances in a range of 0 pF to 100 pF. It results in a short rise-time of only 13 ns at a detector capacitance of 22 pF; this allows precise timing measurements. The anode of the VPT is connected to the LNP-Preamp via a short and shielded cable.

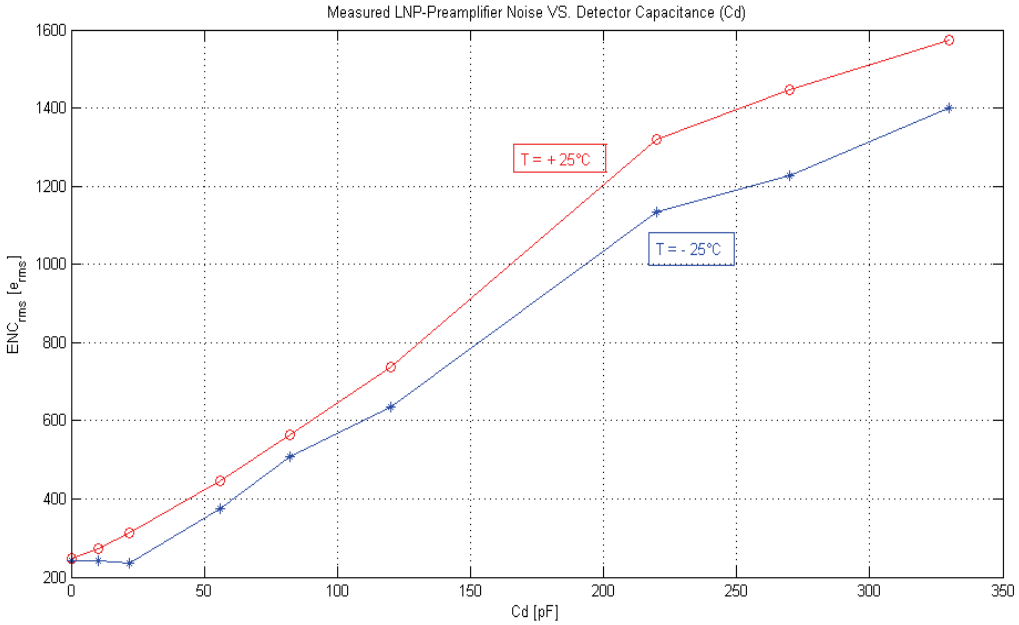

Figure 1: The measured noise performance of the LNP-Preamp versus the detector capacitance (C_d) at room temperature and at –25°C. Measurements are performed by using an ORTEC 450 Research Amplifier with T_{int} = 250 ns and T_{diff} = 2 µs which corresponds to a peaking-time of 650 ns. One can notice the strong decrease of the noise if the detector capacitance drops from 270 pF for a LAAPD, (1'250 e^-_{RMS}) to 22 pF for the VPT (235 e^-_{RMS}). At high event rates, a more adequate shaping filter with a peaking-time of 200 ns must be used; in that case the noise for a detector capacitance of 22 pF is increased by 25%, which results in an ENC of around 300 e^-_{RMS}.

3. CIRCUIT DESCRIPTION

The circuit diagram of the LNP-Preamp is shown in *Figure 2*. The AC-coupled input stage consists of a low noise J-FET of the type BF862 from the company NXP Semiconductors (former Philips). This industrial standard J-FET is often used in preamplifiers of car radio receivers. It is specified with a typical input voltage noise density of 0.8 nV/sqrt(Hz) at 100 kHz and at room temperature. The J-FET input capacitance is 10 pF and the forward transductance is typically 30 mS at a drain-source current (I_{DS}) of 5 mA. Along with the 470 Ohm AC-dominant drain resistor this transductance results in a typical AC-voltage gain of 14 for the J-FET input stage. The gate of the J-FET is protected against over voltages by two low leakage silicon diodes of the type BAS45AL.

The input stage is followed by a broadband (300 MHz), fast (2'000 V/µs) and low power (±1 mA) current feedback operational amplifier of the type AD8011AR from the company Analog Devices. With its typical input voltage noise density of only 2 nV/sqrt(Hz) at 10 kHz, this amplifier suits well for such a low noise design.

The proper frequency compensation is performed by the capacitor C13 (100 pF), in combination with R2 (10 Ohm); this leads to high frequency feedback to the inverting input of the operational amplifier. Overshoot and ringing can be efficiently suppressed and this compensation also prevents from oscillations when no VPT is connected.

The output of the operational amplifier is DC-coupled via the feedback network (1 pF // 25 Meg Ohm) to gate of the J-FET. In parallel the output is AC-coupled via a 1 µF capacitor and a 47 Ohm series resistor to the output of the LNP-Preamp. Therefore the output voltage is divided by a factor of two if it is terminated with 50 Ohm.

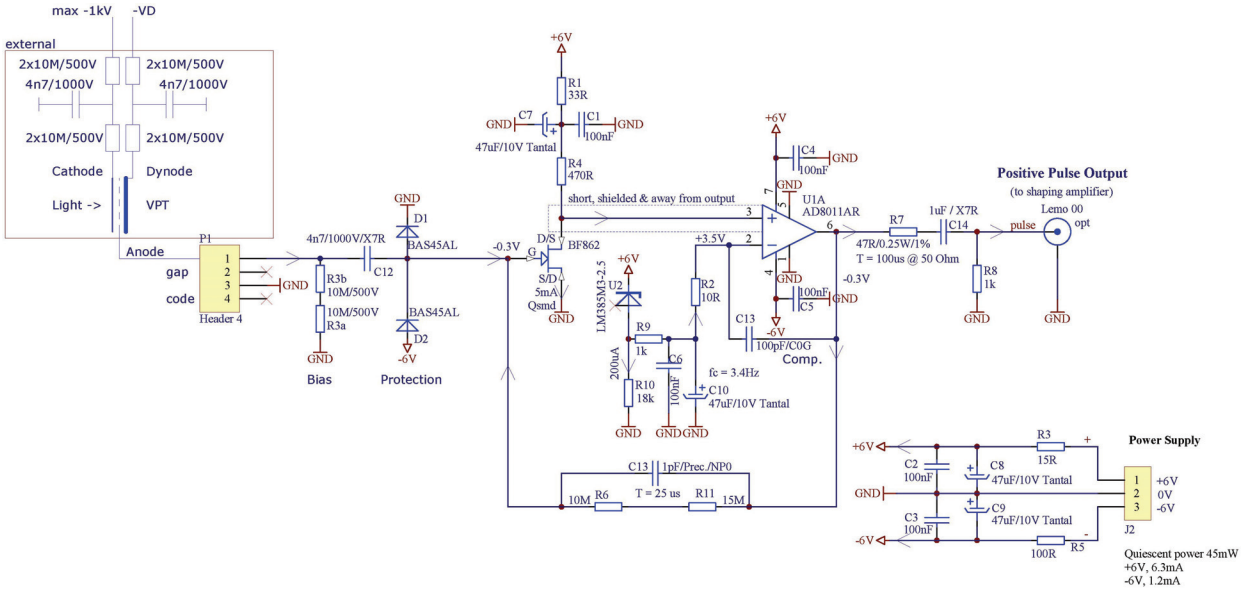

Figure 2: Circuit diagram of the LNP-Preamp prototype for the VPT readout. The flexibility of the discrete design allows easy modifications in the future development process. The HV filter indicated in the top left is not integrated on the preamplifier PCB. This is the revision 1 of the LNP-Preamp and it has the identification number SP 883a01.

With a symmetrical supply voltage of ±6 V the output voltage can swing symmetrically between the positive and negative supply when high continuous event rates at high energies occurs. The LNP-Preamp draws a typical quiescent current of 6.3 mA from the +6 V supply and 1.2 mA from the –6 V supply; this leads to a total power consumption of only 45 mW.

To set the 5 mA operating point of drain-source current through the J-FET, a gate voltage in a range of –0.2 V to –0.6 V (typically –0.3V, depending on the DC characteristics of the individual J-FET) has to be applied. This negative DC voltage is fed from the output of the operational amplifier via the 25 Meg Ohm resistor to the gate of the J-FET. The operating point (I_{DS}=5 mA) is fixed by the well filtered DC voltage applied to the inverting input of the operational amplifier. This set point voltage is obtained by subtracting 2.5 V from the positive supply voltage (+6 V) by using a 2.5 V reference diode. So the same voltage drop of 2.5V must also be present over the total drain resistor of 503 Ohm (470 Ohm + 33 Ohm); this results in a stabilized DC drain current of 5 mA.

As shown in *Figure 2* the anode of the VPT is referenced to ground by a 20 Meg Ohm resistor and the gate input of the J-FET is decoupled by a 4.7 nF high voltage capacitor.

As already discussed in the OVERVIEW (VTP BIAS VOLTAGES) the voltage drop over the LP filter for the VPT bias voltage has to be proven. At high rates in combination with high energies, a maximum current of 80 nA is flowing trough the VPT; mainly drawn from the dynode bias voltage supply. The planned series resistance of the LP filter is 40 Meg Ohm, resulting in a maximum voltage drop of 3.2 V. By using the typical gain sensitivity of 0.1% per volt of the VPT, this voltage drop corresponds to a maximum energy/rate error of –0.32%, which is acceptable. By reducing the series resistance of the LP filter, this energy/rate error could be further minimized.

SPICE SIMULATION

Spice is the abbreviation for Simulation program with integrated circuit emphasis; it allows simulating an electronic system in the time domain (pulse response) as well as in the frequency domain (noise behavior). A precise Spice model of the LNP-Preamp including the shaping filter (peaking-time 650 ns) has been developed.

Our circuit is based on the Spice models of the BF862 (March 2007, NXP Semiconductors) and the model of the AD8011 (Rev. A 1997, Analog Devices). The shaping filter is modeled noiseless by using the Laplace block from the analog behavioral modeling (ABM) library. All simulations are made with PSpice version 16.0 from the company Orcad/Cadence. The good agreement between the simulations and the measurements can be noticed in the *Figures 3* and *4*.

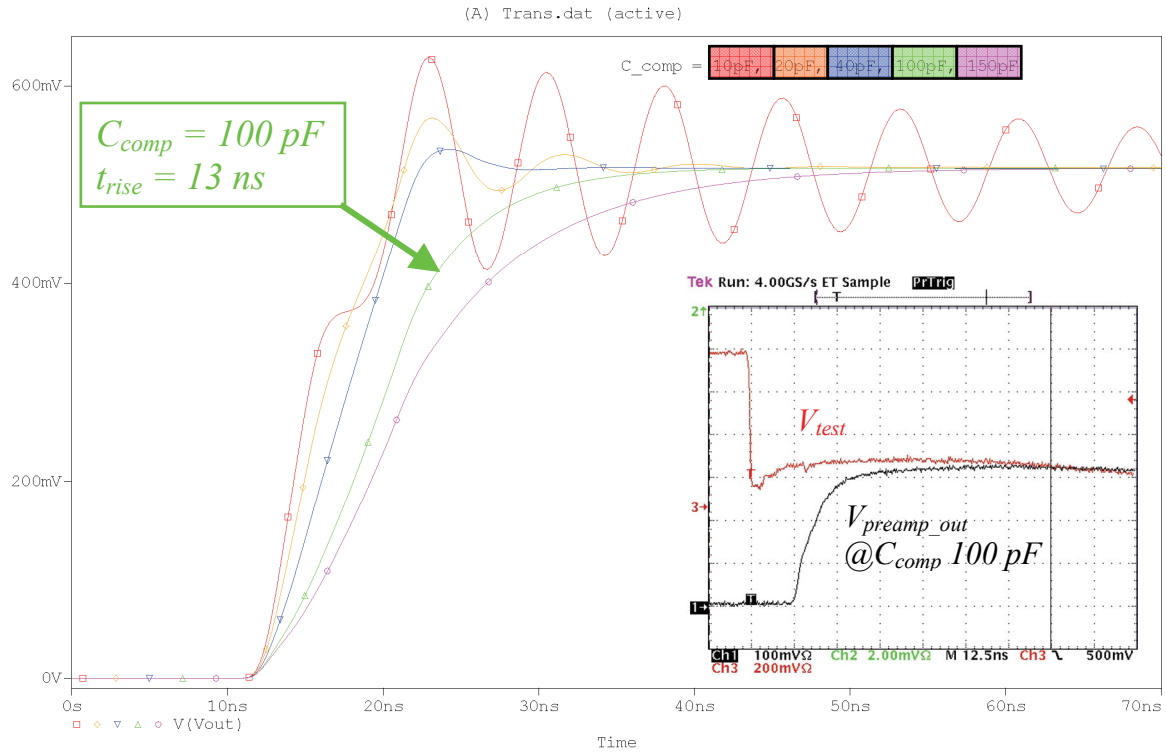

Figure 3: PSpice simulation of the rising edge of the LNP-Preamp output signal with a detector capacitance of 22 pF. The compensation capacitance (C13 in the cicuit diagram of Figure 2) is varied from 10 pF to 150 pF; the green curve shows the response with the chosen compensation capacitance of 100 pF, which leads to a rise time of 13 ns. With a capacitance of only 10 pF (red plot) one can notice the tendency for oscillation. The inset at the bottom right shows a measurement of the rising edge at the output of the LNP-Preamp, compensated with 100 pF. The measurement is in good accordance with the PSpice simulation (green curve).

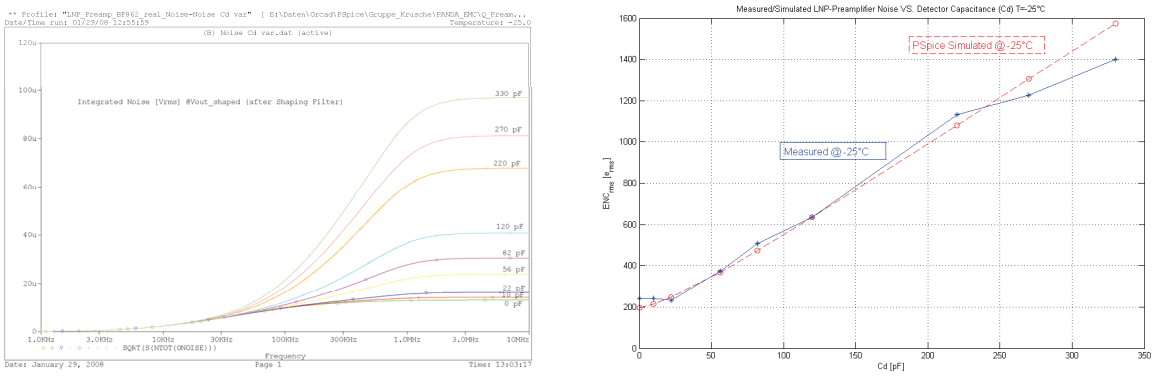

Figure 4: The left graph displays the PSpice simulated integrated output noise of the LNP-Preamp for different detector capacitances from 0 pF …330 pF. The right plot shows the simulated ENC versus the detector capacitance (dashed red) together with the measured ENC (blue line); both at –25°C. The simulation and the measurement are in very good agreement over the entire capacitance range.

4. IMPLEMENTATIONS AND COSTS

The LNP-Preamp is a simple, robust and low cost combination of a standard J-FET with a fast integrated operational amplifier. The single channel version of the LNP-Preamp prototype for the VPT readout is implemented on a small size double layer printed circuit board (PCB) with the mechanical dimensions of (48 x 18) mm^2 (see *Photo 1*). For a lot size of 1'000 units the expected cost of material is about 10 Euros per LNP-Preamp, without any cables. The production and handling costs (without testing) are around 2 Euros per piece.

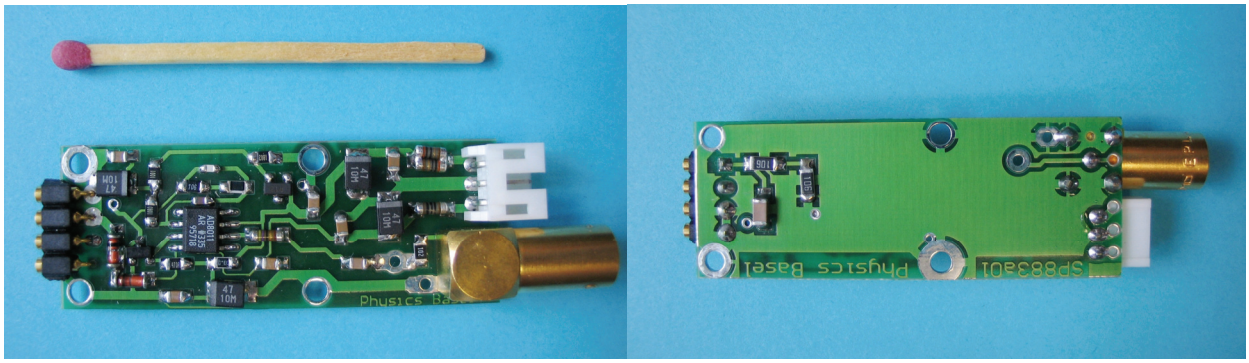

Photo 1: The top- and the bottom side of the single channel LNP-Preamp prototype for the VPT readout. It has a PCB size of (48 x 18) mm^2 and four holes (connected to ground) with a diameter of 2.3 mm are foreseen for mounting. The connector for the VPT is on the left side and the supply voltage (±6 V) is connected via the white socket on the right. For the testing phase a Lemo 00 connector is equipped at the signal output. On the bottom side the two 10 Meg Ohm HV resistors and the HV gate decoupling capacitor are located.

All components, except the connectors, are surface mount devices (SMD). Therefore the LNP-Preamp is well suited for automated mass production.

Due to the discrete design of the LNP-Preamp for the VPT readout, adaptations and modifications can be smoothly made in the future. For example, the power consumption can be easily reduced by changing only the value of two resistors. Of course, lowering the power consumption would also increase the noise level of the preamplifier.