

PHYSICS BASEL
ELECTRONIC LAB 2.17
KLINGELBERGSTR. 82
CH-4056 BASEL

SWITZERLAND

VERSION 2.8
31. MARCH 2008

DISCRETE PREAMPLIFIER FOR APD READOUT

LNP-PREAMPLIFIER VERSION SP 883A02

1. OVERVIEW

The Low Noise / Low Power Charge Preamplifier (LNP-Preamp) is a discrete charge preamplifier which has an excellent noise performance in combination with low power consumption. It is designed for the readout of the Large Area Avalanche Photo-Diodes (LAAPDs), developed for the Panda Electromagnetic Calorimeter (EMC). The LAAPDs are attached to the end face of the lead tungstate scintillating crystals (PWO-II) which have a typical geometry of $(200 \times 25 \times 25) \text{ mm}^3$. In contrary to a photomultiplier, the LAAPDs are also working in a strong electromagnetic field. In the barrel of the EMC the LAAPDs act as photo detectors converting the scintillating light to an electrical charge. The LNP-Preamp linearly converts the charge signal from the LAAPD to a positive voltage pulse which is transmitted via a 50 Ohm line to the subsequent electronics.

1.1. POWER CONSUMPTION

Since the complete barrel, together with the APDs and the preamplifiers, will be cooled to low temperatures (to increase the light-yield of the PWO-II crystals), the power dissipation of the preamplifier has to be minimized. Low power dissipation leads to a smaller cooling unit and thinner cooling tubes; it also helps to achieve a uniform temperature distribution over the length of the crystals. The LNP-Preamp has a quiescent power consumption of 45 mW. The power dissipation is dependent on the event rate and the photon energy; at very high rates combined with the maximum photon energy, the power consumption is increased up to 90 mW.

1.2. APD AND NOISE

To reach the required low detection threshold of only several MeV, the noise performance of the preamplifier is crucial. The LAAPD from Hamamatsu (Type S8664-1010) have an active area of $(10 \times 10) \text{ mm}^2$ resulting in a quite high detector capacitance which requires a low noise charge preamplifier. The total output noise is a combination of the preamplifier's noise and the noise generated by the dark current flowing through the APD. By cooling the APD to -25°C the dark current is reduced by a factor of about ten, with respect to room temperature. Using a low leakage LAAPD at low temperature, the charge preamplifier is the dominating noise source due to the relative high detector capacitance of around 270 pF. The noise floor of the LNP-Preamp at -25°C loaded with an input capacitance of 270 pF, has a typical equal noise charge (ENC) of $1'250 \text{ e}^-_{\text{RMS}}$. This is measured with an ORTEC 450 shaping filter/amplifier with a peaking-time of 650 ns.

When the LAAPD as well as the LNP-Preamp are cooled to -25°C the total output noise corresponds to an ENC of about $1'700 \text{ e}^-_{\text{RMS}}$, also measured with a peaking-time of 650 ns. Assuming 100 photons/MeV at the end face of the cooled (-25°C) PWO-II crystal would result in 16 photons/MeV on the active area of the LAAPD. This is coming from the fill factor of only 16%: LAAPD active area of 100 mm^2 with respect to an end face area of about 625 mm^2 . Since the end face not covered by the LAAPD will be masked by highly reflective material, we assume 25 photons/MeV on the LAAPD; this number is compatible with the measurements performed. Further the quantum-efficiency of the LAAPD is around 70% for the scintillating light of the PWO crystals. An internal gain (M) of 50 is presumed for the voltage

biased LAAPD. By applying these numbers, a primary photon with the energy of 1 MeV induces an input charge of 140 aC (875 e⁻) to the preamplifier. So an ENC of 1'700 e⁻_{RMS} corresponds to an energy noise level of about 2 MeV_{RMS}.

Radiation damage of the APD leads to a higher dark current and therefore also to a higher noise level. If the dark current is increased by a factor of six, due to radiation damage, the total output noise is then dominated by the APD dark current and the energy noise floor is doubled to about 4 MeV_{RMS}.

1.3. EVENT RATE

To cope with the expected event rates in the barrel of maximum 100 kHz per crystal, the LNP-Preamplifier has a concerted feedback time constant of 25 μs. This feedback time constant is a trade-off between noise performance and pile-up problematic.

For a single pulse (or very low rates) the LNP-Preamplifier accepts an input charge of up to 4 pC; for a continuous event rate of 100 kHz an input charge of up to 8 pC is allowed. This discrepancy is due to the following reason: A single output pulse starts from zero output voltage and is limited by the positive supply voltage (+6 V) of the LNP-Preamplifier. At high continuous event rates the output pulses will swing between the negative (-6 V) and the positive (+6 V) supply voltage; therefore the maximum input charge is doubled. If a 100 kHz event rate is applied abruptly (burst) to the LNP-Preamplifier it takes around one second until a continuous input charge of up to 8 pC is allowed. During that transition period, a maximum input charge of 1 pC can be handled. With this charge restriction, the output voltage of the preamplifier stays always in the linear range and is never limited from the power supply voltages. Nevertheless, the electronics after the preamplifier has to perform a good base-line correction, because at higher rates it is likely that one pulse sits on the trailing edge of the previous one.

If a charge of 140 aC/MeV is assumed from the LAAPD (see section APD and Noise) the maximum expected photon energy of 10 GeV results in an input charge of 1.4 pC. Since at such energies the primary photon will induce showers in the neighboring crystals and the energy will be distributed on several crystals; that's why even the maximum 1 pC input charge for a burst at 100 kHz should be sufficient.

1.4. APD BIAS VOLTAGE AT HIGH EVENT RATES

At the maximum event rate of 100 kHz with the maximum expected photon energy of 10 GeV (1.4 pC from the LAAPD) a mean current of 140 nA is flowing through the LAAPD. Under these extreme conditions, the voltage drop over the low-pass filter for the APD bias voltage gets relevant, since the internal gain (M) of the LAAPD varies about 3% per volt.

This means, that the measured energy will be dependent on the event rate. To minimize this effect one can design the low-pass filter with low series resistance resulting in a degraded noise performance of the preamplifier and the need for larger filter capacitors. Eventually, the various regions of the barrel with different event rates could be equipped with adapted low-pass filters to obtain an optimum noise performance combined with low rate/energy dependence.

Another solution is that the APD bias-voltage supply sources a voltage which is corrected on the output current (the more current the more voltage). This means the output resistance of the bias-voltage supply is negative and therefore compensating the series resistance of the low-pass filter. The advantage is a better noise performance of the preamplifier due to the highly resistive APD bias-voltage filter. This solution would demand a more complex bias-voltage supply system with a sophisticated overvoltage and overload control. Each LAAPD has its own measured bias voltage where it reaches the nominal internal gain of M=50. To reduce the number of APD bias-voltage channels, it is foreseen to group LAAPDs with similar bias-voltages. Since this grouping will be very locally, where similar event rates are expected, the solution with the negative resistance bias-supply could still be feasible.

1.5. DYNAMIC RANGE

As explained in the section Event Rate, the LNP-Preamplifier is designed for a single pulse charge input of maximum 4 pC. With an input charge of 140 aC/MeV coming from the LAAPD (see section APD and Noise) this corresponds to a maximum photon energy of 28 GeV. Therefore the dynamic range of the

LNP-Preamplifier is restricted by the noise floor only. That's why the specification of a dynamic range is strongly dependent on the applied shaping filter.

In principle, the energy range of the LNP-Preamplifier spans from the noise floor of $2 \text{ MeV}_{\text{RMS}}$ (with a peaking-time of 650 ns, see section APD and Noise) up to the maximum energy of 28 GeV; this corresponding to a theoretical dynamic range of 14'000. In practice, the typical energy range will start from 4 MeV ($2 * \sigma_{\text{noise}}$) and end at 10 GeV which corresponds to a dynamic range of 2'500.

1.6. TRADITIONAL READOUT

If a peak-sensing analog to digital converter (ADCs) is used for the energy readout, the needed baseline correction is performed by the shaping filter/amplifier, which is installed between the preamplifier and the peak-sensing ADC. For our application, a reasonable peaking-time is between 250 ns and 500 ns. Longer peaking-times result in better noise performance, but they suffer from worse double pulse accuracy. The best signal to noise performance of the LNP-Preamplifier, attached to a LAAPD (at -25°C) is reached for a peaking-time of 6 μs . This is not compatible with the expected maximum event rates in the barrel crystals at small angles in forward direction. For good timing information a timing amplifier with a peaking-time between 20 ns and 100 ns seems to be suitable in front of a constant fraction discriminator (CFD). With that scheme one can easily reach a timing resolution of better than 2 ns for energies above 200 MeV.

1.7. FADC READOUT

Readout with a flash ADC (FADC) does not need a dedicated shaping and timing amplifier. Only a good anti aliasing low-pass filter/amplifier has to be implemented in front of the FADC. The cut-off frequency of that filter is given by the sampling frequency of the FADC divided by 2.5; this prevents from aliasing effects due to the sampling.

To determine the energy with a high signal to noise ratio the digitized values are processed by a digital shaping filter followed by a digital peak determination. It could be possible to choose different digital energy shaping filters for the different regions of the barrel: A short peaking-time for the small angles in forward direction and the region orthogonal to the target position, where high event rates are expected. For other regions of the detector where smaller event rates are estimated, the peaking-time could be larger and therefore resulting in a better energy resolution. Even a rate dependent automatically adaptation of the digital energy shaping filter could be imagined.

The timing information is extracted by processing the digitized values similarly to the traditional signal chain with a fast digital timing filter followed by a digital implemented CFD. Measurements have shown, that a timing resolution well below 1 ns can be reached with that regime.

One has to point out, that the processing for the energy- and timing information extraction must be performed in real time. This can be implemented by using programmable digital signal processors (DSPs) or complete in hardware by using field programmable gate arrays (FPGAs). The needed signal throughput at the high sampling frequency (50 MHz - 100 MHz) combined with the complex algorithm will result in a remarkable power dissipation.

2. PERFORMANCE & SPECIFICATIONS

The LNP-Preamplifier (Version SP 883a02) is a further development of the charge preamplifier described in the section 8.5.2 on page 204ff in the "Panda Technical Progress Report, February 2005". Some modifications on the circuit are made and a couple of components are changed to SMD types.

A summary of the LNP-Preamplifier (Version SP 883a02) performance and specifications is given below:

- J-FET (BF862, NXP Semiconductors) in combination with a low power, high-speed current-feedback operational amplifier (AD8011AR, Analog Devices)
- Supply +6 V@6.3 mA, -6 V@1.2 mA → 45 mW quiescent power consumption
- (Supply +8V@6 mA, -2 V@1 mA → 50 mW quiescent power consumption)
- Rise-time:
 - $C_d = 82 \text{ pF}$: 10 ns
 - $C_d = 270 \text{ pF}$: 18 ns
- Feedback time-constant: 25 μs
- Gain: 0.5 V/pC at 50 Ohm termination
 - Maximum single pulse input charge: 4 pC ($\pm 6 \text{ V}$ supply)
 - Maximum 100 kHz burst input charge: 1 pC ($\pm 6 \text{ V}$ supply)
 - Maximum continuous 100 kHz input charge: 8 pC ($\pm 6 \text{ V}$ supply)
- APD bias voltage (up to +500 V) filtering on the bottom side of the PCB: $f_c = 3.4 \text{ Hz}$
- Single channel LNP-Preamplifier version: PCB size (48 x 18) mm^2
- Quad LNP-Preamplifier version: PCB size (46 x 46) mm^2
- Typical noise performance (Shaping $T_{\text{int}} = 250 \text{ ns}$ / $T_{\text{diff}} = 2 \mu\text{s}$ → Peaking-time 650 ns)
 - $C_d = 82 \text{ pF}$: $\text{ENC} = 510 \text{ e}^-_{\text{RMS}}$ @ -25°C
 - $C_d = 270 \text{ pF}$: $\text{ENC} = 1'250 \text{ e}^-_{\text{RMS}}$ @ -25°C

The single ended output of LNP-Preamplifier is designed to drive a 50 Ohm transmission line. The charge sensitivity is 0.5 V/pC and so the maximum input charge of 4 pC corresponds to a positive output pulse with a peak voltage of 2 V at 50 Ohm.

The LNP-Preamplifier (Version SP 883a02) can handle detector capacitances in a range from 0 pF to 500 pF. Therefore it is applicable for different types of APDs including the (10 x 10) mm^2 LAAPDs with a detector capacitance of 270 pF. Future larger APDs with higher capacitances can be readout by this preamplifier. To reach an optimal rise time, the frequency compensation of the amplifier can be tuned by a capacitor. For different ranges of detector capacitances the frequency compensation must be matched. The actual frequency compensation is suitable for detector capacitances in a range of 100 pF to 300 pF. It results in a short rise-time of only 18 ns at a detector capacitance of 270 pF. Due to the intrinsic internal series resistor of the LAAPD the rise-time with that photo detector is increased to around 28 ns; this still allows precise timing measurements. The LAAPD can be either directly plugged onto the LNP-Preamplifier or it can be connected by a short and shielded cable.

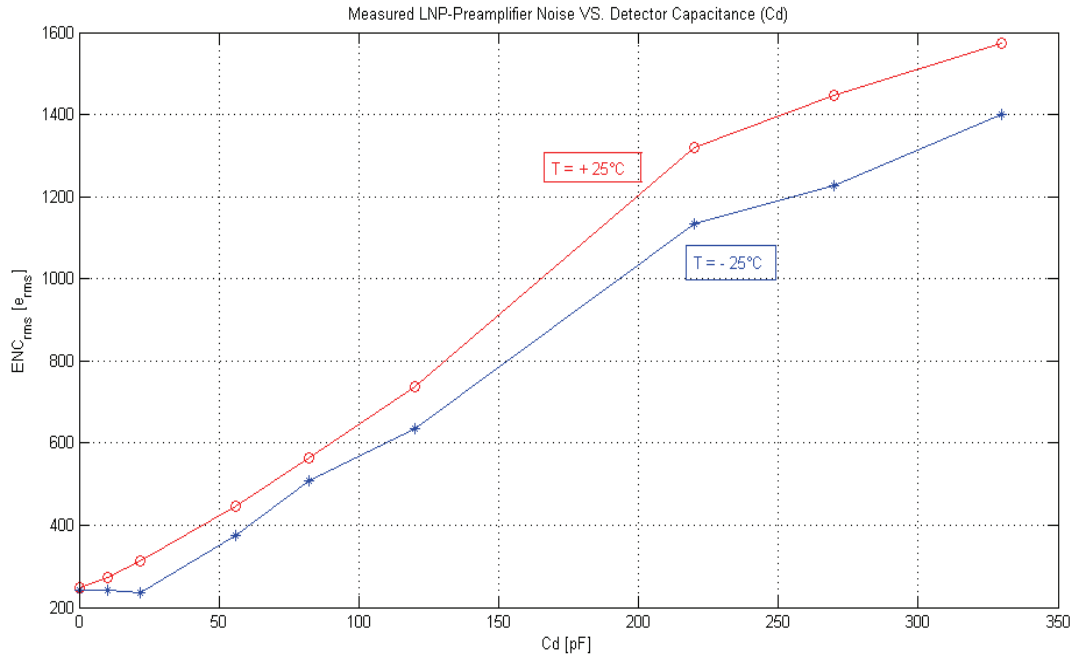


Figure 1: The measured noise performance of the LNP-Preamp versus the detector capacitance (C_d) at room temperature and at -25°C . Measurements are performed by using an ORTEC 450 Research Amplifier with $T_{\text{int}} = 250 \text{ ns}$ and $T_{\text{diff}} = 2 \mu\text{s}$ which corresponds to a peaking-time of 650 ns .

By cooling the LNP-Preamp to -25°C the noise level at $C_d = 270 \text{ pF}$ is decreased by around 15% with respect to room temperature (see Figure 1). As mentioned before, a much bigger noise improvement results from the smaller dark current of the APD at lower temperature. For an internal APD gain of $M=50$ the noise is reduced from around $4'000 \text{ e}_{\text{RMS}}$ to $1'700 \text{ e}_{\text{RMS}}$ by lowering the temperature from $+25^\circ\text{C}$ to -25°C (see Figure 2).

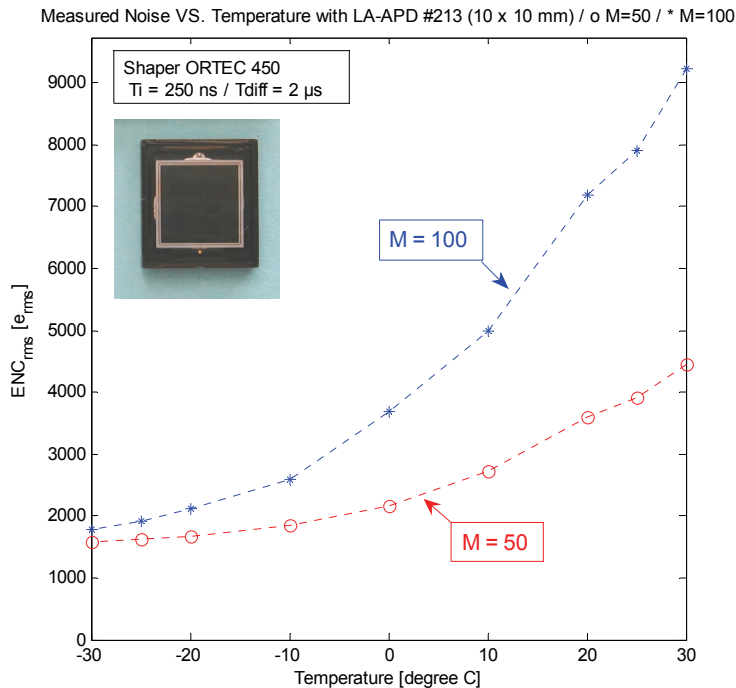


Figure 2: The measured noise of the LNP-Preamp connected to a LAAPD versus temperature at two different internal APD gains of $M=50$ and $M=100$. At room temperature the main noise source is the dark current of the LAAPD. The photo at the top left shows the front face (active area) of the LAAPD.

3. CIRCUIT DESCRIPTION

The circuit diagram of the LNP-Preamplifier is shown in *Figure 3*. It is the same circuit for the single channel- and the Quad LNP-Preamplifier, except that for the quad version the voltage reference (U2) and its supply (R10, C6) is common for all the four channels.

The AC-coupled input stage consists of a low noise J-FET of the type BF862 from the company NXP Semiconductors (former Philips). This industrial standard J-FET is often used in preamplifiers of car radio receivers. It is specified with a typical input voltage noise density of 0.8 nV/sqrt(Hz) at 100 kHz and at room temperature. The J-FET input capacitance is 10 pF and the forward transconductance is typically 30 mS at a drain-source current (I_{DS}) of 5 mA. Along with the 470 Ohm AC-dominant drain resistor this transconductance results in a typical AC-voltage gain of 14 for the J-FET input stage. The gate of the J-FET is protected against over voltages by two low leakage silicon diodes of the type BAS45AL.

The input stage is followed by a broadband (300 MHz), fast (2'000 V/ μ s) and low power (± 1 mA) current feedback operational amplifier of the type AD8011AR from the company Analog Devices. With its typical input voltage noise density of only 2 nV/sqrt(Hz) at 10 kHz, this amplifier suits well for such a low noise design.

The proper frequency compensation is performed by the capacitor C13 (47 pF), in combination with R14 (10 Ohm); this leads to high frequency feedback to the inverting input of the operational amplifier. Overshoot and ringing can be efficiently suppressed and this compensation also prevents from oscillations when no APD is connected or unshielded wires are used between the LNP-Preamplifier and the APD.

The output of the operational amplifier is DC-coupled via the feedback network (1 pF // 25 Meg Ohm) to gate of the J-FET. In parallel the output is AC-coupled via a 1 μ F capacitor and a 47 Ohm series resistor to the output of the LNP-Preamplifier. Therefore the output voltage is divided by a factor of two if it is terminated with 50 Ohm.

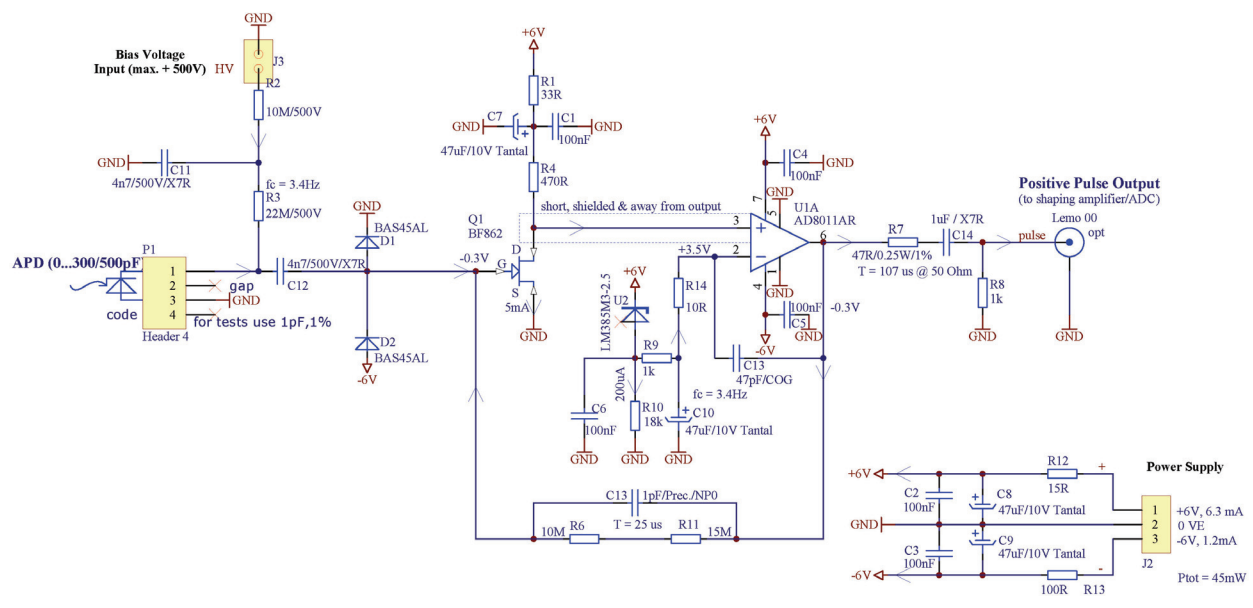


Figure 3: Circuit diagram of the LNP-Preamplifier for the APD readout. At the top left the high voltage LP filter for the APD bias is indicated. This charge sensitive preamplifier is a simple and compact circuit consisting of a low noise J-FET coupled to high performance integrated operational amplifier. The flexibility of the discrete design allows easy modifications in the future development process. This is the revision 2 of the LNP-Preamplifier and it has the identification number SP 883a02.

With a symmetrical supply voltage of ± 6 V the output voltage can swing symmetrically between the positive and negative supply when high continuous event rates at high energies occurs (see Figure 4). The LNP-Preamp draws a typical quiescent current of 6.3 mA from the +6 V supply and 1.2 mA from the -6 V supply; this leads to a total power consumption of only 45 mW. Operating with an asymmetric supply voltage of +8V and -2V gives more restrictions at high continuous event rates, but is principally possible; it results in a little higher power consumption of 50 mW.

To set the 5 mA operating point of drain-source current through the J-FET, a gate voltage in a range of -0.2 V to -0.6 V (typically -0.3V, depending on the DC characteristics of the individual J-FET) has to be applied. This negative DC voltage is fed from the output of the operational amplifier via the 25 Meg Ohm resistor to the gate of the J-FET. The operating point ($I_{DS}=5$ mA) is fixed by the well filtered DC voltage applied to the inverting input of the operational amplifier. This set point voltage is obtained by subtracting 2.5 V from the positive supply voltage (+6 V) by using a 2.5 V reference diode. So the same voltage drop of 2.5V must also be present over the total drain resistor of 503 Ohm (470 Ohm + 33 Ohm); this results in a stabilized DC drain current of 5 mA.

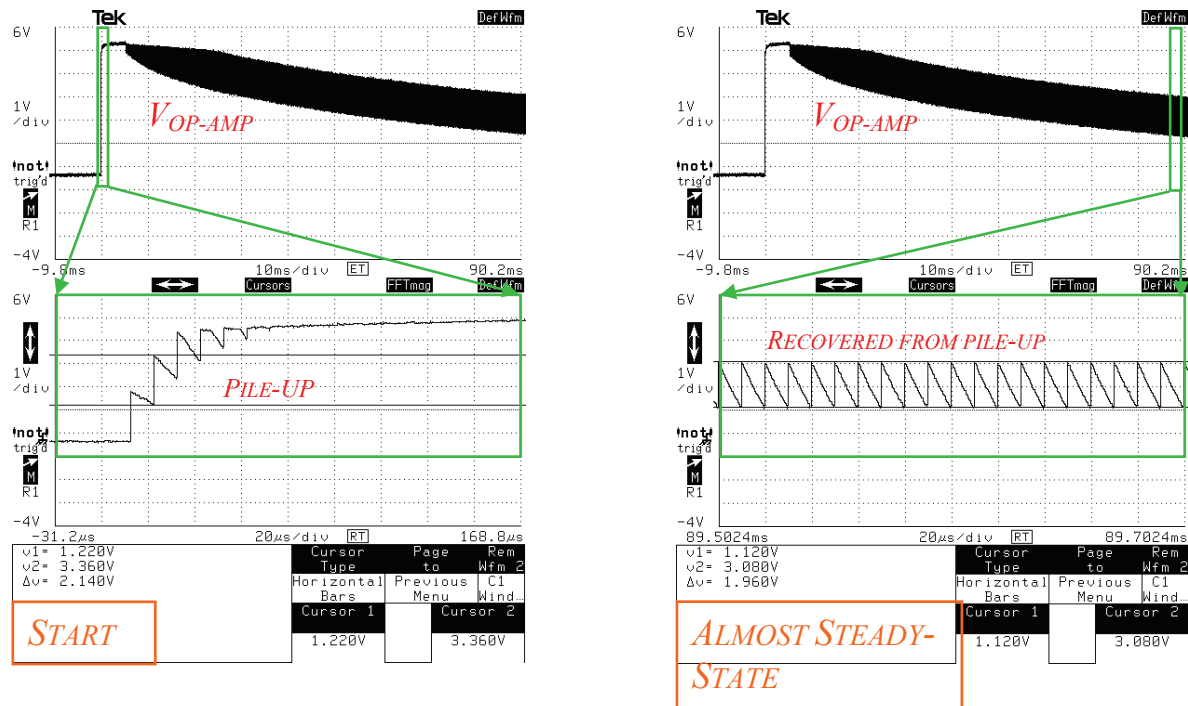


Figure 4: Measurement with a fast LED-pulsar and an APD connected to the LNP-Preamp; the signal (V_{OP-AMP}) is measured directly at the output of the operational amplifier (pin 6). A DC voltage of -0.3 V lies at that node; this is the typical gate voltage for an I_{DS} of 5 mA. During a 100 kHz burst with an input charge of 2.1 pC the pile-up and its recovery is recorded. The burst is switched on at $t=10$ ms and the left picture shows a zoom into this start point, where the pile-up to the positive supply voltage occurs. After around 30 ms the preamplifier recovers from the pile-up and slowly starts to restore the initial mean DC value of -0.3 V; this happens with a time-constant of about 200 ms. Then the output voltage will swing symmetrically around this gate operating point of typical -0.3V. The right graph shows the recovery after 90 ms. Due to the voltage drop over the low-pass filter (for the APD bias) the internal gain of the APD is reduced and the signal amplitude is already around 10% smaller. As the APD bias filter has also a time-constant of around 200 ms, the signal will be even more reduced when it reaches the steady state condition after around one second.

The APD bias voltage is low-pass (LP) filtered by a 10 Meg Ohm resistor and a 4.7 nF high voltage (HV) capacitor which results in a cut-off frequency of 3.4 Hz. After this LP filter the bias voltage is fed via a 22 Meg Ohm resistor to the cathode of the APD; the anode of the APD is wired to ground. The gate input of the J-FET is also decoupled by a 4.7 nF high HV capacitor. A maximum APD bias voltage of +500 V can be applied and the total leakage current of the circuit under dry and clean conditions is below 2 nA.

As already discussed in the OVERVIEW (APD BIAS AT HIGH EVENT RATES) the voltage drop over the LP filter is critical at high event rates in combination with high energy; a maximum current of 140 nA is then flowing through the APD. The actual series resistance of the LP filter is 32 Meg Ohm, resulting in a maximum voltage drop of 4.5 V. By applying the typical gain sensitivity of 3% per volt of the LAAPD, this voltage drop corresponds to an energy error of -13.5%, which is not acceptable (see *Figure 4*). Reducing the series resistance of the LP filter to 1 Meg Ohm will diminish this energy/rate error below -0.5%, but the noise of the preamplifier will increase by 15%. Using the same filter capacitor with 4.7 nF, the cut-off frequency will increase to 103 Hz; which will also worsen the noise performance. This cannot be exactly specified, because it is depending on the noise characteristics of the bias-voltage supply. Larger HV filter capacitors would consume more space on the PCB.

These drawbacks could be bypassed when using a special APD bias-voltage supply system with a current dependent output voltage resulting in a negative output resistance (see OVERVIEW).

4. SPICE SIMULATION

A precise Spice model of the LNP-Preamplifier including the shaping filter (peaking-time 650 ns) has been developed. Spice is the abbreviation for Simulation program with integrated circuit emphasis; it allows simulating an electronic system in the time domain (pulse response) as well as in the frequency domain (noise behavior).

Our circuit is based on the Spice models of the BF862 (March 2007, NXP Semiconductors) and the model of the AD8011 (Rev. A 1997, Analog Devices). The shaping filter is modeled noiseless by using the Laplace block from the analog behavioral modeling (ABM) library. All simulations are made with PSpice version 16.0 from the company Orcad/Cadence. The good agreement between the simulations and the measurements can be noticed in the *Figures 5* and *6*.

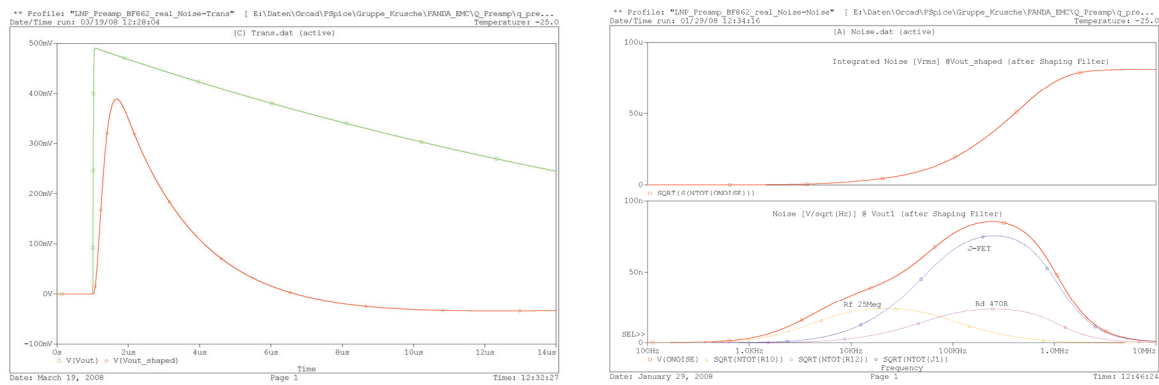


Figure 5: The left part shows the result of a PSpice time domain simulation with an input charge of 1 pC. In green the output signal from the LNP-Preamplifier ($V_{out\ peak} = 500\ mV_p$) and in red the pulse after the shaping filter ($V_{out\ shaped} = 390\ mV_p$) is plotted; the shaping filter has a peaking time of 650 ns. The right graph illustrates a noise simulation in the frequency domain with a detector capacitance of 270 pF. With the curves in the lower part, the impact of the different noise sources to the total output noise (in red) can be studied; the y-axis is a noise density with the unit V/\sqrt{Hz} . It is obvious that the noise from the J-FET is the dominating noise source. The red curve in the upper part is the integrated output noise which results in $82\ \mu V_{RMS}$. This value in respect to the $390\ mV_p$ for an input charge of 1 pC corresponds to a simulated ENC of $1'300\ e^-_{RMS}$, which is in very good agreement with the measurement. Notice that the temperature of the simulation, as well as the noise measurements, is performed at $-25^\circ C$.

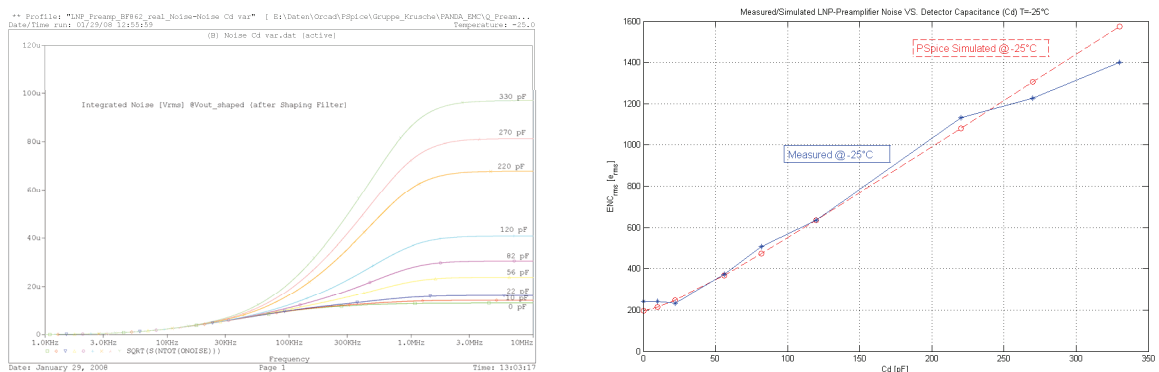


Figure 6: The left graph displays the PSpice simulated integrated output noise of the LNP-Preamplifier for different detector capacitances from 0 pF ... 330 pF. The right plot shows the simulated ENC versus the detector capacitance (dashed red) together with the measured ENC (blue line); both at $-25^\circ C$. Over the whole capacitance range the simulation and the measurement are in very good agreement.

5. IMPLEMENTATIONS AND COSTS

The LNP-Preamplifier is a simple, robust and low cost combination of a standard J-FET with a fast integrated operational amplifier. A low-pass (LP) filter for the APD bias voltage of up to +500 V is an integral part of the device. The single channel version of the LNP-Preamplifier is implemented on a small size double layer printed circuit board (PCB) with the mechanical dimensions of $(48 \times 18) \text{ mm}^2$ (see *Photo 1*). For a lot size of 1'000 units the expected cost of material is about 10 Euros per LNP-Preamplifier, without any cables. The production and handling costs (without testing) are around 2 Euros per piece.

This single channel version has been successfully used for the readout of the (3×3) and the (5×5) PWO-II crystal matrixes with LAAPDs.

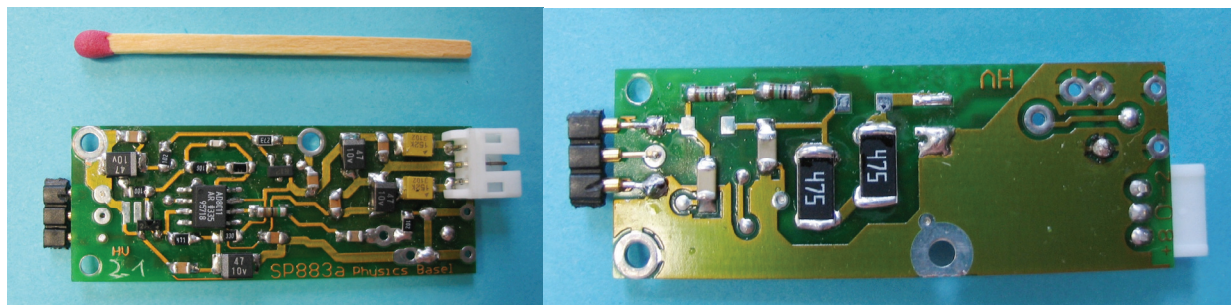


Photo 1: The top- and the bottom side of the single channel LNP-Preamplifier PCB $(48 \times 18) \text{ mm}^2$. The connector for the APD is on the left side and the supply voltage ($\pm 6 \text{ V}$) is connected via the white socket. On the bottom side the APD bias voltage is connected and low-pass filtered with the HV components.

The four channel version (Quad LNP-Preamplifier) consists of four independent LNP-Preamplifiers on one PCB. It has also four separate APD bias voltage LP filters and it covers a PCB size of $(46 \times 46) \text{ mm}^2$. This quad version is installed in the 60 crystals prototype (Proto60) of the Panda EMC (see *Photo 2*).

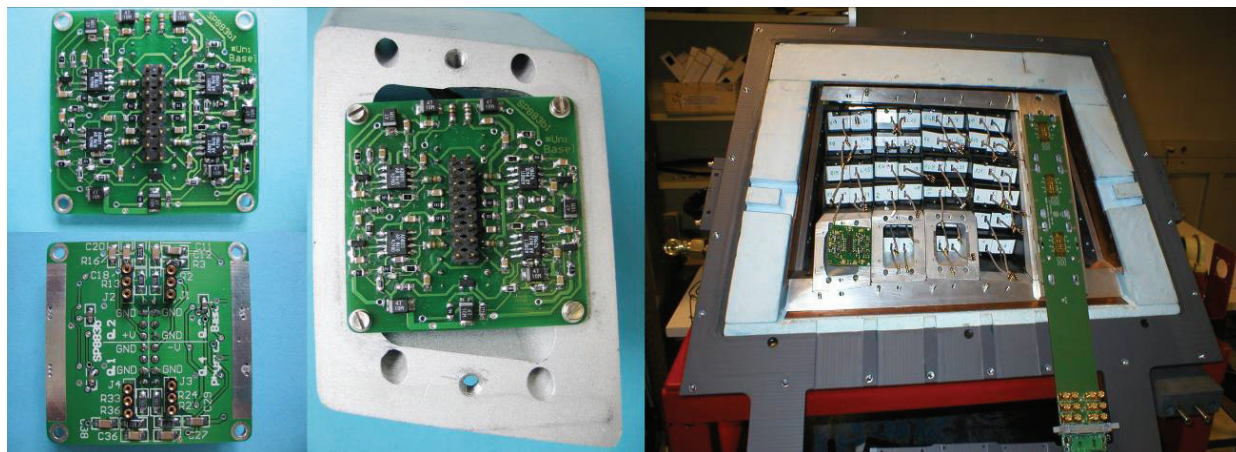


Photo 2: Left: The PCB (top- and bottom side) of the Quad LNP-Preamplifier with the dimension of $(46 \times 46) \text{ mm}^2$; at the bottom one can recognize the four connectors for the APDs. Center: The Quad LNP-Preamplifier is mounted on the aluminum insert of the Proto60 detector. In the center one can see the 2.54 mm spacing connector for the low voltage supply ($\pm 6 \text{ V}$ or $+8 \text{ V}$, -2 V), the four APD bias voltages and the four output signals. This connector fits into the Proto60-backplane which leads the signals through the thermal isolation. The four fast output signals are wired by 50 Ohm impedance strip-lines on the backplane. Right: The back side of the partially equipped Proto60 detector with one backplane already mounted for the most left three Quad LNP-Preamplifiers.

All components of both preamplifiers (single channel and quad), except the connectors, are surface mount devices (SMD). Therefore the LNP-Preamp is well suited for automated mass production. The expected cost of material are 35 Euros per Quad LNP-Preamp with no cables included; this is also calculated for a lot size of 1'000 pieces. In addition the production and handling (without testing) will charge about 5 Euros per Quad LNP-Preamp.

Due to the discrete design of the LNP-Preamp, adaptations and modifications can be smoothly made in the future. For example, the power consumption can be easily reduced by changing only the value of two resistors. Of course, lowering the power consumption would also increase the noise level of the preamplifier.