Low mass aluminium microstrips for data transmission in the Micro Vertex Detector of the Panda experiment

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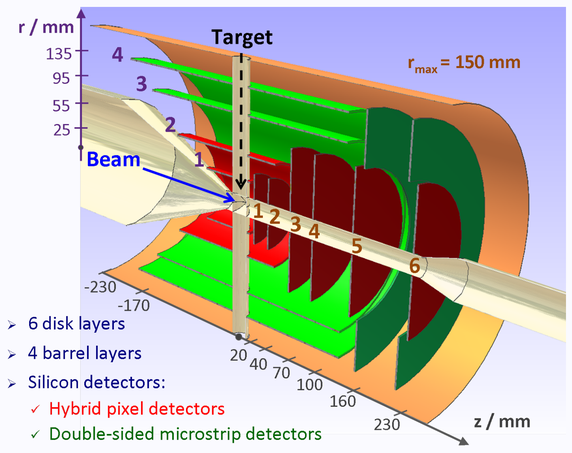
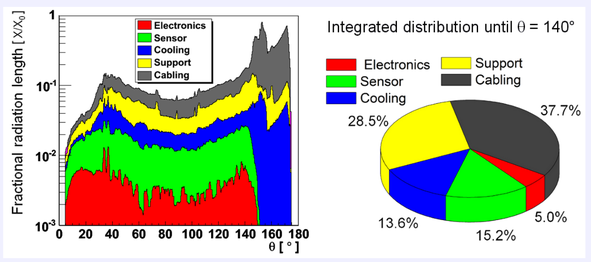
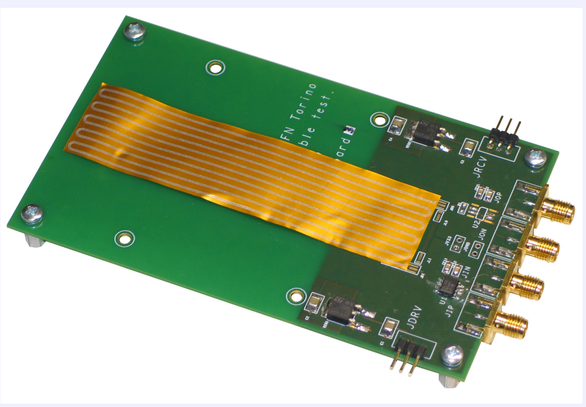
The Micro Vertex Detector (MVD) is the innermost one in the antiProton ANnihilation at DArmstadt (Panda) experiment. It features 4 coaxial barrels (two with hybrid pixel sensors at small radii and two with strip sensors at large radii), and 6 forward disks (all disks are made with hybrid pixels and the last two are completed by a ring of strips). The routing regarding all the cables for the electrical signals and the pipes for the cooling water must be performed in the backward zone, that is the only way out for the micro vertex services. In the backward direction all cables and pipes have to be distributed along a narrow circle enclosing the large beam pipe.

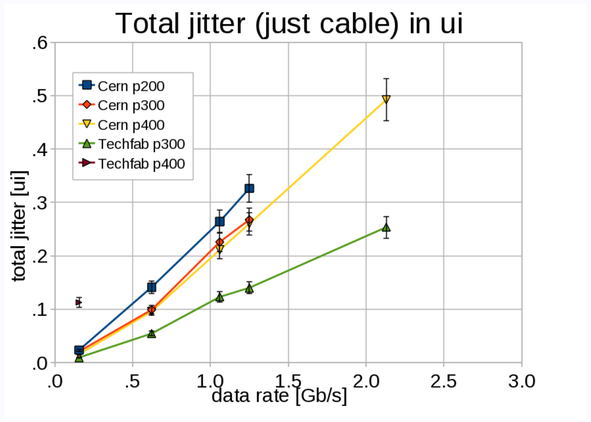


Due to the low momentum particles, the material budget is very limited. Representing it as a fraction of the total radiation length, it must be kept down to a value of about 10^{-1} taking into account all the parts making up the detector (sensor, cooling, support, cabling, ..) and every direction from the interaction point. The simulation shows that the component responsible for the most of the material budget is the cabling (roughly 40%), and for this reason the actual layout foresees that the long interconnections are made in aluminium instead of standard copper that have a radiation length respectively of 88.9 and 14.4 mm.



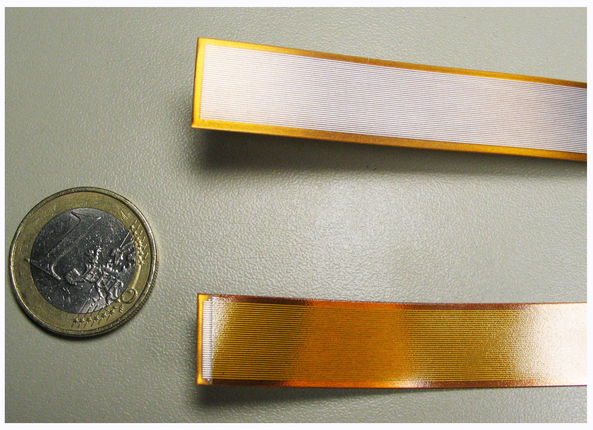


Different technologies were investigated exploiting the aluminium lamination (performed at the Cern workshop), and aluminium deposition (performed at the Techfab company). In both cases the samples feature a differential pair 1 m long in a folded layout, implemented as a differential microstrip with tracks widths in the range 100÷200 μm and same spacing, thus producing a final pitch in the range 200÷400 μm. The insulator layer, between the tracks and the reference plane, is made in polyimide and presents an overall thickness of roughly 50 μm.

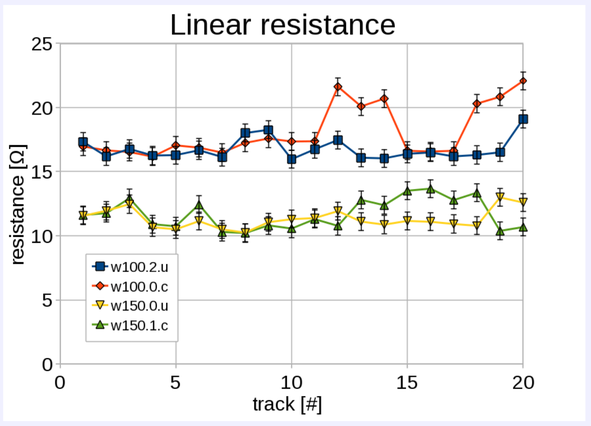


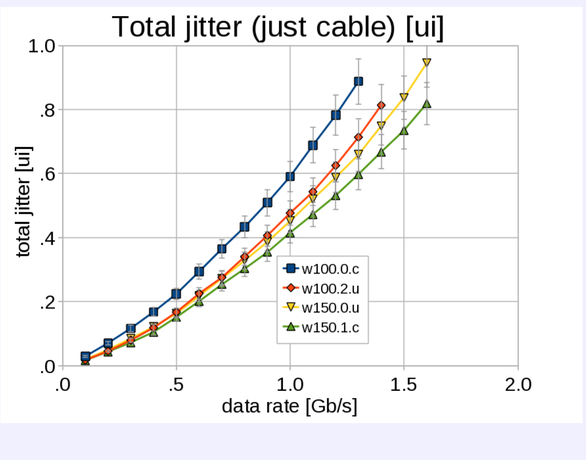
The sample has been assembled on a test board by a conductive glue to provide a ground reference, while the differential pair has been connected by wire bonds. The input signal generated by a pulser can be injected directly, or buffered with a transceiver. Considering safe a communication channel where the total jitter represents about the 30% of the unit interval (.3 ui), the cables can be used with a data rate around 1 Gb/s. The Techfab sample looks the best one, but shows many problem during the wire bonding procedure.

The next step has been the development of some aluminium flexcable 1 m long in straight layout, with tracks 100 μm and 150 μm width and the same spacing. In both these cases the cable carries 36 independent tracks, and has been manufactured with and without a thin cover layer to allow the stacking of some samples. The top and bottom aluminium layers have a thickness of 15 μm while the insulator sheet is polyimide 75 μm thick, and the layout foresees a nominal differential impedance of roughly 100Ω.

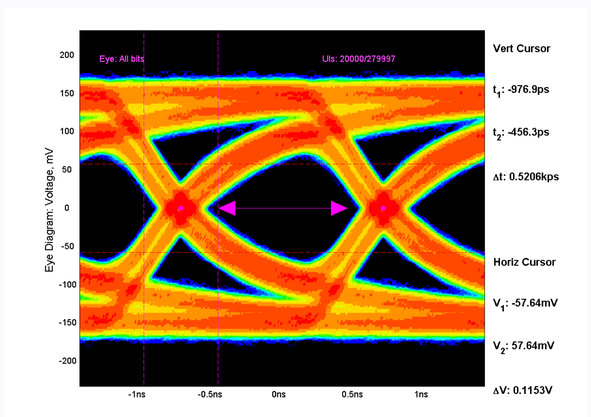


From a static point of view the linear resistance has been evaluated to study the possible dependence from the track position along the transverse section, from the outer location to the inner one. The measurement has been performed bonding both ends of the tracks to a test station, to reduce the contact problems. The result shows that the track linear resistance is quite stable and there is no correlation with the position; the same happens to the capacitance parameter.

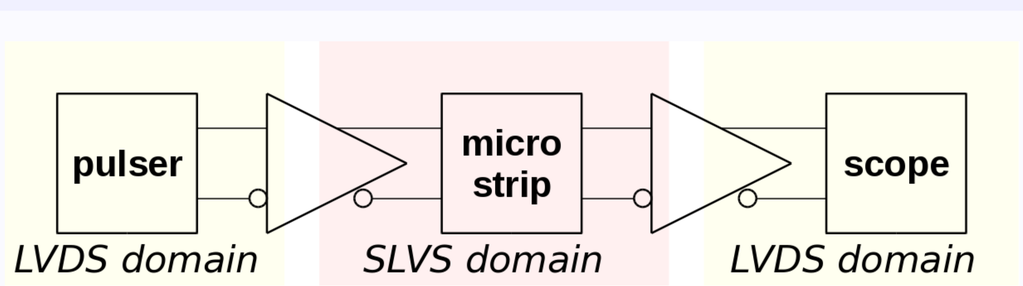




Regarding the dynamic performances, the cable without any transceivers has been measured to evaluate the working range. For these flexcables with 18 differential pairs, the threshold value of about .3 ui for the total jitter is reached with a data rate of roughly 600 Mb/s; the microstrips with larger width can run at a slight higher speed. The input test signal respects the Scalable Low Voltage Signaling (SLVS) standard.



The microstrips have been tested by a Pseudo Random Binary Sequence (PRBS), with a pattern 2^{23}-1 bit long. From the acquired bits and the relative eye diagram, it is evident the effect due to the distributed R and C components. Besides, it is clear the differential amplitude reduction caused by the linear resistance, that produces a value of about 300 mV instead of 400 mV.



The test has been accomplished with an SLVS signal, since that was chosen for the serial communication between the readout and the optical converter. A CERN group has designed a level translator from the common Low Voltage Differential Signaling (LVDS) to SLVS. A rad hard implementation (crt700) has been tested and applied at the input and output of the differential pair under test.

The whole channel, composed by the cable and the SLVS transmitter and receiver, has been measured for the total jitter, and at present the system works below the safety value of .3 ui for a data rate up to 260 Mb/s. That is good enough to run with the current prototype Topix3, but the SLVS transceiver has to improve his performances to reach the required serial speed of 320 Mb/s for the final readout Asic.