PANDA MVD

Sezione di Torino

The silicon pixel system for the Micro Vertex Detector of the PANDA experiment

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Outline

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- The PANDA experiment
- The PANDA Micro Vertex Detector
- Silicon pixel detectors
  - Epitaxial layer based silicon pixel detectors
  - Sensor irradiation measurements
- The ToPiX readout ASIC architecture
  - ToPiX prototype : architecture and measurement
  - Total dose and single event effect measurement
- Conclusions

PANDA experiment

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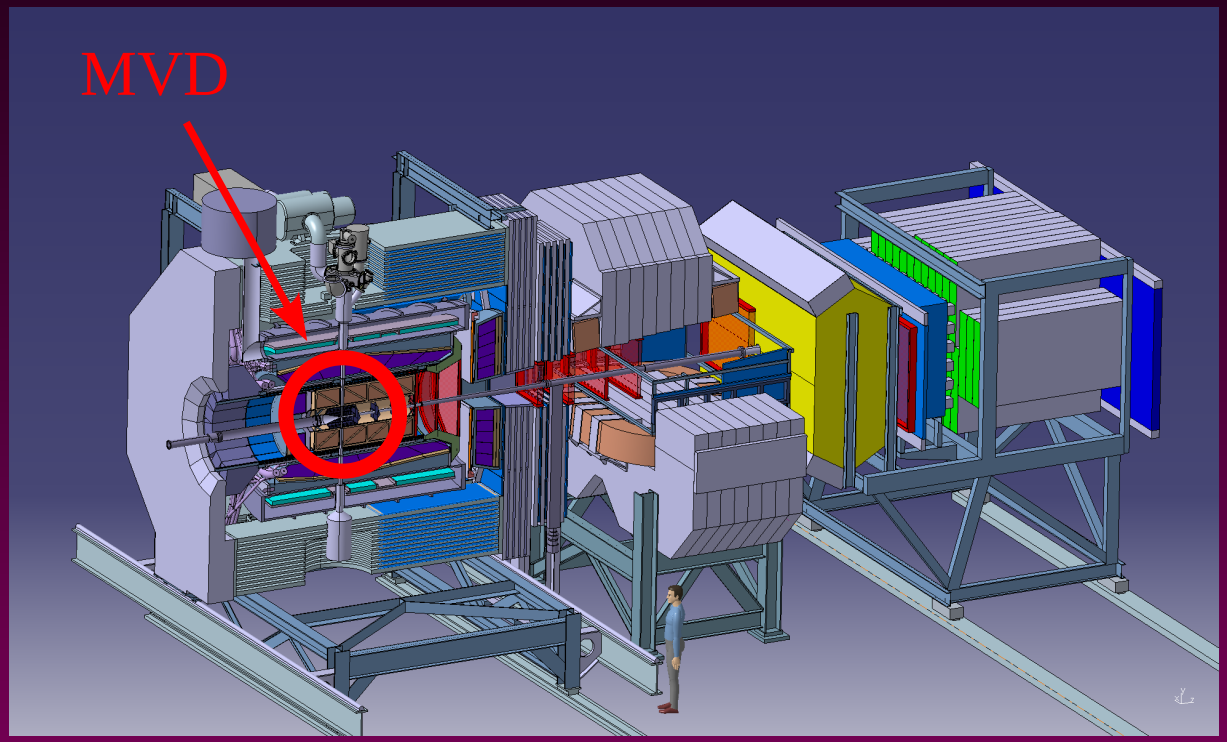
- Located at the new FAIR facility in Darmstadt
- Fixed target experiment at the High Energy Storage Ring for antiprotons at FAIR
- No trigger



→ The silicon Micro Vertex Detector is the closest detector to the interaction point

MVD layout

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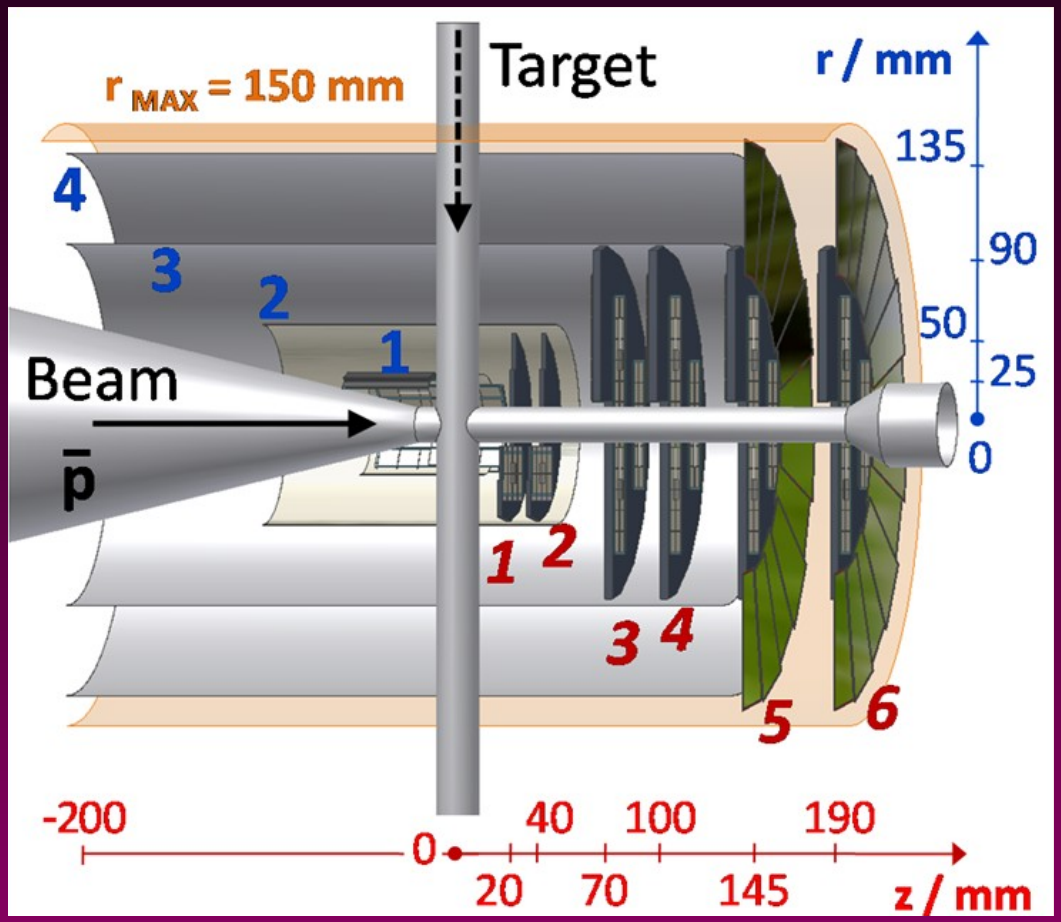
MVD layout :

- 4 barrels + 6 disk
- Inner layers (2) : SPD
- Outer layers (2) : SSD
- Forward : 4 SPD disks + 2 mixed disks
- SPD : ~11.5 Mpixels, 0.115 m^2
- SSD : 70 kstrips, 0.5 m^2



SPD requirements

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Pixel size	100 μm × 100 μm
Time resolution	< 6 ns (r.m.s.)
dE/dx measurement	yes (via ToT)
Dynamic range	0.032 fC ÷ 100 fC (12 bits)
Event rate	12.3 MHz/cm^2 (max)
Power consumption	< 500 mW/cm^2
Total ionizing dose	100 kGy
Total fluence	$5 \cdot 10^{14}$ 1MeV n_{EQ}/cm^2

Mechanical layout

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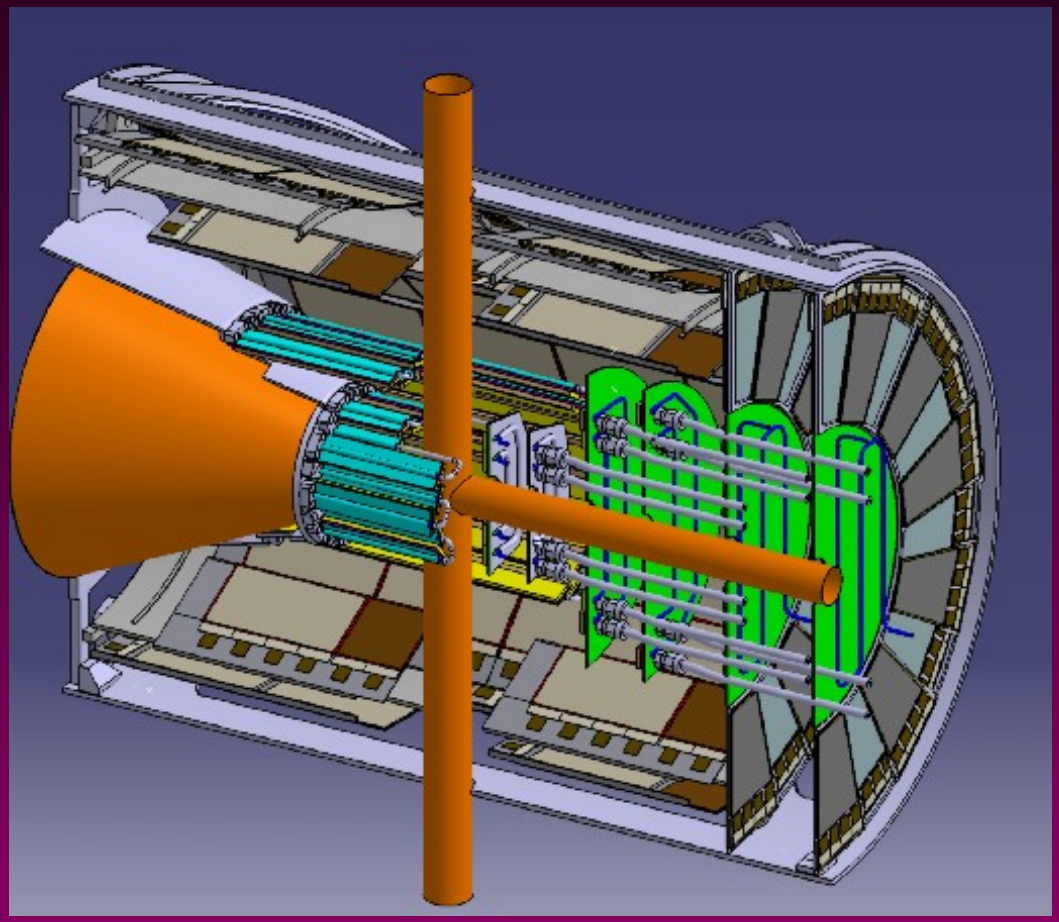

Layer 1 (66 ASICs) :

- 8 short staves (30 mm)
- 10 long staves (60 mm)

Layer 2 (384 ASICs) :

- 8 short staves (80 mm)
- 28 long staves (150 mm)

Disks 1-2 (40 ASICs) :

- Inner/outer diameter : 22/75 mm

Disks 3-6 (432 ASICs) :

- Inner/outer diameter : 22/150 mm

Module concept

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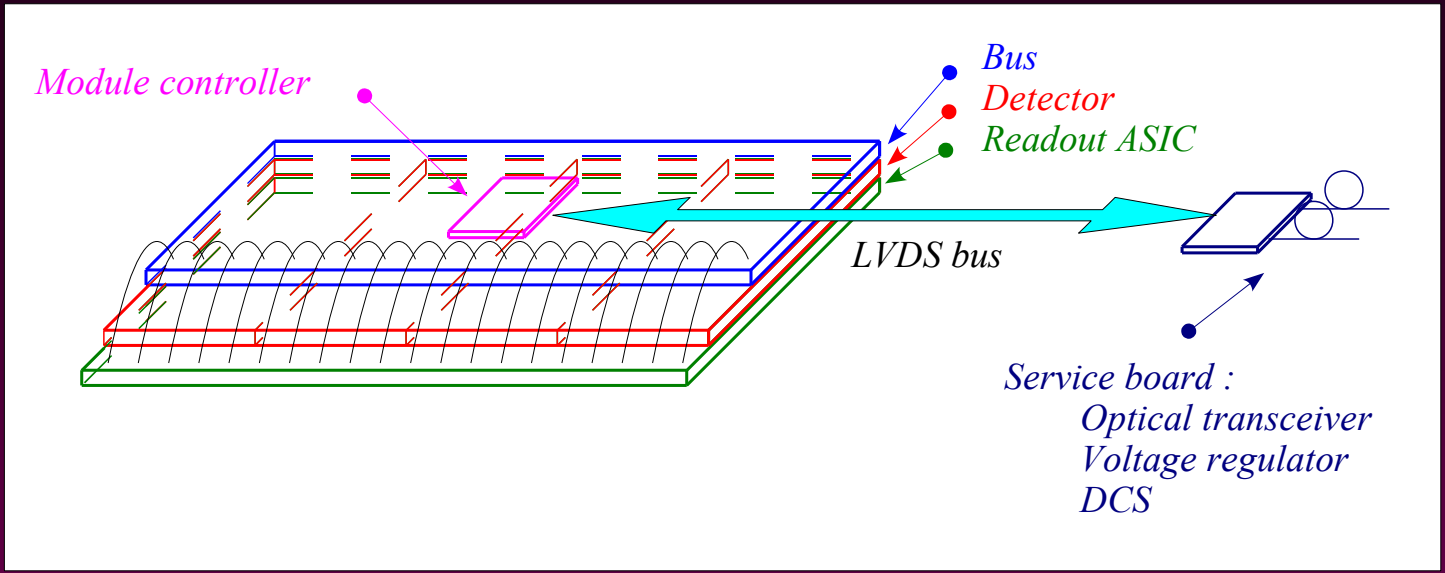

- Module : detector, readout ASICs, controllers and service board
- Module size : 2, 4, 5 and 6 chips/module
- Very limited space for cabling → electrical to optical conversion close to the detector
- Low voltage electronics → voltage regulator

Module layout

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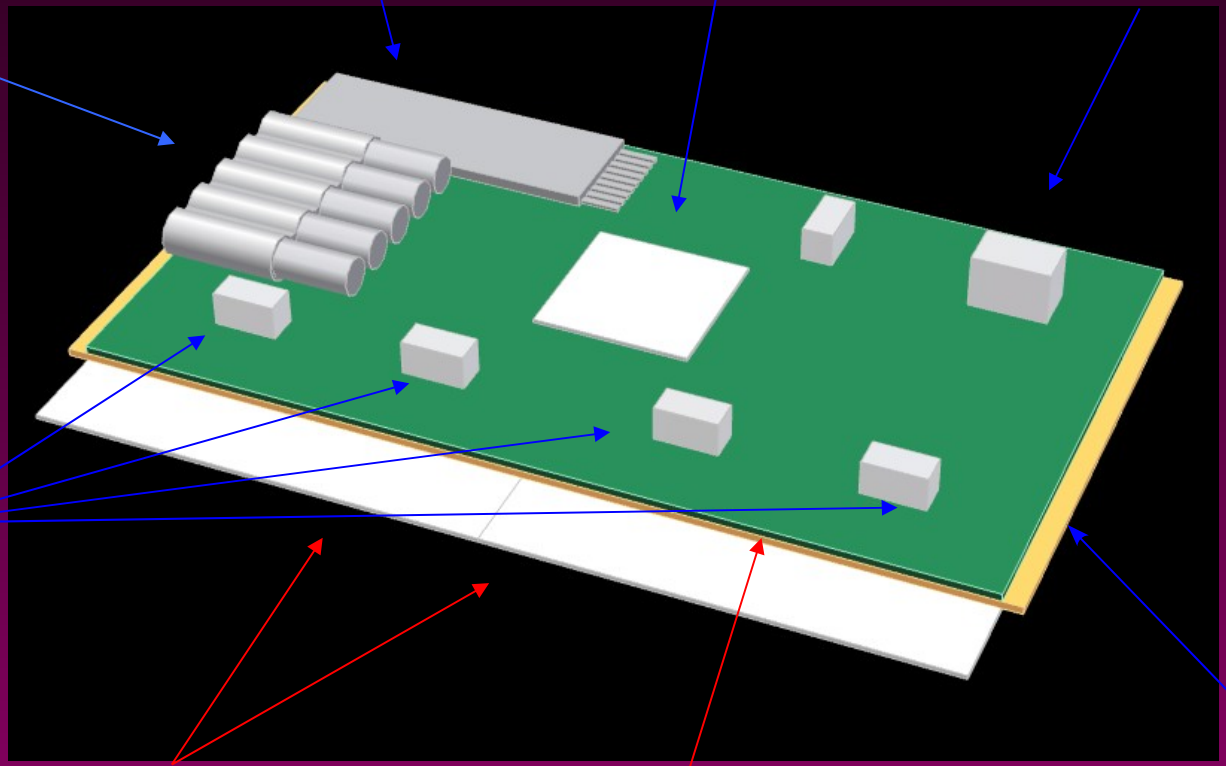
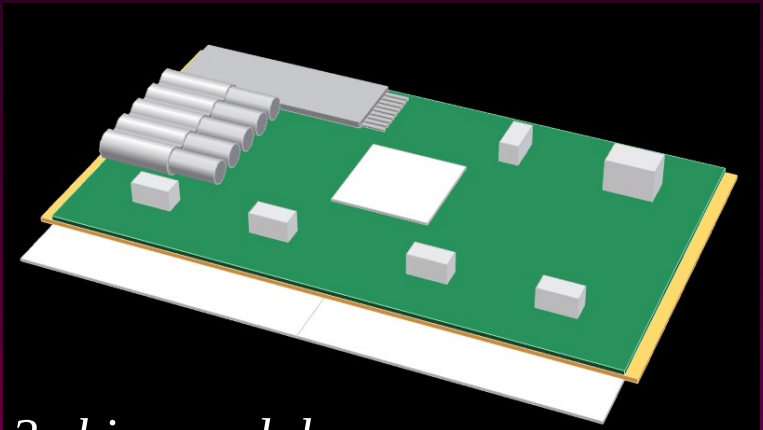
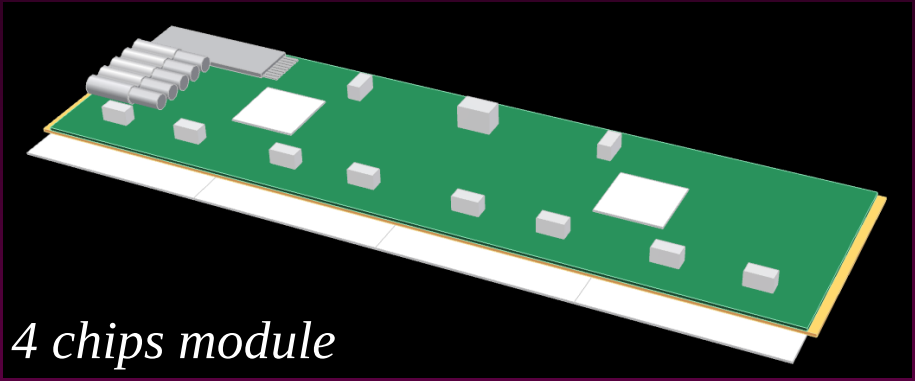


Module types

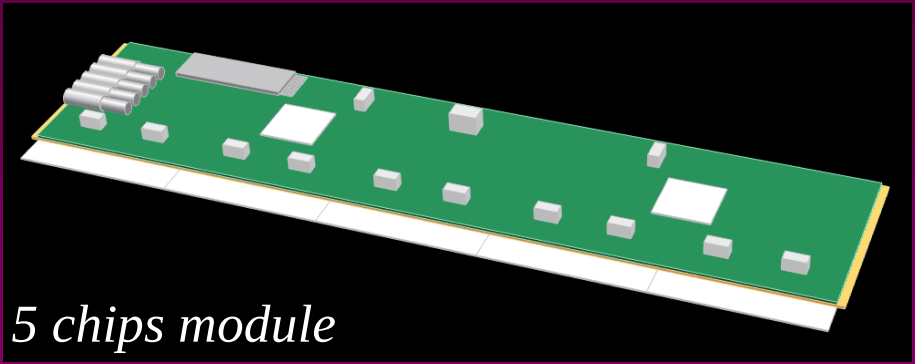
Sezione di Torino



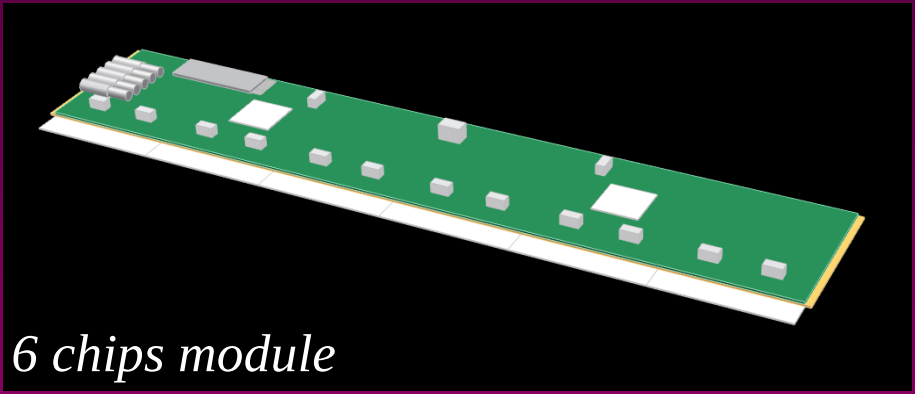
2 chips module



4 chips module



5 chips module



6 chips module

Disk layout

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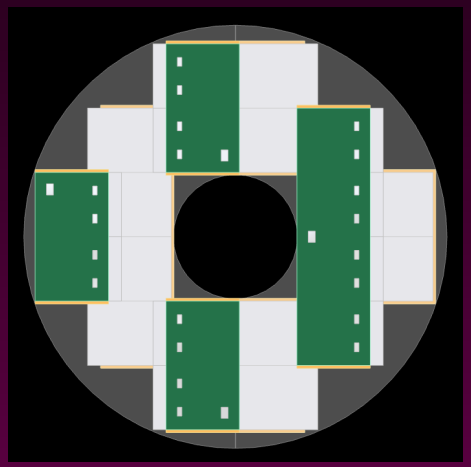

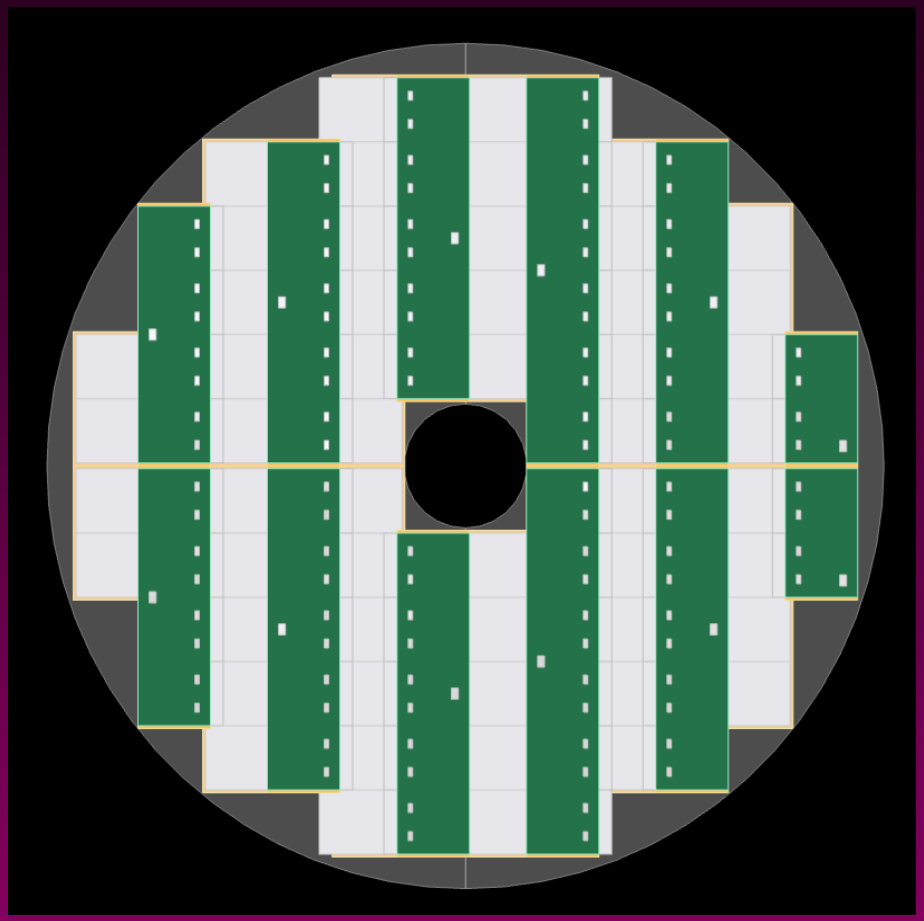

- Disk driven module layout
- Disks 1-2 : 75 mm diameter, 6+2 modules
- Disks 3-6 : 150 mm diameter, 4+4+12+4 modules

Epitaxial detector

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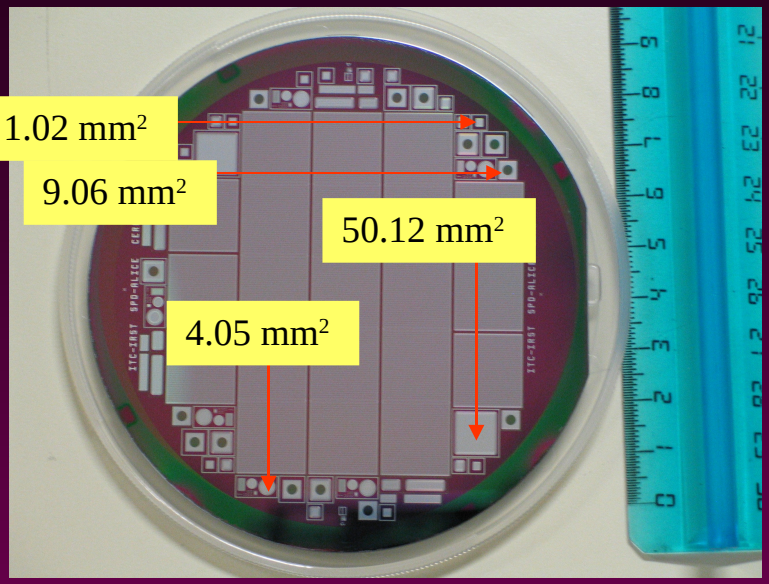


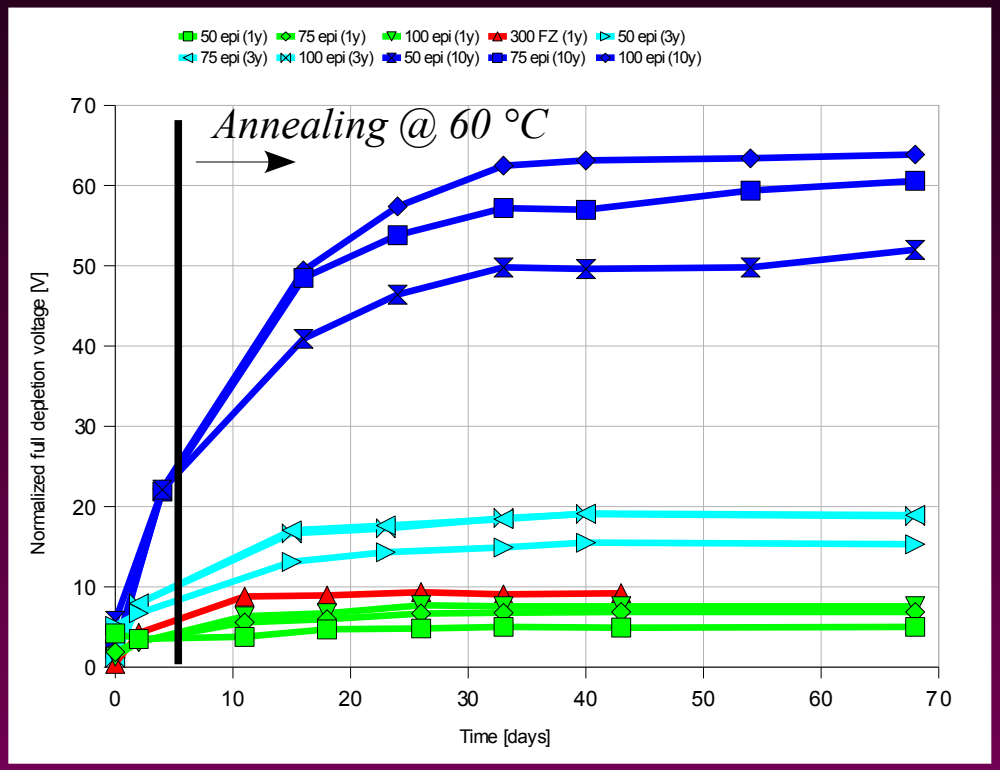
- Pixel detector with the ALICE masks (pixel size 50 μm × 425 μm)
- Test performed using the ALICE readout chip and test system (ack. to P. Riedler)

→ *D. Calvo et al., Thinned epitaxial silicon hybrid pixel sensors for the PANDA experiment, NIM-A594 (208) 29-32*

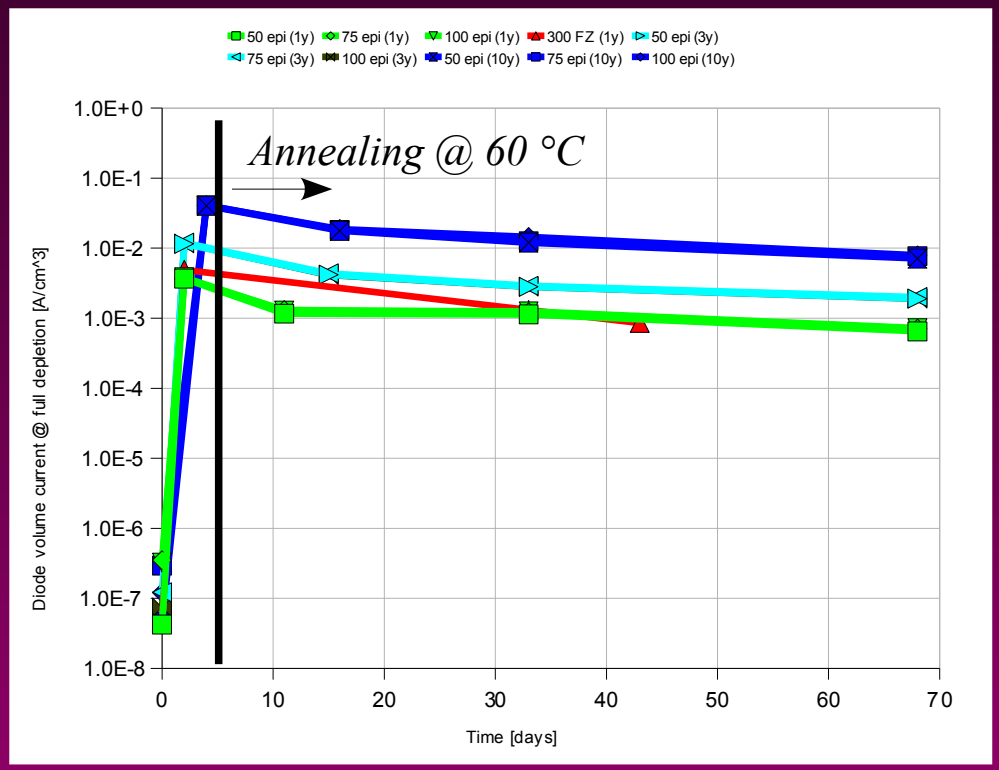
- 49 μm (4060 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 100 μm
- 74 μm (4570 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 120 μm
- 98 μm (4900 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 150 μm

Measurements

Sezione di Torino



Equivalent fluence values on the diodes : 5.13×10^{13}, 1.54×10^{14}, 5.13×10^{15} n_{EQ}/cm^2 corresponding to 1,3 and 10 years of PANDA



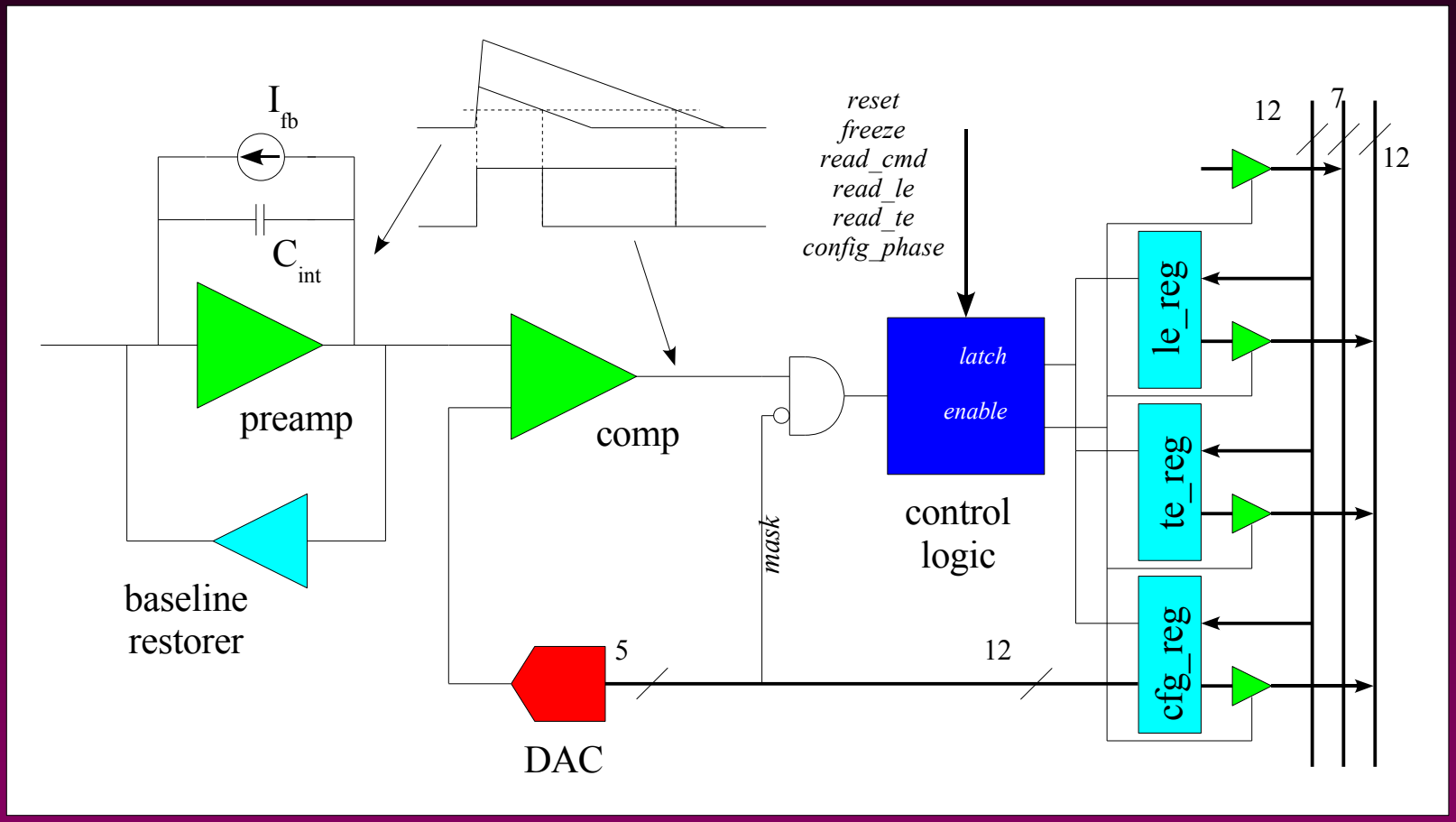
Leakage current < 50 nA for a 100 μm ×100 μm, 100 μm thick pixel

ToPiX

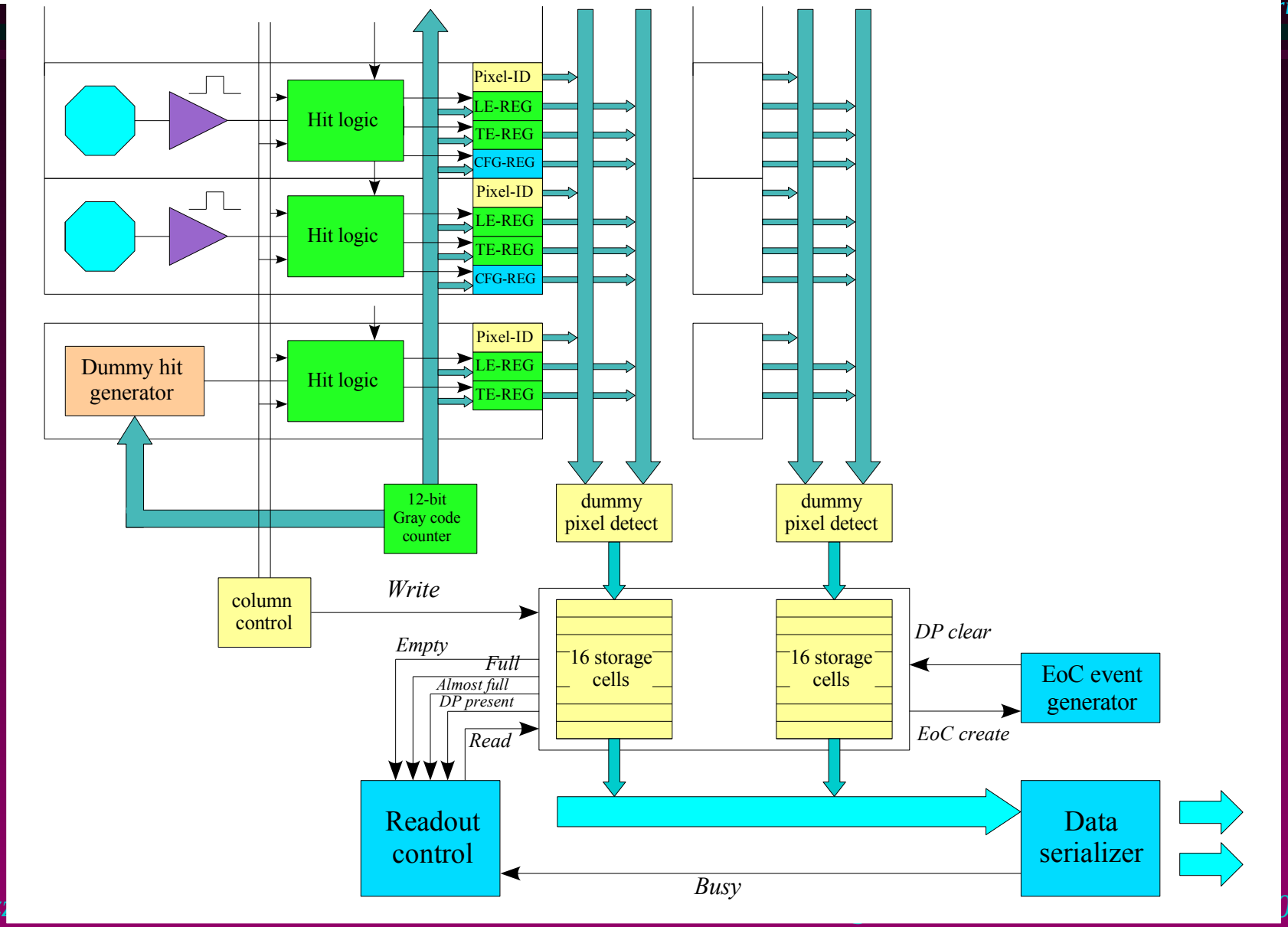
Sezione di Torino

- Custom readout ASIC for the PANDA MVD
- Provides spatial and time coordinates plus energy resolution measurement (via ToT) : 7 bits linearity, 12 bits dynamic range
- Compatible either with p-type or n-type detectors
- Self triggered architecture
- Active area size : 11.4 mm × 11.6 mm
- Chip estimated size : 11.2 mm × 14.8 mm
- Clock frequency : 50 MHz
- Event rate per chip : 5.56 kHz (avg), 16.3 MHz (max)
- Data rate per chip : 278 Mb/s (avg), 815 Mb/s (max)

Pixel cell


I fb
C int
preamp
baseline restorer
comp
DAC
5
mask
reset
freeze
read_cmd
read_le
read_te
config_phase
latch
enable
control logic
12
le_reg
te_reg
cfg_reg
12
7
12

ToPiX schematic



ToPiX prototype

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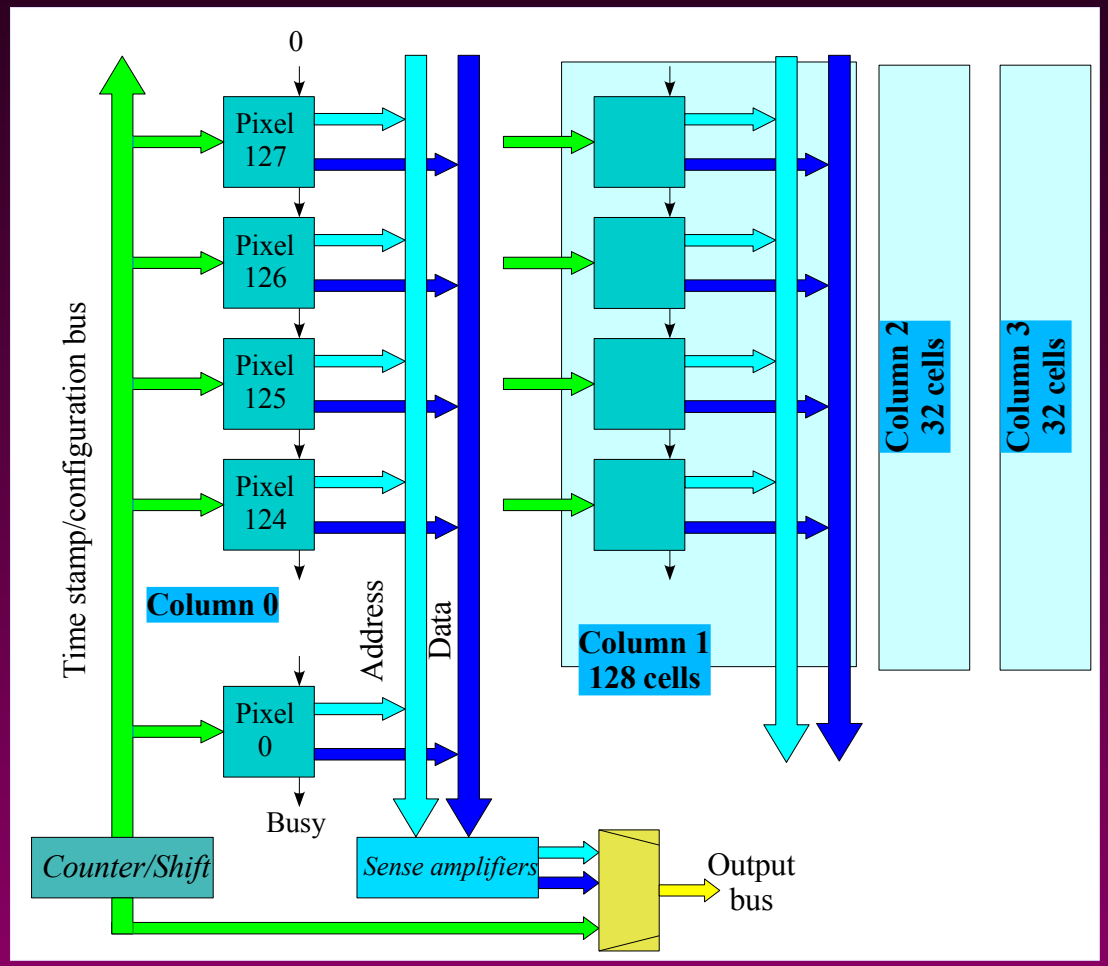

- Full pixel cell (analogue + digital)
- Two folded columns with 128 cells
- Two columns with 32 cells
- 5x2 mm^2 die area
- CMOS 0.13 µm technology
- SEU tolerant logic (based on the DICE cell)

Prototype layout

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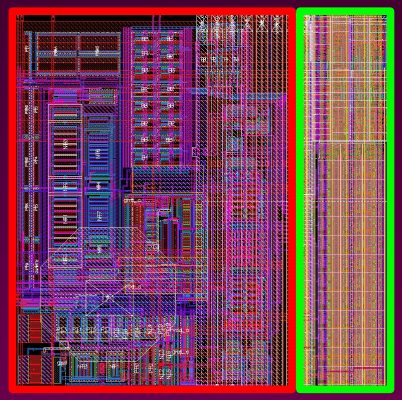
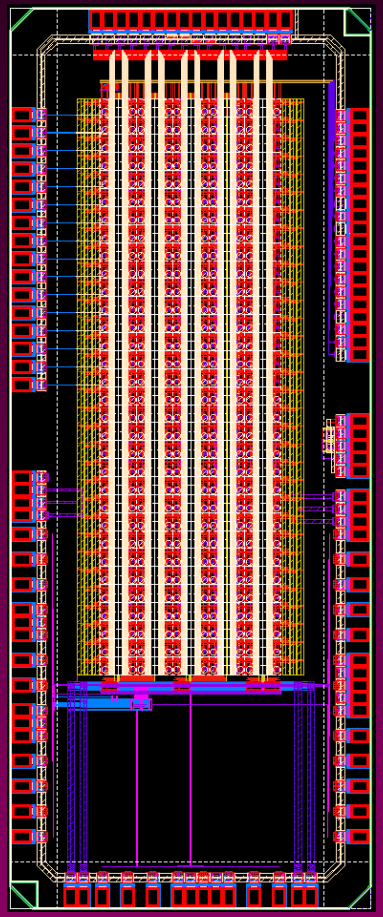
Pixel cell

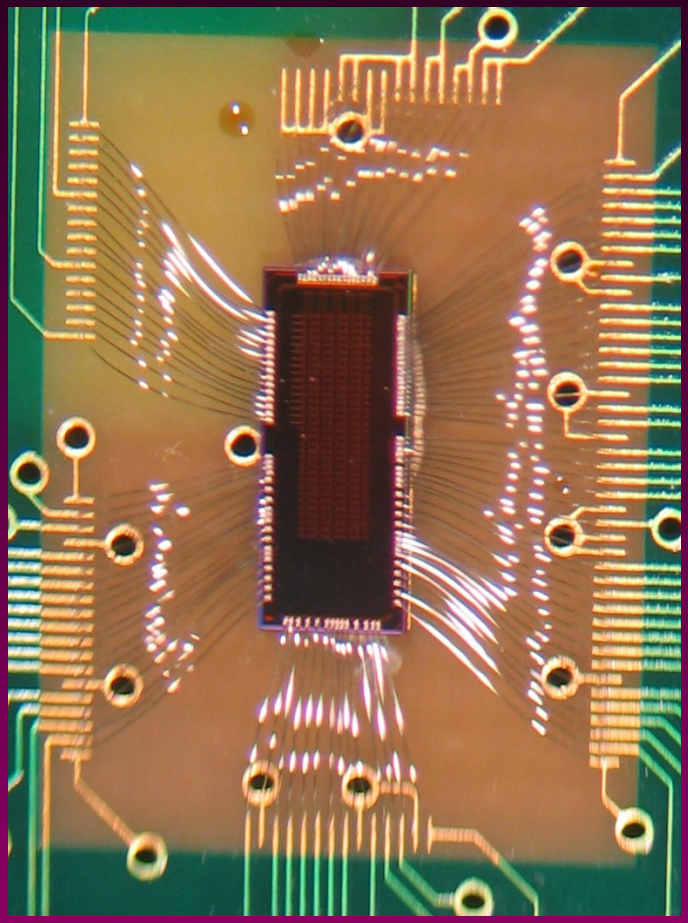
100 μm × 100 μm



Analog *Digital*

ToPiX prototype 5 mm × 2 mm





Test results

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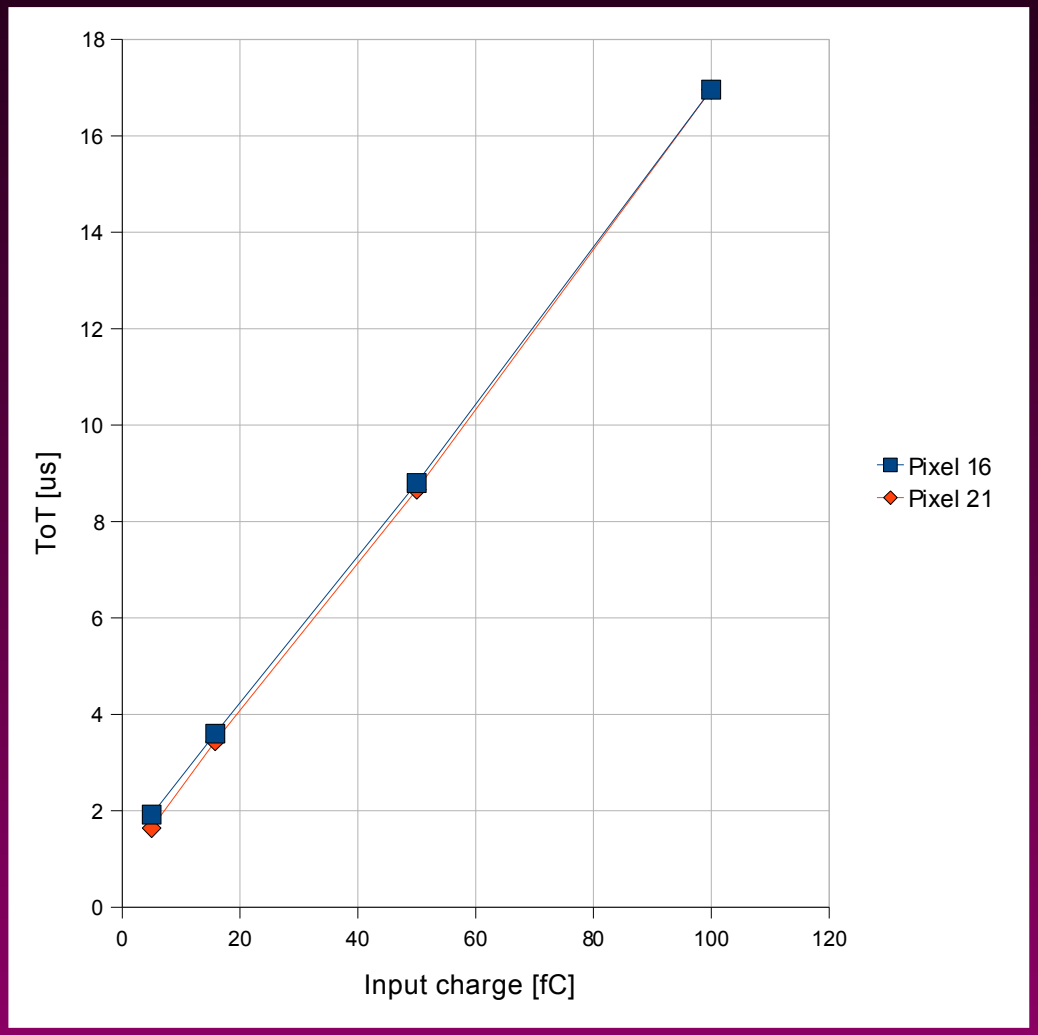
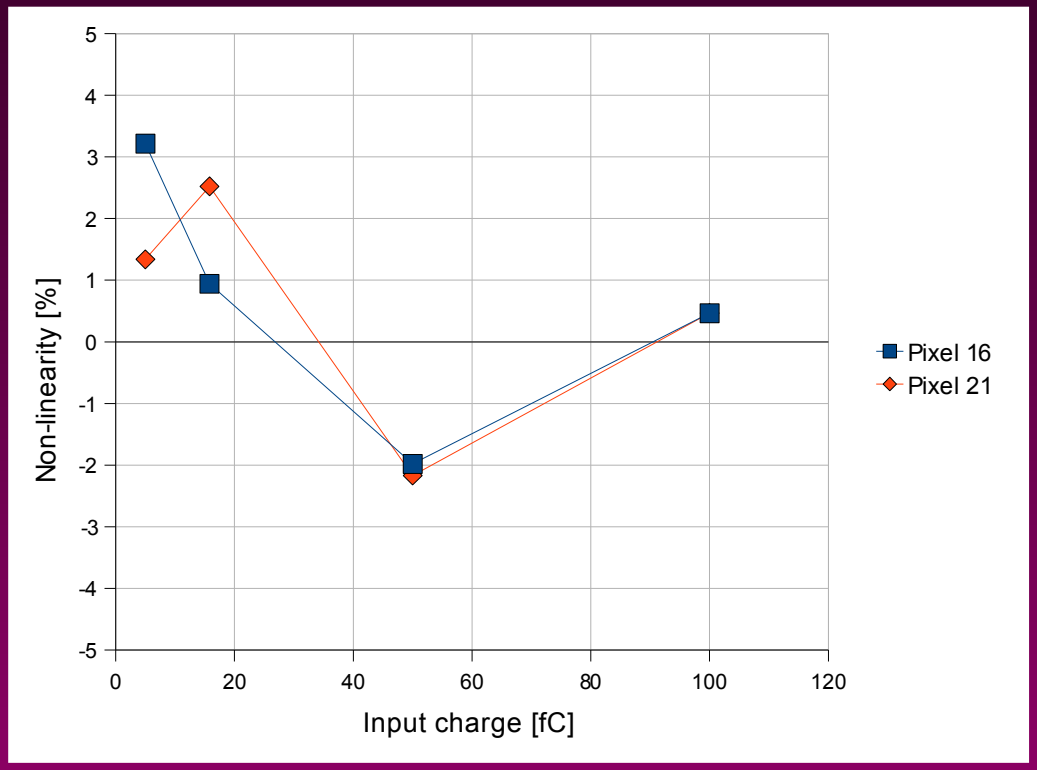
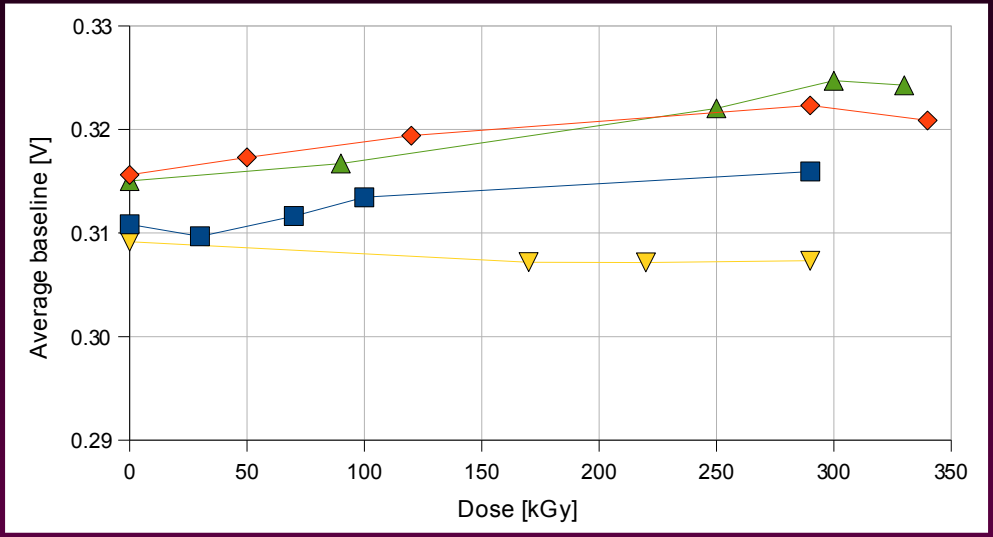


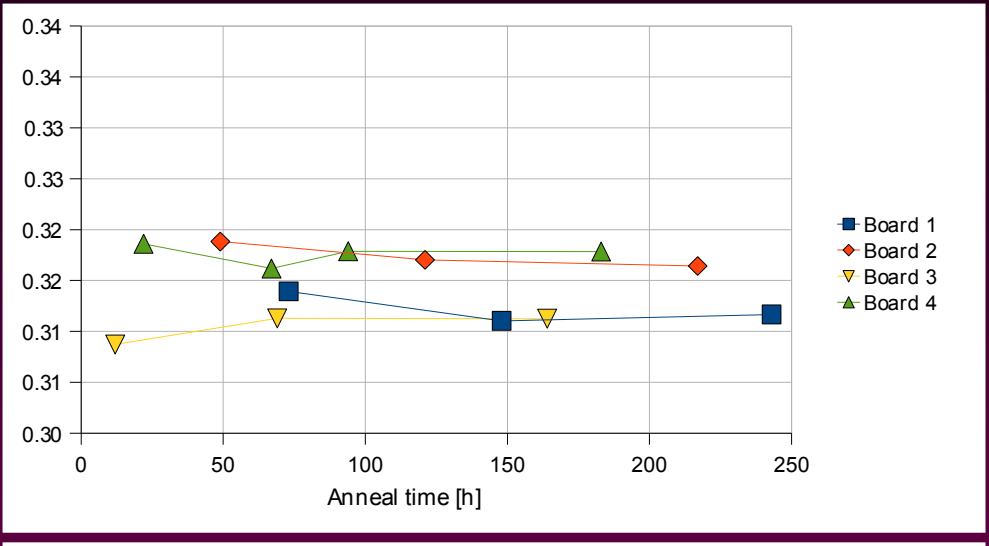
Average gain = 152 ns/fC
σ = 6 ns/fC

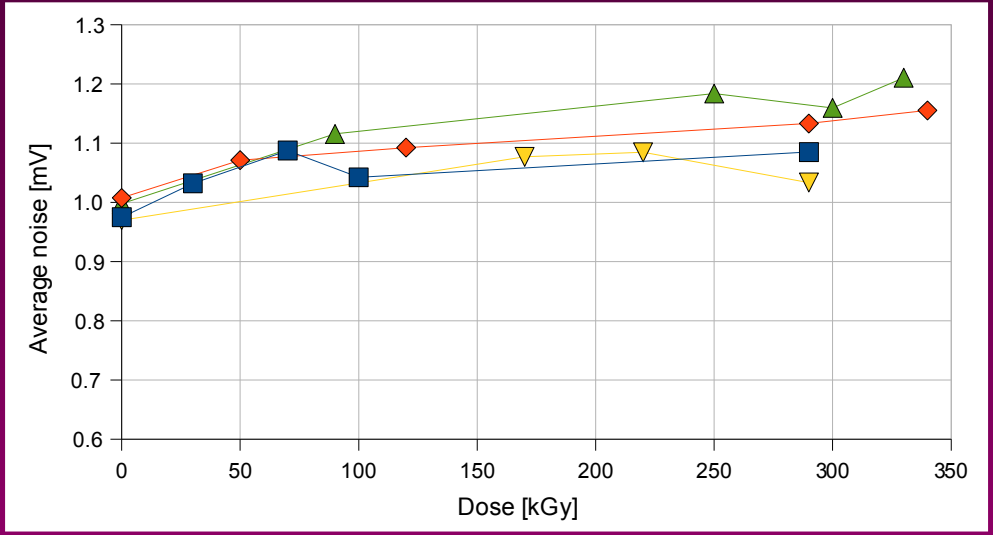


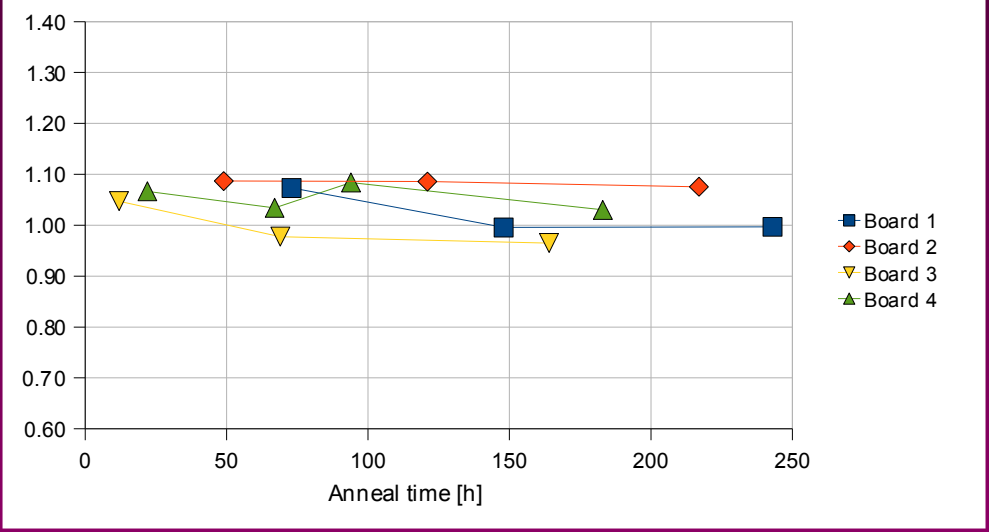
Irradiation tests - 1

Sezione di Torino



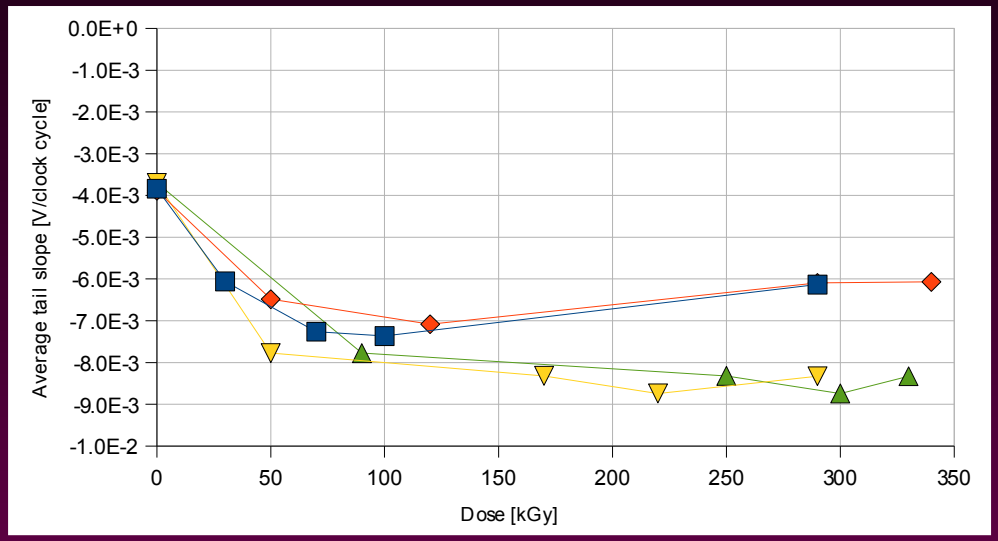


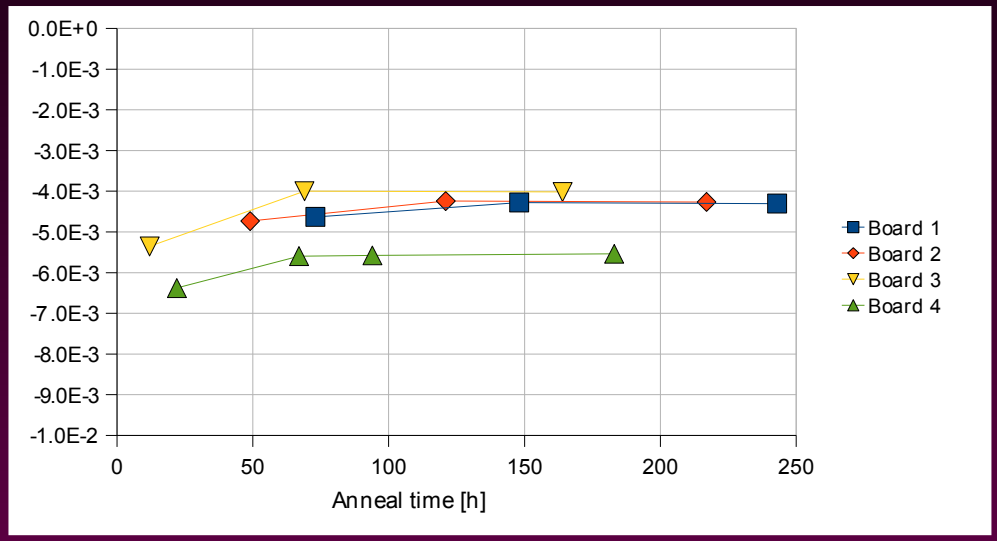


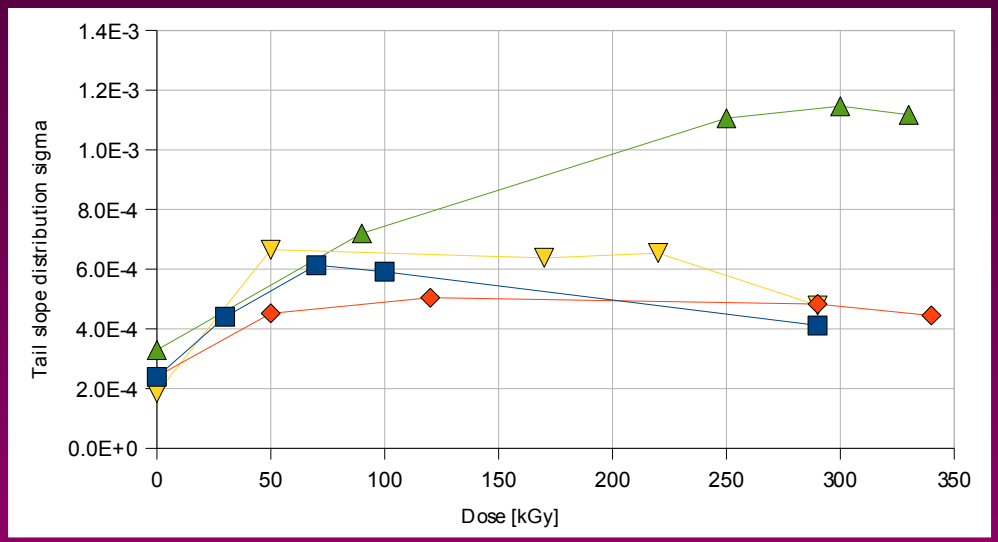


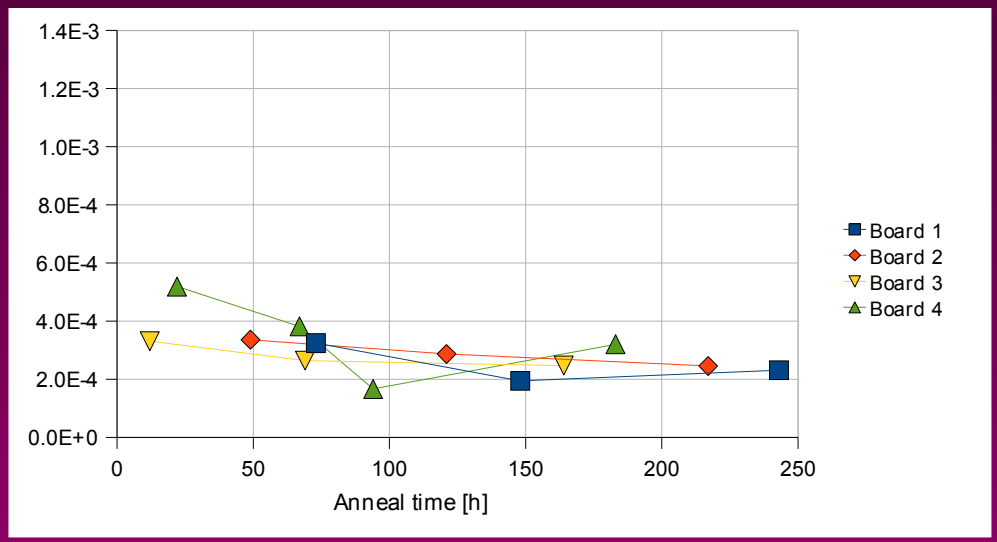
Irradiation tests - 2

Sezione di Torino









SEU effects

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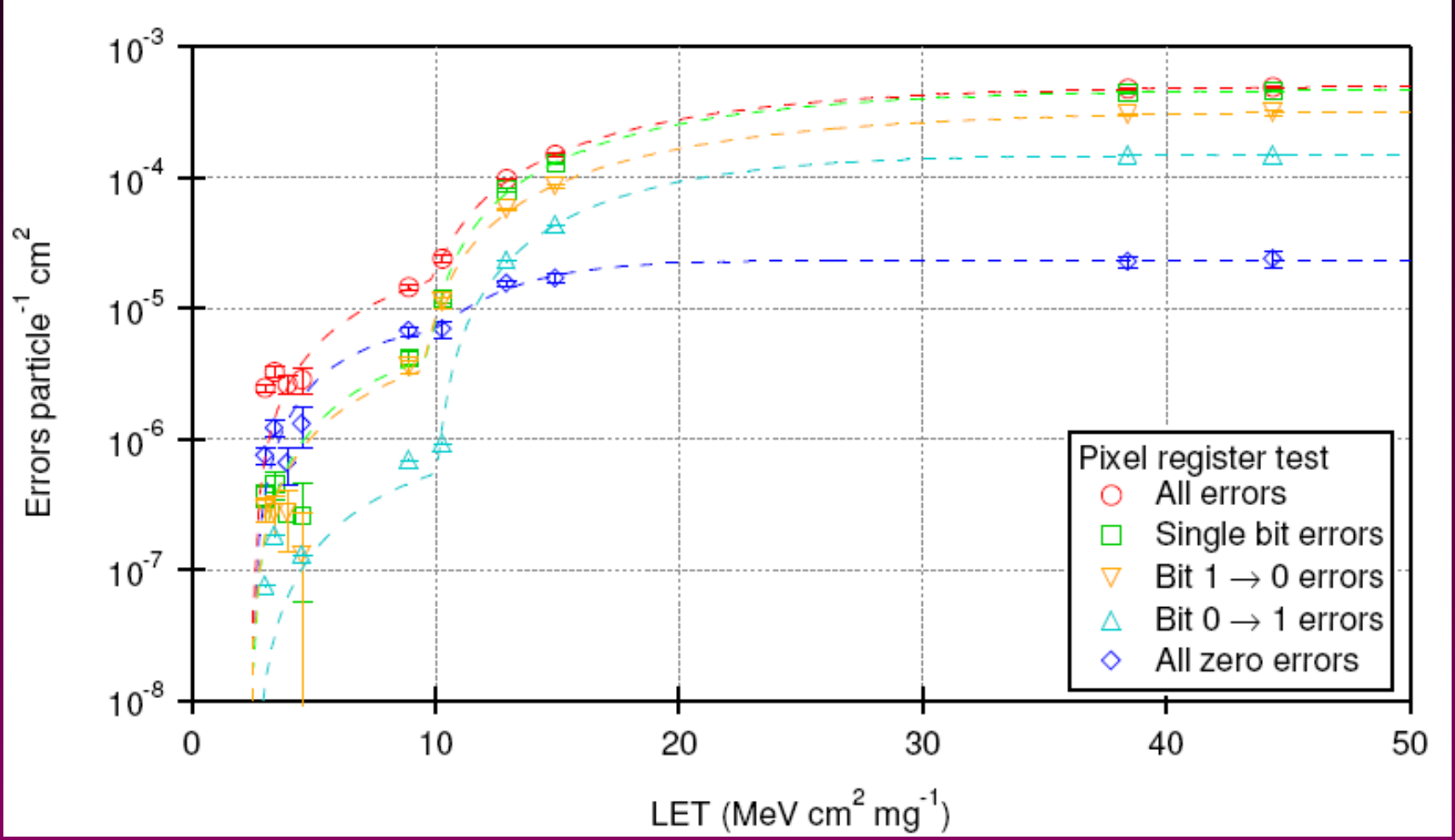

Conclusions

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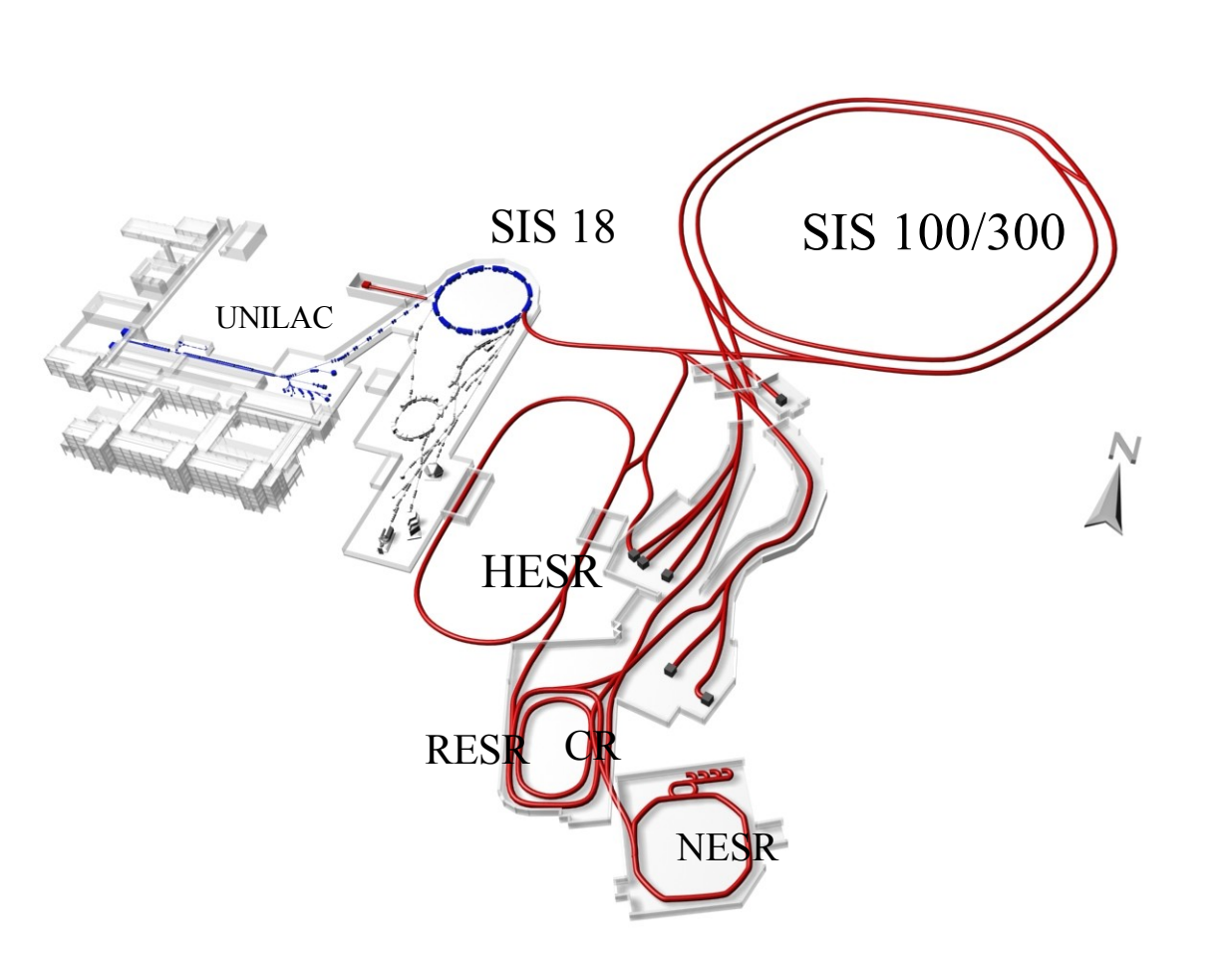
- The design of Micro Vertex Detector for the PANDA experiment poses significant design challenges.
- The silicon pixels are the closest detector to the interaction point, thus receiving the highest particle density.
- Due to the absence of a trigger signal, each event has to be tagged with a time reference, thus increasing the amount of data.
- A hybrid pixel sensor based on epitaxial material is under development. Epitaxial silicon shows better tolerance to radiation environment.
- A custom readout ASIC, named ToPiX, is under design in a CMOS 0.13 μm technology. A reduced scale prototype has been designed and tested. The overall performances and radiation tolerance are satisfying.

Spare slides

FAIR



Antiproton production

- → Proton **LINAC** 50 MeV
- → Accelerate p in SIS18/100
- → Produce $\bar{p}$ on target
- → Collect in **CR**, cool in **RESR**

HESR : storage ring for $\bar{p}$

- → Injection on $\bar{p}$ at 3.7 GeV
- → Slow synchrotron (1.5-15 GeV)
- → Luminosity up to ~2×10^{32} cm^{-2} s^{-1}
- → Beam cooling (stochastic and electron)

PANDA at FAIR

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Routing

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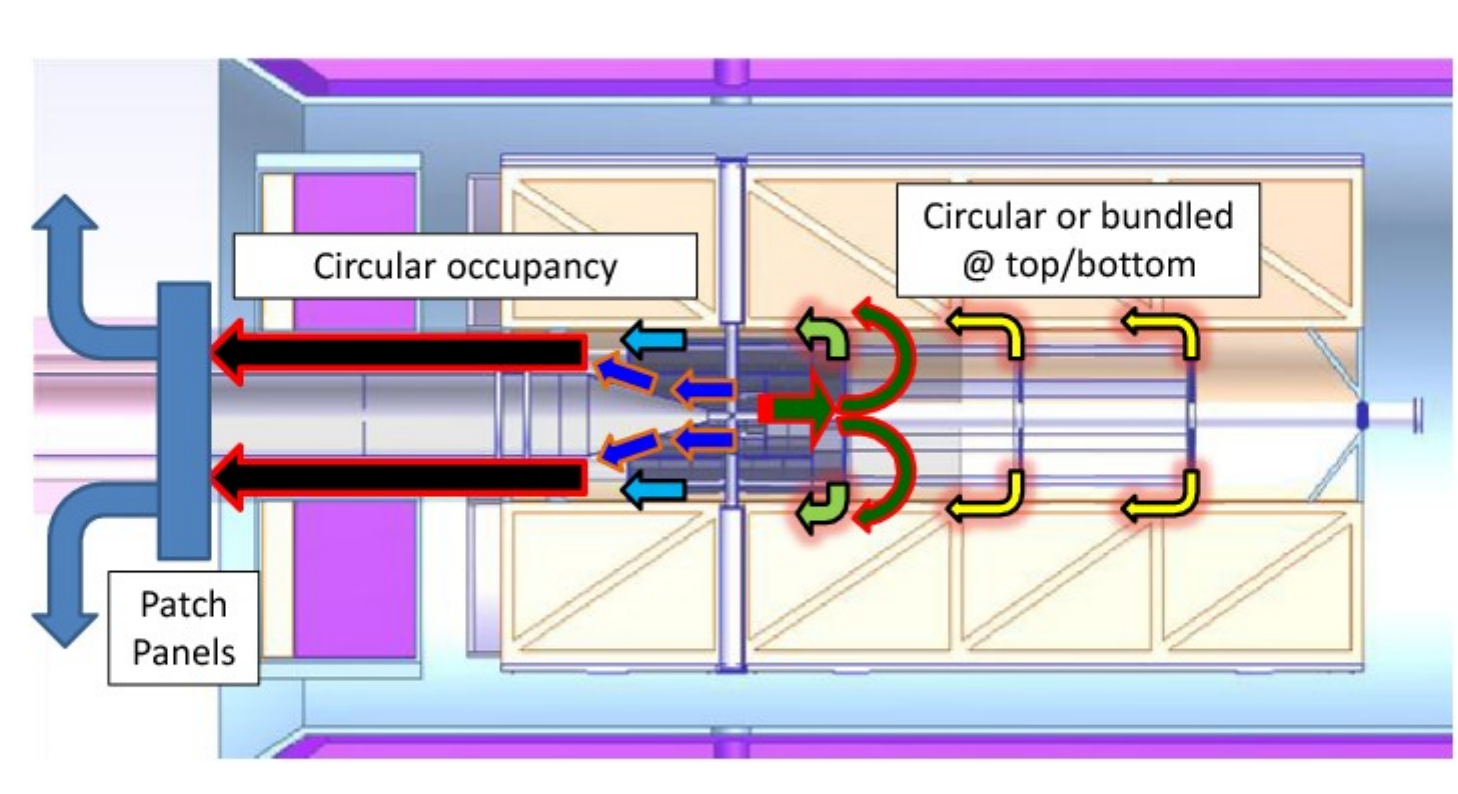
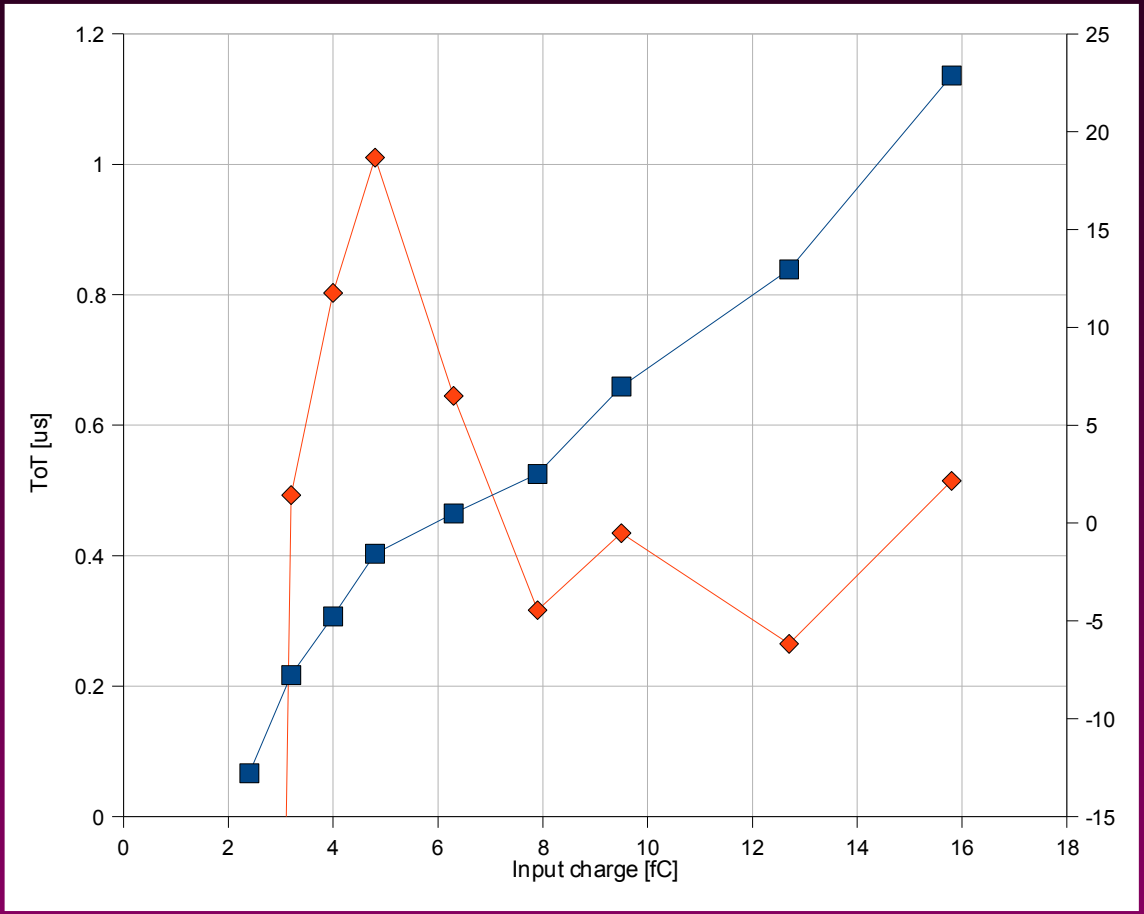
Access possible on the upstream direction
→ possible criticity in cables and service routing



Low range

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