A Time-Based Front-End ASIC for the Silicon Micro Strip Sensors of the P̄ANDA Micro Vertex Detector

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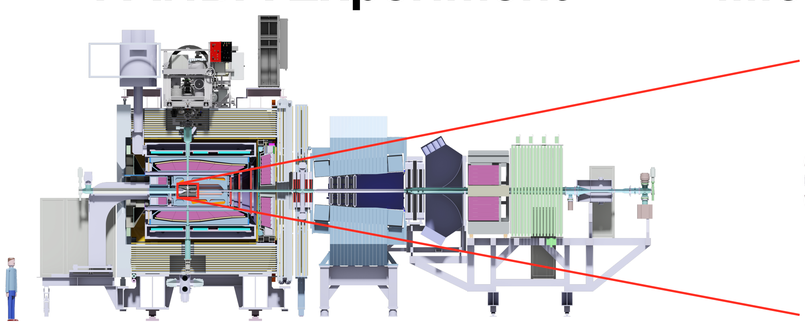
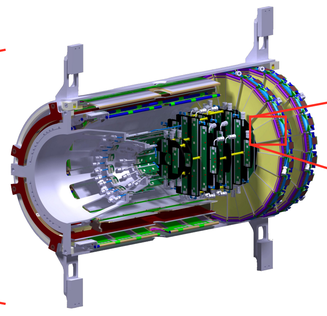
P̄ANDA Experiment



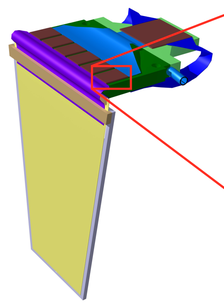
Antiproton **An**nihilation at **Da**rmstadt

Micro Vertex Detector

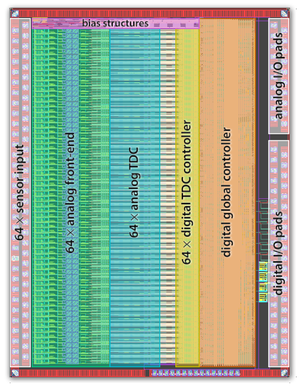


Hybrid pixel and double-sided strip sensors

Sensor Module



Example of a trapezoidal strip sensor



Readout ASIC

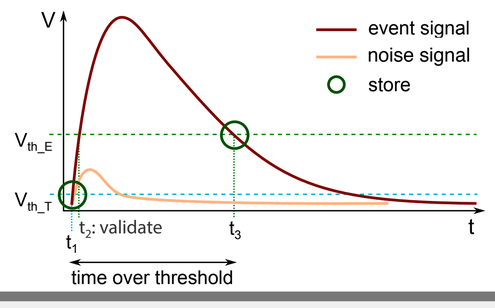
P̄ANDA Strip ASIC (PASTA)

• Channels (input pitch)	64 (63 µm)
• Technology	CMOS 110 nm
• Rate capability	100 kHz/ch
• Power consumption	< 4 mW/ch
• Front-end noise	< 600 e^-
• Time bin width	50-400 ps
• Charge resolution	8 bit (dyn. range)*
• Radiation dose	100 kGy*

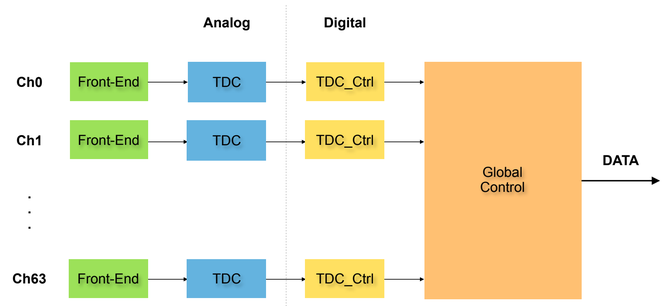
* Design Goal

Measurement Concept

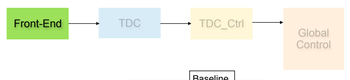
Inspired by TOFPET

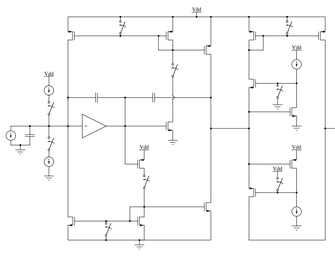


ASIC Architecture

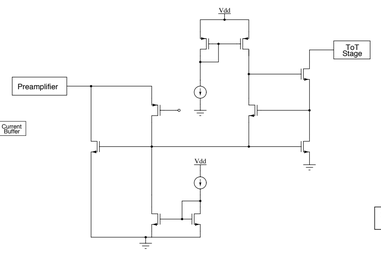


Front-End Architecture

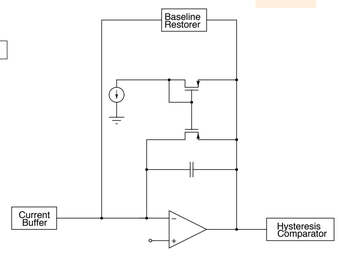




Preamplifier
First amplification stage capable of processing signals of both polarities (n-type or p-type strips)

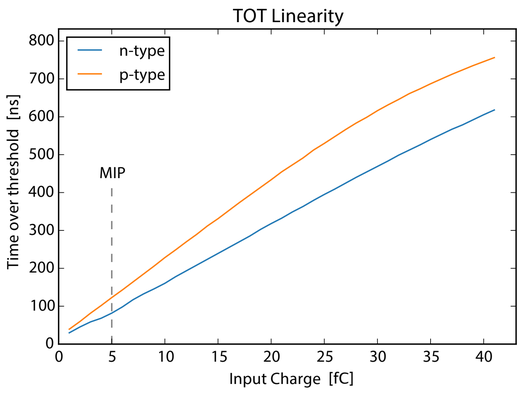


Current Buffer
Stage providing both current gain and impedance adjustment

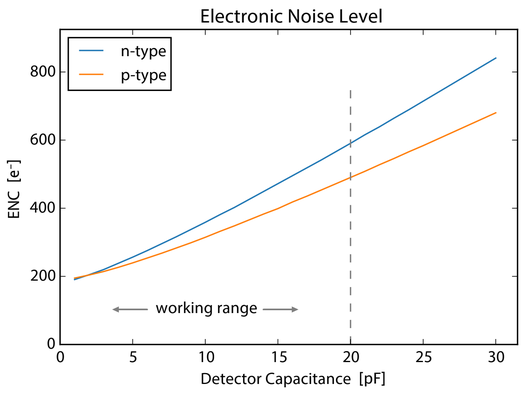


ToT Amplifier
Second amplification stage for the linear discharge of the feedback capacitance

Simulations

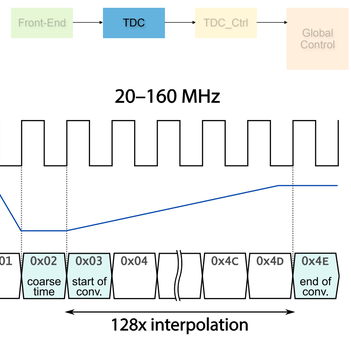


Input capacitance C_{det} = 20 pF



Input charge Q_{in} = 4 fC

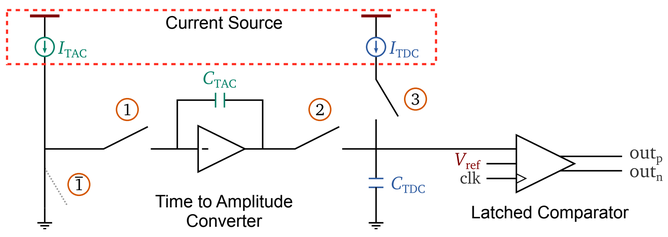
Time to Digital Converter



Motivation

- High temporal precision
- Low power consumption
- Compact structure

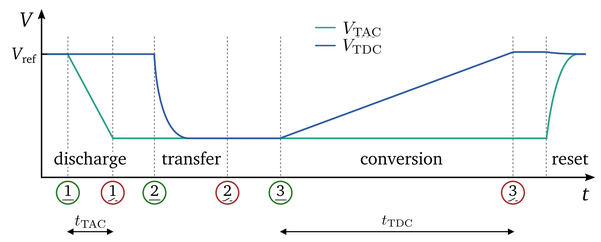
Architecture



Current Source
Block providing a fine tuning system for I_{TDC} in order to fix the ratio of the two currents and secure the desired resolution

Time Amplification

The time of conversion t_{TDC} can be calculated as follows:

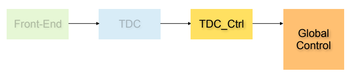


$$C_{\mathrm{TDC}} = 4 \cdot C_{\mathrm{TAC}}$$

$$I_{\mathrm{TDC}} = {}^{1}\!/_{32} \cdot I_{\mathrm{TAC}}$$

$$V_{\mathrm{TDC}} = V_{\mathrm{TAC}} \iff \frac{I_{\mathrm{TDC}} \cdot t_{\mathrm{TDC}}}{C_{\mathrm{TDC}}} = \frac{I_{\mathrm{TAC}} \cdot t_{\mathrm{TAC}}}{C_{\mathrm{TAC}}} \implies t_{\mathrm{TDC}} = 128 \cdot t_{\mathrm{TAC}}$$

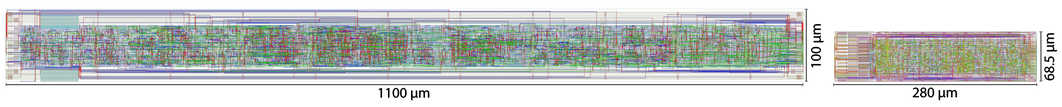
Digital Blocks



Optimization of the TDC Control

- Size reduced by ~80%
- Overall power consumption halved
- Radiation-hard logic implemented

} compared with TOFPET



Single Event Upset (SEU) Protection

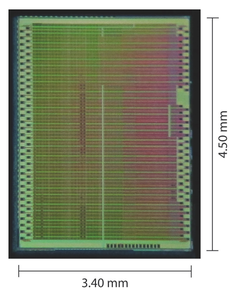
- 1 bit: Triple Modular Redundancy
- n bits: Hamming encoding

Conclusions

- Chip designed according to the given specifications
- Analog, digital, and mixed-mode simulations extensively studied
- Project submitted in April 2015
- Prototypes delivered in September 2015

Perspectives

- Readout system under development
- PCB design started
- Beam test planned for early 2016



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