



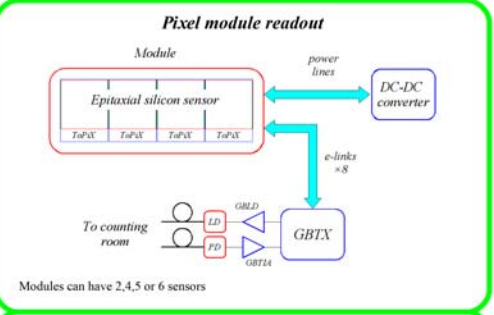
# Triggerless Readout Architecture for the Silicon Pixel Detector of the PANDA Experiment

**Abstract** : The readout architecture for the silicon pixel sensors of the PANDA MVD is presented. The pixel detector has to provide timing, position and energy information on an event-driven base, since no trigger signal is foreseen. The readout system is based on a custom ASIC, named ToPiX, directly connected to the GBT optical transceiver.

A reduced size prototype with most of the main functionality has been designed and tested. The ASIC has been bonded to a sensor based on the epitaxial technology and tested on a beam test. Both TID and SEU tests on the ToPiX prototype have been performed.

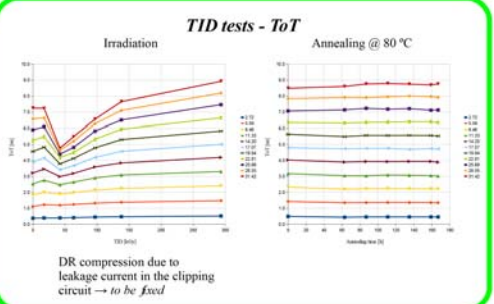
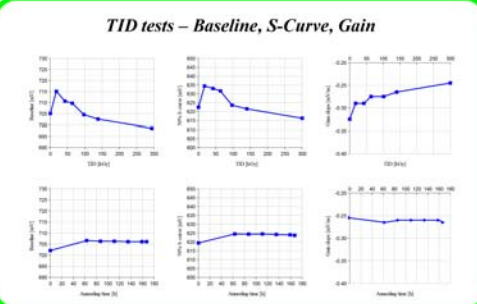
### PANDA Micro Vertex Detector layout

- Barrel
  - Layer 1 : radius 28 mm, SPDs
  - Layer 2 : radius 53 mm, SPDs
  - Layer 3 : radius 92 mm, SSDs
  - Layer 4 : radius 120 mm, SSDs
- Forward
  - Disks 1-2 : radius 37.5 mm, SPDs
  - Disks 3-4 : radius 75 mm, SPDs
  - Disks 5-6 : radius 130 mm, SPDs + SSDs



### ToPiX v3

- Die size : 4.5 × 4 mm<sup>2</sup>
- Technology : CMOS 0.13 μm
- Single 1.2 V power supply
- Bump bonding pads
- 2 × 2 × 128 cells columns
- 2 × 2 × 32 cells columns
- 32 cells EoC FIFO
- SEU protected logic via TMR (pixel cell) or Hamming encoding (EoC)
- Serial data output
- SLVS I/O



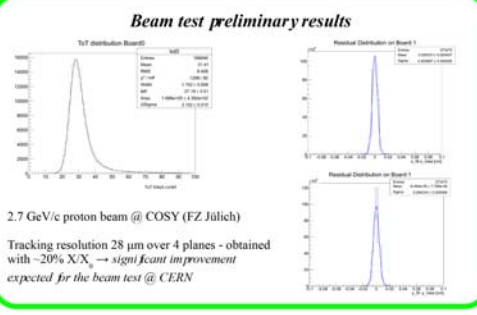
### Readout system for tests

Based on Xilinx Virtex-6 ML605 Evaluation Kit

Remote control via TCP/IP. Up to 4 boards controlled in parallel by a single PC.

Limited number of external interconnections → very flexible

Already used in a beam test at COSY (Jülich) and SPS (CERN)



### Beam test setup (pixel + strip)

4 pixel planes spaced by 60 mm  
640 pixel cells per chip (32×20 matrix)  
4 double layer silicon strip sensors (50 μm pitch, 19.2×19.2 mm<sup>2</sup> sensitive area)

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