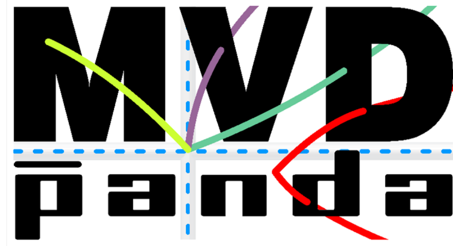
$\overline{\text{P}}$anda-MVD - note 008



Study of the Single Event Upset on ToPix_2

D. Calvo[1], P. De Remigis [1], G. Mazza [1], M. Mignone [1], R. Wheadon [1]
T. Kugathasan[1,2], L. Zotti [1,2]
A. Canderoli[3], S. Mattiazzo [3]

[1] INFN Torino
Via P. Giuria 1, 10125, Turin, Italy
[2] Torino University
Email: zotti@to.infn.it
[3] INFN Padova & Padova University

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Abstract

The second prototype of pixel readout electronics (Topix_2) has been studied for the estimation of the Single Event Upset (SEU). The prototype includes 320 readout cells, designed with a first basic level of Double Inter-locked storage CEll (DICE) architecture, meanwhile the end of the column logic has been designed with a standard architecture, this difference allows a comparison between a radiation tolerant architecture and the standard one. The goal of this work was the estimation of the SEU rate in the $\overline{\mathsf{P}}$ANDA environment. To this aim the SEU cross section of the devices has been measured at the SIRAD irradiation facility of INFN-LNL. Moreover the results of a dedicated study of the particles flux in the pixel part of the MVD have been used.

1 Introduction

The SEU is one of the possible single event effects (SEE) which occur in digital electronics due to the passage of particles or ions in the device. In particular the SEU is the change in state, i.e. a bit flip, that causes a glitch in the device output. It is not a permanent damage of the circuits functionality, and it is caused by a high energy deposition in a small volume. Following the literature [1], we can simply parametrize the SEU by two main parameters:

- the sensitive volume (SV), that is the volume in which the energy has to be deposited in order for the SEU to appear;
- the energy threshold (E_{dep}), that represents the minimum energy that must be deposited in the SV in order to cause an upset.

As described in [1], the SV to be considered for 130 nm CMOS electronics is 1 μm^3, that shows the better results in the comparison between experimental and simulation results. In particular it underestimates the SEU rate by a factor 30%, which we will take in account in our estimation.
The main effects of the SEUs are:

- the corruption of the data stored in the data memory;
- the variation of the detector configuration due to a bit flip of the configuration register.

In order to verify if the DICE architecture is sufficient in the $\overline{\text{P}}$ANDA environment, relative to a standard architecture, we tested our device with heavy ions, and we simulated the particle environment coming from the $\bar{\text{p}}$-p and $\bar{\text{p}}$-nuclei annihilations in $\overline{\text{P}}$ANDA.

2 SEU test

In order to estimate the SEU rate in the pixel part of MVD, it's necessary to know the SEU sensibility of the electronic circuit. To this aim a beam time was scheduled at the SIRAD (SIlicon RAdiation Damage) irradiation facility, located at the INFN National laboratory of Legnaro.

2.1 ToPix_2

ToPix_2 is the second reduced scale pixel readout prototype. It has been designed at the INFN Electronic Laboratory of Turin using the 130 nm CMOS technology [2], and a first basic level of DICE architecture [3]. It features an overall area of 5 x 2 mm^2, with 320 pixel cells of 100 x 100 μm^2, (arranged in two long columns with 128 cells, and two short columns with 32 cells). Topix_2, see Fig.1, has a dynamic range from 1 fC up to 100 fC, a triggerless read-out, an implementation for the time over threshold (ToT) technique, an analogue circuit (with preamplifier and comparator) and a digital circuit (with control logic and registers). Moreover the cell can be biased to work with signals coming from sensors of both polarities.

The Topix_2 architecture is based on three main functional blocks: the pixel

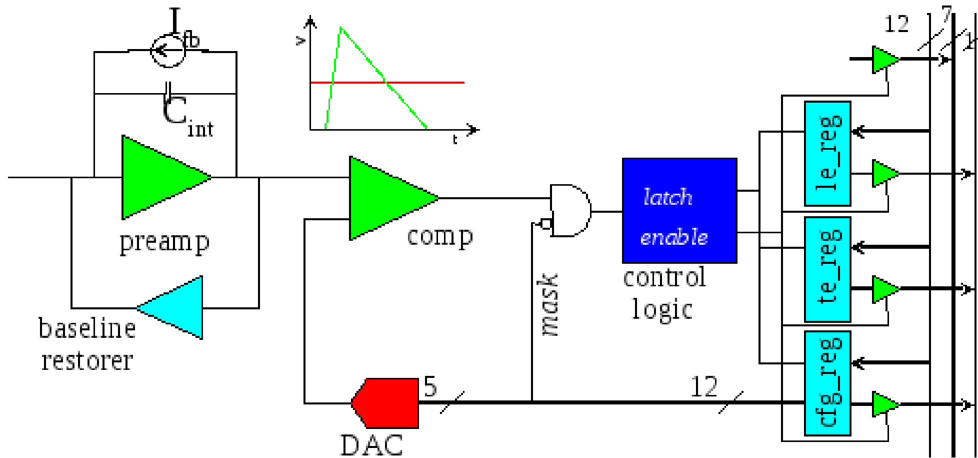

Figure 1: Analog and digital circuits of ToPix_2.

column, the end of the column logic and the data transmission circuit. A 12 bit time stamp bus, a 7 bit address bus and a 12 bit data bus are shared among all the pixels of the same column.
In each pixel readout cell there are 3 registers each 12 bit wide:

- the leading edge register stores the value of the time stamp bus when the comparator output switches from logic 0 to logic 1 (from 0 V to 1.2 V);
- the trailing edge register stores the value of the time stamp bus when the comparator output switches from logic 1 to logic 0 (from 1.2 V to 0 V);
- the configuration register contains the values for the cell working setup: 5 bits to set the comparator threshold, 1 bit to mask the chip, 2 bits to select the test mode and to address the pixel, and the remaining 4 bits to bias the circuits for choosing the sensor polarity and the leakage compensation.

The time stamp value in the leading register gives the time information, while the difference between the value in the falling and the leading register provides the width signal information that, due to a constant current discharge circuit, is proportional to the amplitude of the signal and thus to the particle energy loss. If an upset occurs in the configuration register, for example, the threshold value will change, and consequently all the information stored in the leading and falling edge register will be incorrect until a re-write operation of the configuration register will take place.
The cell readout has been designed with all the PMOS transistors in a common Nwell layout in order to be tolerant to SEU, for the moment no inter-guard rings have been provided.

2.2 Experimental setup and data analysis

In order to estimate the SEU rate in the $\overline{\text{P}}$ANDA environment, it's necessary to know the SEU sensibility of the electronic circuit. To this aim a long beam time has been organized at the SIRAD irradiation facility. The SIRAD irradiation facility is located at the INFN National Laboratory of Legnaro [4].

In general, the SEU study needs low ion fluxes (from 10^3 to 10^5 ions/(cm^2s)) [4]. The device irradiations are performed inside an irradiation chamber in which a residual pressure of 8 10^{-6} mbar is achieved. In the irradiation chamber there are two support structures, one fixed and the other movable perpendicular to the beam direction, see Fig.2. On the fixed structure there are 4 "fixed" diodes, arranged around a 2x2

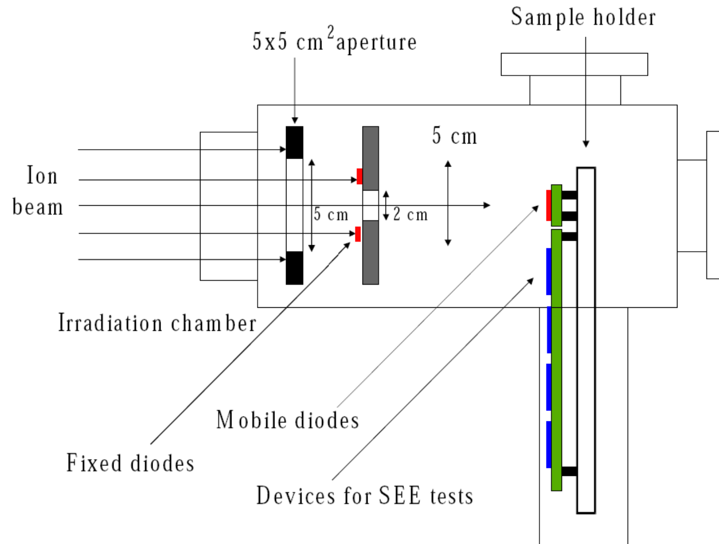

Figure 2: Side view of the experimental setup: the irradiation chamber with the dosimetry system and the sample holder is shown. [Figure not in scale]

cm^2 central aperture. On the mobile structure, a quartz, four mobile diodes and the device under test (DUT) are arranged as shown in Fig.3. These three components can be alternatively placed in the central aperture of the fixed structure, by moving the support by 0.5 mm steps using a motor controlled system. The quartz has been used to center the beam and to check its defocalization. The four "mobile" diodes, together with the fixed ones allow the measurement of the beam fluence, for dosimetry purpose. The knowledge of the sensitive diode area (0.5 x 0.5 cm^2) allows to calculate the ion fluence, which is defined as the number of ions per cm^{-2}.

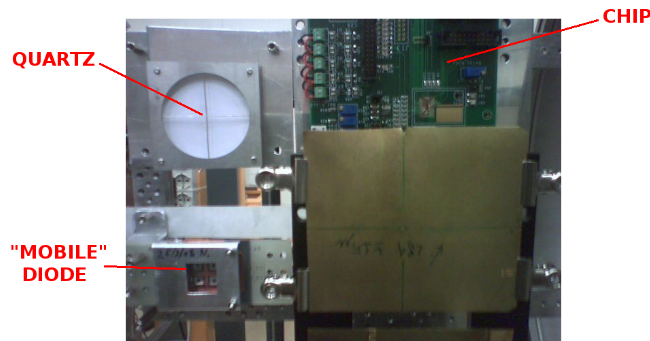

Figure 3: The sample holder inside the irradiation chamber.

The correct functionality of the setup and of the data acquisition system of ToPix_2 has been checked with a long beam time of 12 hours, with the DUT positioned 10 cm far from the beam spot, no SEU occurred.
More ions of different energies, see Tab. 1, have been used in order to have a wide range of deposited energy. Moreover it was possible to investigate the deposited energy due to different incident angles, rotating the mobile structure [5]. The irradiation runs lasted about 20 minutes and before and after each run dosimetry measurements were carried out. In these runs the "mobile" diodes were exposed to the beam, in order to calculate a correcting factor, equal to the ratio between the "mobile" diode fluence and the "fixed" diode fluence. In this way, during the DUT irradiation, we have quantified the fluence on the chip, multipling the "fixed" diode fluence with the correction factor.
The ToPix_2 DAQ chain is based on a NI-PCI system using the PCI-783IR board

Ion	Beam Angle	E_{cin} [MeV]	E_{dep} (in 1 μm^3) [MeV]
^{16}O	0°	101	0.70
^{16}O	30°	101	0.81
^{19}F	0°	111	0.91
^{19}F	30°	111	1.07
^{28}Si	30°	146	2.40
^{35}Cl	0°	159	3.01
^{58}Ni	0°	223	6.47
^{79}Br	0°	215	8.96

Table 1: Ions used in the beam test with the corresponding kinetic energy, incident beam angle and deposited energy in a SV of 1 μm^3.

and a LabView software, see Fig.4. The clock was set to 10 MHz during the test because of the long cable between the DUT and the PC. In order to test the ToPix_2 with a 50 MHz clock, a bidirectional FIFO has been implemented on the FPGA board using short connection cables.

The study of the configuration register was performed using a control program developed with the LabView software, that carried out the following tasks:

- step 1: it writes the configuration register with a 12b legal sequence composed of alternated 0 and 1;
- step 2: it waits for 2s;
- step 3: it checks the register value with respect to the original value, if it is changed then the error counter is increased and it goes to step1;
- step 4: it goes to step 2;

The probability to have an upset, usually called SEU cross section, is given by:

$$\sigma_{SEU} = \frac{N_{errors}}{\Phi \cdot N_{bit}} \tag{1}$$

where N_{errors} are the number of SEUs, Φ is the total incident particle fluence and N_{bit} is the number of bits. The σ_{SEU} has been calculated as the average of the cross

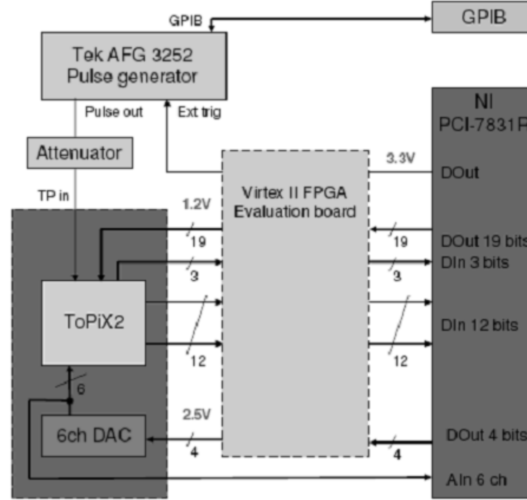

Figure 4: Data Acquisition system diagram for ToPix_2.

sections coming from the several irradiation runs with the same ion, and we used the standard deviation as an estimation of the error.
The experimental cross sections obtained are generally fitted by a Weibull function, see Fig.5, which represent the cross section as a function of the deposited ionization energy E_{dep}. It has the form:

$$\sigma = \sigma_0 \left[1 - e^{-\left(\frac{E_{dep}-E_0}{W}\right)^s} \right] \tag{2}$$

where W and s are shape parameters. In particular in our fit we use s=3 as fixed parameter. The saturation value σ_0 represents the maximum probability to have SEU, and E_0 is the threshold deposited energy.

Our fit parameters for the configuration register, see Fig. 5, are:

- E_{th}=0.4688 MeV
- σ_0 =1.99 10^{-8} [cm^2 bit^{-1}]
- W = 4.375 [MeV]

and as described before only ions, or particles, which deposit in the sensitive volume of 1 μm^3 an energy larger than the threshold energy can trigger an upset.
To evaluate the SEU rate of electronics developed in a standard layout without DICE architecture two components of the end column circuit of ToPix_2 were tested for irradiation.
The 12 bit shift register was tested using a software and a method similar to the previous one (for the configuration register).
The 12 bit counter was tested with a software comparing at fixed time intervals its value with the one of a "mirror" FPGA counter. This test was performed with a 10 MHz clock, although the nominal clock of ToPix_2 is 50 MHz.
The obtained fit parameters, see Tab.2, in these cases are very different from the Weibull parameters obtained from the test of the configuration register. In particular the energy threshold is practically zero, see Fig.6. This means that even a small

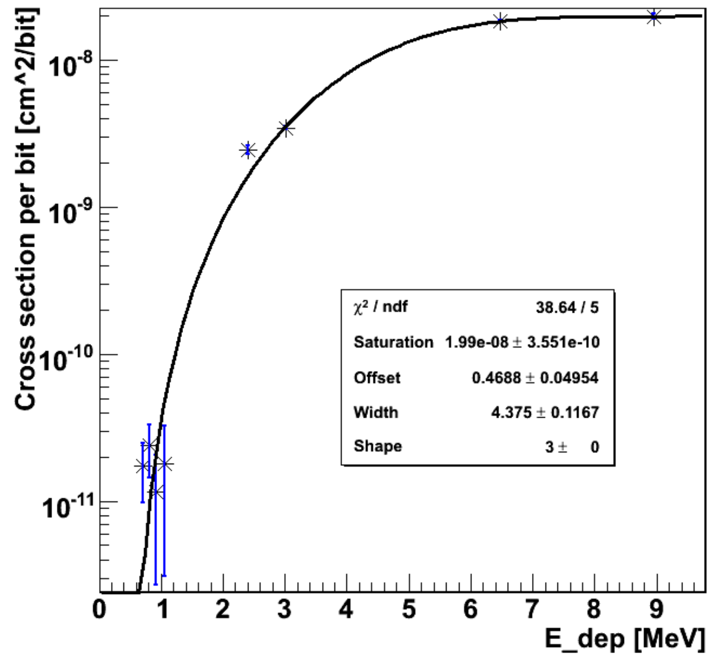

Figure 5: Weibull fit to the experimental ion data of ToPix_2 configuration register. A sensitive volume of 1 μm^3 is assumed.

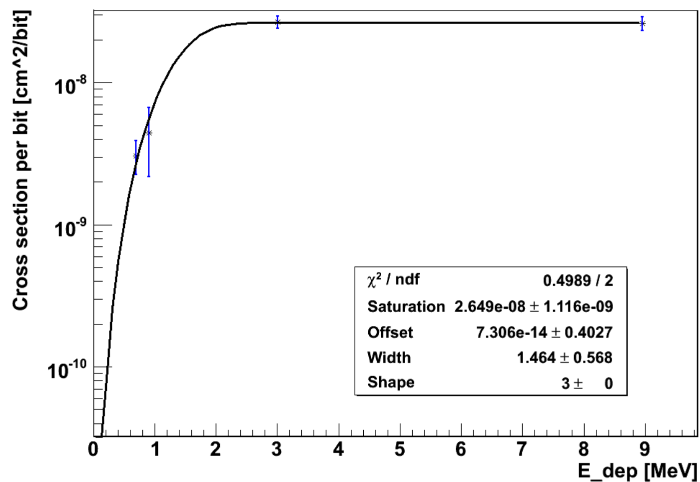

Figure 6: Weibull fit to the experimental ion data of ToPix_2 shift register. A sensitive volume of 1 μm^3 is assumed.

deposited energy can trigger an upset. The saturation cross section is bigger by a factor 2, in agreement with the fact that a higher SEU rate is expected in electronics designed in this standard layout.

Device	E_{th} [MeV]	σ_0 [cm^2 bit^{-1}]	W [MeV]
Shift register	1.58 10^{-15}	2.6 10^{-8}	1.03
12 bit counter	7.31 10^{-14}	2.6 10^{-8}	1.46

Table 2: Fit parameter of the shift register and the 12 bit counter in standard electronics

3 SEU on ToPix_2

In order to obtain the SEU rate, we need to know the probability for a certain particle to deposit a certain energy in the sensitive volume.
The probability value to deposit a certain energy in 1 μm^3 sensitive volume is known, from [1], for four different proton energies. Besides, all other hadrons can be related to the proton, and above 200 MeV the energy deposition probability is almost independent of the particle energy, and the study of the particle environment in $\overline{\text{P}}$ANDA shows that most of the hadrons have energy above 200 MeV. Besides, the lepton contribution is negligible [6].

In order to calculate the rate of SEU for the $\overline{\text{P}}$ANDA hadron flux the following method has been applied. For each energy bin "i" we have an energy deposition probability P_i and we can calculate from the Weibull distribution, the increase of sensitive area in this energy range: $\Delta\sigma_i = \sigma_{i+1} - \sigma_i$. We can then derive the SEU cross section Σ in the hadron environment as:

$$\Sigma = \sum_i P_i \frac{\Delta\sigma_i}{A} \tag{3}$$

where A is the cross-sectional area of the Sensitive Volume (SV).

The evaluated SEU cross section Σ in the hadron environment for the three tested elements of the ToPix_2 prototype, is summarized in Tab.3. Besides, as described before, the SEU cross section Σ has to be corrected for the before mentioned 30 % in order to take into account the under-estimation of the sensitive volume [1]. The corrected Σs are reported in Tab. 4.

Configuration Register	Shift Register	Counter
8.78 10^{-16} [cm^2/bit]	2.96 10^{-14} [cm^2/bit]	4.70 10^{-14} [cm^2/bit]

Table 3: Σ in the hadron environment.

Multiplying the above Σ cross section by the hadron flux, obtained from a dedicated particle rate study [7], the SEU rate for annihilations on proton and on nucleus are obtained. The results are reported in Tab.5.

Taking into account the final design of Topix, we can derive the SEU rate /h in each chip readout taking into account that there are 12760 pixels, and 12 bits either

Configuration Register	Shift Register	Counter
11.65 10^{-16} [cm^2/bit]	3.94 10^{-14} [cm^2/bit]	6.25 10^{-14}[cm^2/bit]

Table 4: Σ in the hadron environment, corrected for the under-estimation of the SV.

Annihilation	Configuration Register	Shift Register	Counter
$\bar{p}-p$	6.99 10^{-9}	23.64 10^{-8}	37.5 10^{-8}
$\bar{p}-N$	1.43 10^{-9}	4.85 10^{-8}	7.69 10^{-8}

Table 5: SEU (bit^{-1} s^{-1}) in the ToPix_2 prototype.

in the registers or in the counter. The estimated rates are listed in Tab.6. The SEU rate for the configuration register corresponds to about 4 upsets in each chip per hour. Considering the total number of chips (824) in the MVD pixel part, we can estimate about 3296 upsets per hour. The SEU rates foreseen for the shift register and the counter are higher in comparison to the configuration register as expected.

Annihilation	Configuration Register	Shift Register	Counter
$\bar{p}-p$	4	130	207
$\bar{p}-N$	1	27	42

Table 6: SEU ($chip^{-1}$ h^{-1}) for $\overline{\text{P}}$ANDA environment, in the final ToPix prototype.

4 Conclusion

The variation of one bit in the digital circuitry (SEU), following the passage of a particle, can be problematic in the $\overline{\text{P}}$ANDA environment. The corruption of the data is not a dangerous effect itself, because the corrupted data can be easily identified and discarded. Instead a more dangerous effect is the loss of the detector control function that can be restored resetting the chip. As a consequence all the data stored from the upset event to the reset operation have to be discarded. As shown there is a relevant different SEU rate between radiation tolerant architecture like the configuration register of ToPix_2 and the non-radiation tolerant architecture, like the shift register and the counter. Our conclusion is that the hardness of the readout chip to the SEU effects has to be improved within the limits imposed by the pixel size. The triple redundancy architecture application could be a solution and it has been already designed for the new ToPix prototype.

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