

Setup of a test-station for double-sided silicon microstrip detectors

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Abstract

A test station for double-sided silicon strip detectors (DSSD) has been set up allowing a full functional characterization of both silicon sensors and connected readout electronics. Due to the modular concept an adaptation to different sensor and frontend types is possible in future applications. First sensor modules have been tested successfully using the APV25 frontend chip. The entire setup can be controlled and monitored with a standard commercial PC. Components for signal processing and data acquisition are either custom made or commercially available. In parallel to a complete online monitoring, data is stored for further offline analysis. First measurements with the implemented sensor modules demonstrate the full functionality of the test station. In addition to a complete characterization of frontend electronics and sensors, results concerning energy deposition of penetrating particles, charge distribution within the sensor and imaging position resolution were obtained.

This article contains a summary of all main components used within the test station, an illustration of the experimental setup and a description of the implemented software and data acquisition. Finally, main results of the measurements are summarized.

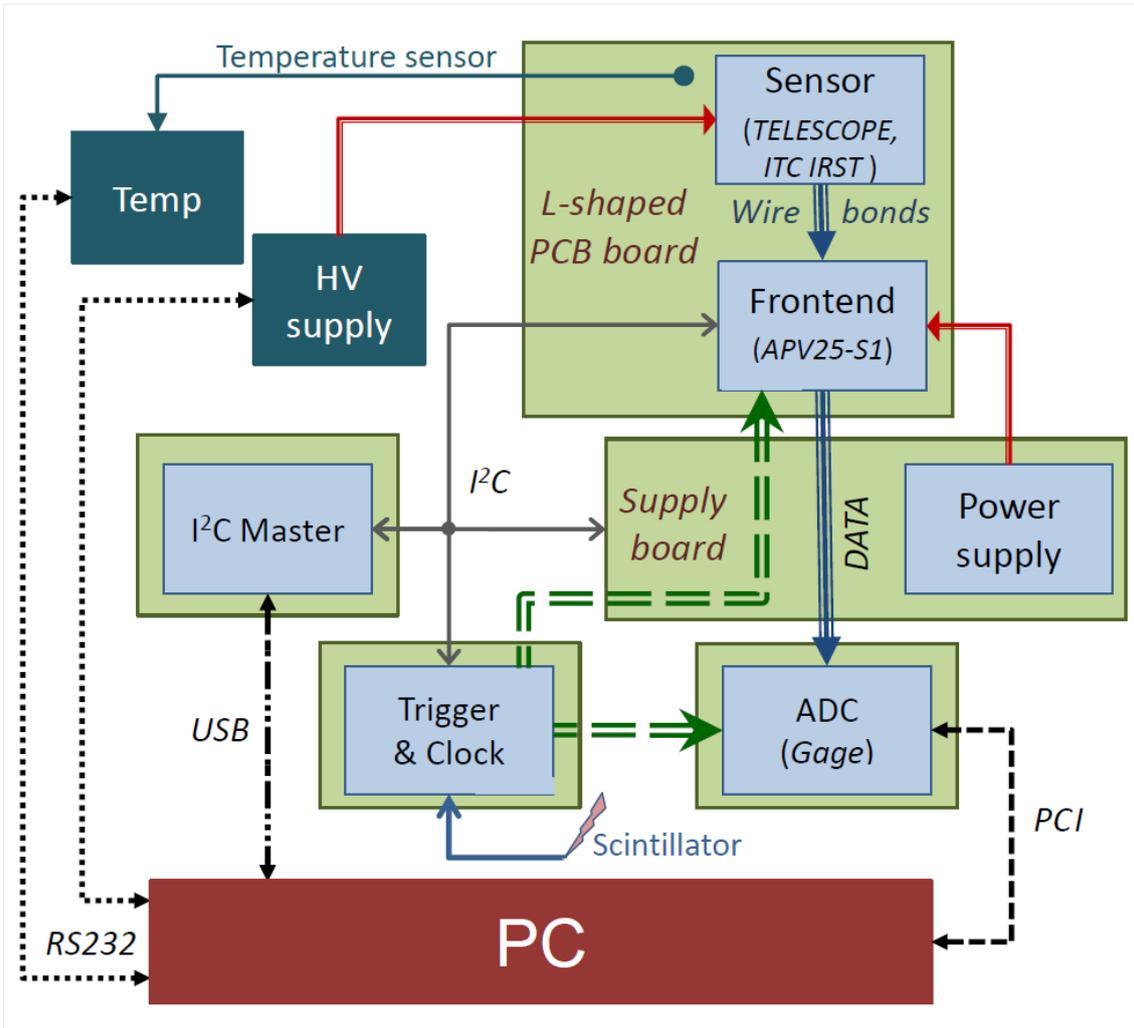


Figure 1: Schematics of the test station with all main components. A modular concept of independent building blocks has been implemented. High voltage (HV) supply [12], ADC card [15] and the FPGA board (using a SPARTAN 3-E) [13] delivering trigger and clock are commercially available modules. All other components have been developed specifically for the test station driven by specifications of the chosen frontend chip (APV25-S1) and the sensor used.

1 Introduction

Double-sided silicon strip detectors (DSSD) are widely used as tracking devices for charged particles. Due to their fast response and the low material budget they became popular in a wide range of applications in high energy physics, hadron physics and medical imaging. One of the large scale experiments in hadron physics intending to use DSSDs is the PANDA experiment [1], [2], at the future FAIR facility [3] where this detector type will be employed, amongst other sub-detectors, within the silicon micro-vertex-detector (MVD) [4].

The implementation of DSSD requires suitable tools to evaluate the main characteristics for both sensors and connected frontend electronics. For this purpose a test station was set up providing a fast and flexible way of different testing procedures. A detailed description of the test station which is schematically shown in figure 1 and the results obtained can also be found in reference [5], [6] and [7].

2 Hardware components

The set-up features a modular concept. A schematic overview is shown in figure 1. The silicon detector is glued to L-shaped circuit boards thus achieving a double-sided readout with one common design. A ceramic pitch adapter is introduced in between sensor and ASIC leading from the readout structure of the DSSD to the inputs on the backside of the frontend chip. Currently, square DSSD with a side length of 2 cm, a thickness of 300 μm , a stereo angle of 90° and a pitch of 50 μm are used [8]. All connections are done by wire-bonding.

The readout is carried out by APV25-S1 frontend chips [9]. A sensor module consists of one sensor and two circuit boards, hence a total number of six frontend chips. A temperature sensor is placed close to both detector and frontend chip. A commercial power supply unit is used for biasing the DSSD [12]. The supply board provides the operating voltage for the ASICs of one sensor module and furthermore acts as repeater and transition card for frontend signals as well as for the trigger and the clock signal. All currents and voltages are measured on board.

Clock and trigger signals are generated with a commercial FPGA board [13] allowing an adjustable clock frequency in the range of 0.5 MHz up to 50 MHz. Moreover, additional specific parameters such as the trigger latency or the number of triggers sent after an external strobe can be defined explicitly.

Slow control for frontends, supply board and FPGA is implemented using I²C standard [14]. The I²C master is integrated within a separate unit (PCB). For digitization a commercial ADC card is used [15] which features a simultaneous sampling of up to eight input channels with a maximum sampling rate of 125 MS/s. The sample clock is synchronized with the system clock delivered by the FPGA. The whole test station is controlled by a standard PC using common interfaces (see figure 1).

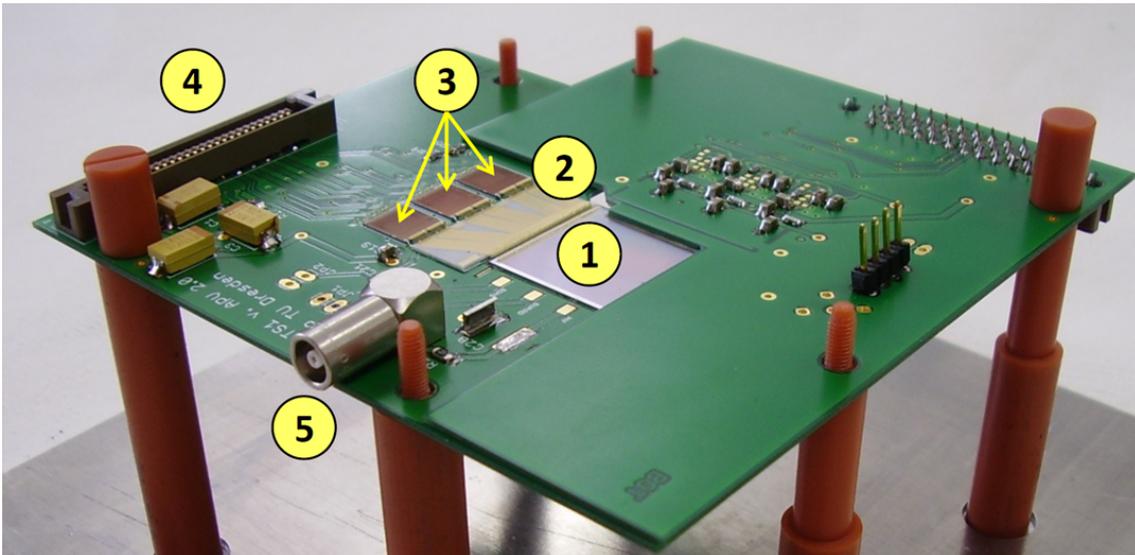


Figure 2: Photograph of a complete sensor-module equipped with two identical L-shaped PCB boards for the double sided readout of the sensor (1). Main components of each individual sensor board: (2) pitch adapter; (3) frontend chips; (4) high density connector for connection of the frontends (power supply, slow control, data output). The HV connection for the sensor (5) is implemented on one board.

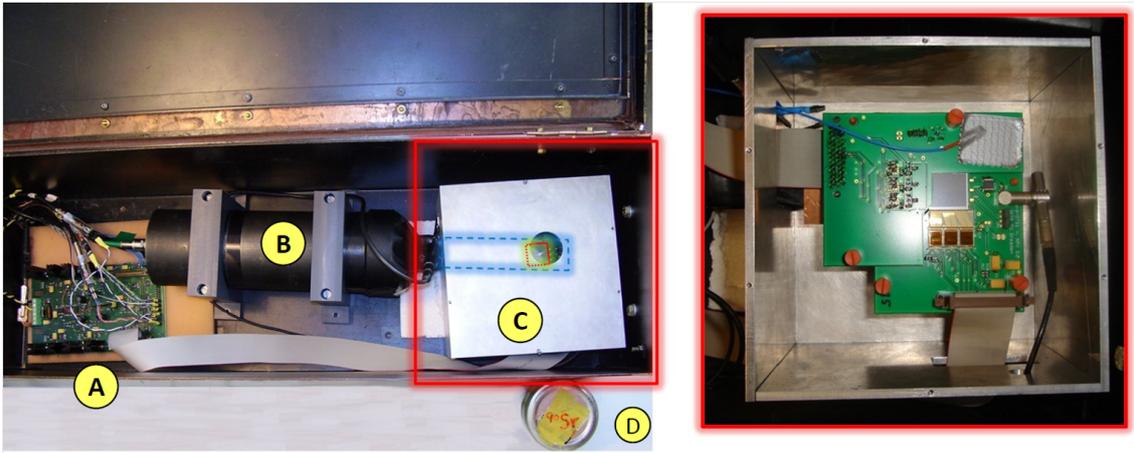


Figure 3: Photographs of the laboratory setup. *Left:* Top view of the opened shielding box: (A) Supply board; (B) Trigger: Photomultiplier connected to a scintillator; (C) Sensor box. The cut-out at the top allows the positioning of the source, e.g. a point-like ^{90}Sr source (D), with respect to the sensor. *Right:* Top view of the opened sensor box with a operational sensor module.

3 Experimental set-up

An aluminum box has been used to house the sensor module and to protect all sensitive elements. Provisions have been made for the positioning of radioactive sources above the sensor under study in order to perform first measurements. A finger-shaped scintillator counter equipped with a photomultiplier is arranged below the DSSD. It delivers a trigger signal for all particle crossing the detector. Together with the supply board this system is put into a light-tight shielding box made of copper.

All other components, including a NIM crate for the signal processing and a HV supply for the PMT of the scintillator counter, are arranged outside the copper box in the laboratory. Photographs of the test station can be found in figure 3, a sensor module board is shown in figure 2.

4 Software and data acquisition

The implemented software controls both the setting and online monitoring of all operating parameters as well as the data acquisition during measurement. Important operating parameters are the supply voltages for sensor and frontends, leakage current of the sensor, power consumption of the frontend chips and the temperature at the DSSD and the frontend chips. Furthermore, specific parameters needed for the setting of the ADC card, the frontend chips and for triggering purposes must be included. Finally, all variables concerning a proper definition and distribution of the system clock have to be taken into account for an accurate operation of the whole system.

In order to start a data acquisition, a trigger signal must be sent via an I²C command to both ADC card and frontend chips. The trigger signal may be delivered either by an external signal from the scintillator or it is created internally on the FPGA board. In this way it is possible to send a physical trigger, a calibration

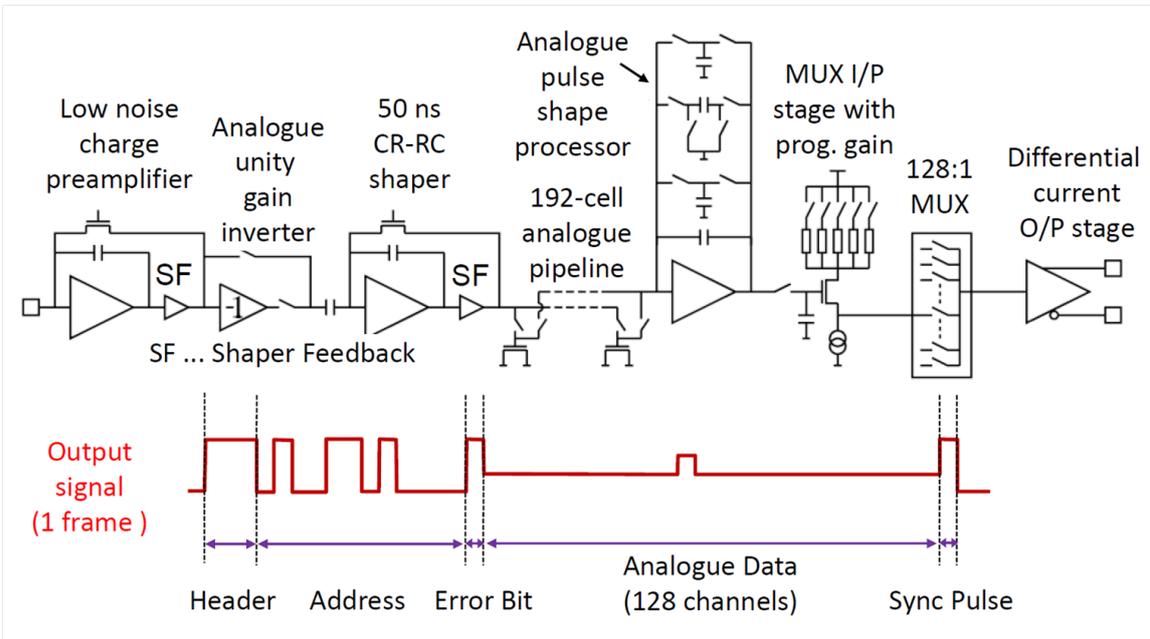


Figure 4: Specifications of the readout chip APV25-S1 currently used in the setup. *Top:* Diagram of the analog chain. Each of the 128 channels has its own chain from the preamplifier to the multiplexer stage [9]. *Bottom:* Serialized data output [11]. Data for a corresponding trigger is delivered within one frame consisting of a digital header and an analog part containing the pulse heights of all channels. Each frame ends with a synchronization pulse.

trigger or a reset pulse to the frontend chips. All input channels of the ADC card are unambiguously connected to the corresponding frontend channels of the sensor module.

The serialized output signal for each frontend (see figure 4) is sampled simultaneously with the given clock frequency. After digitization, all frames are re-extracted from the raw data. Thereby, channels are re-ordered in such a way that they coincide with the running strip number on the sensor. The strip numbers of the second sensor side follow subsequently after the first one in the data stream. In the next step pedestal correction and noise analysis are carried out for all individual channels. Afterwards, a hit finding algorithm is analyzing all appropriate frames belonging to one global event. If a threshold value is exceeded in a given number of subsequent frames (minimum request: $n > 1$) of the same channel, the respective hit information is stored.

Moreover, a cluster finder is implemented allowing the extraction of the hit multiplicity, which is given by the number of activated channels, and the total collected charge within an event. With this information a charge weighted averaging of all neighbouring strips is performed which improves the single-hit position resolution. The charge sum is proportional to the energy loss of the penetrating particle in the detector.

All software components are embedded in a common graphical user interface (GUI) for comfortable handling. Individual buttons enable the initialization of trigger and clock, ADC card and frontends as well as the setting and survey of operating parameters. Online monitoring during the measurement displays extracted frames, noise level and pedestals for all individual channels as well as the histogrammed total charge sum and hit multiplicity for the measured events. All data is stored

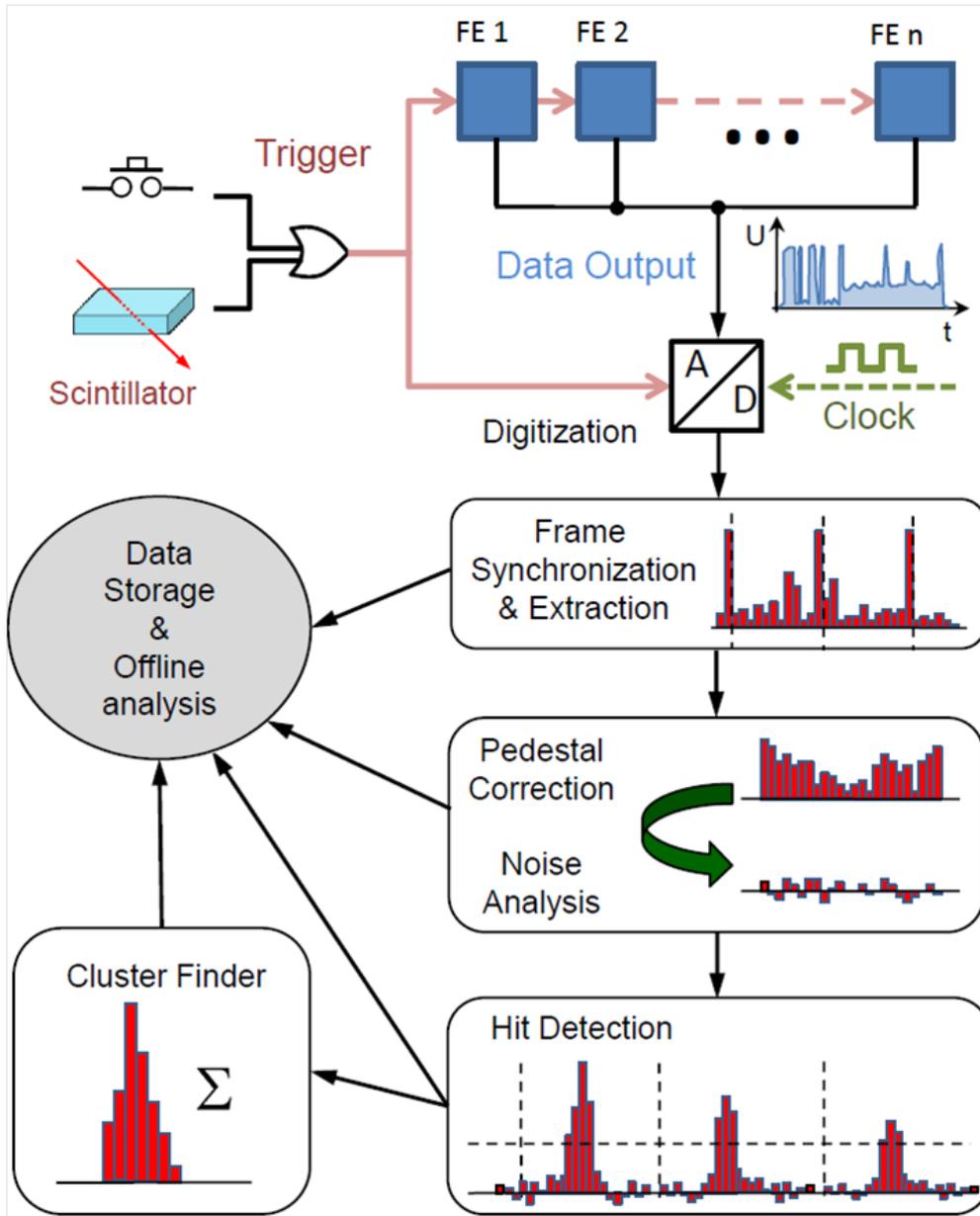


Figure 5: Schematics of the DAQ and the data extraction of the test station.

for further offline analysis. Archive storage of datasets for all sensor modules is organized in a MySQL database allowing e.g. permanent access to calibration data of each individual module, which is needed in the analysis. A schematic overview of the data acquisition is given in figure 5.

5 Measurements and Results

Before measuring with external sources both frontend chips and DSSD must be characterized. A check of functionality for all frontends includes internal calibration as one of the main features. Therefore, well defined charges are injected into each single channel and the resulting pulse height of the corresponding output signal is stored. The scan is performed over the full dynamic range. The APV25 frontend

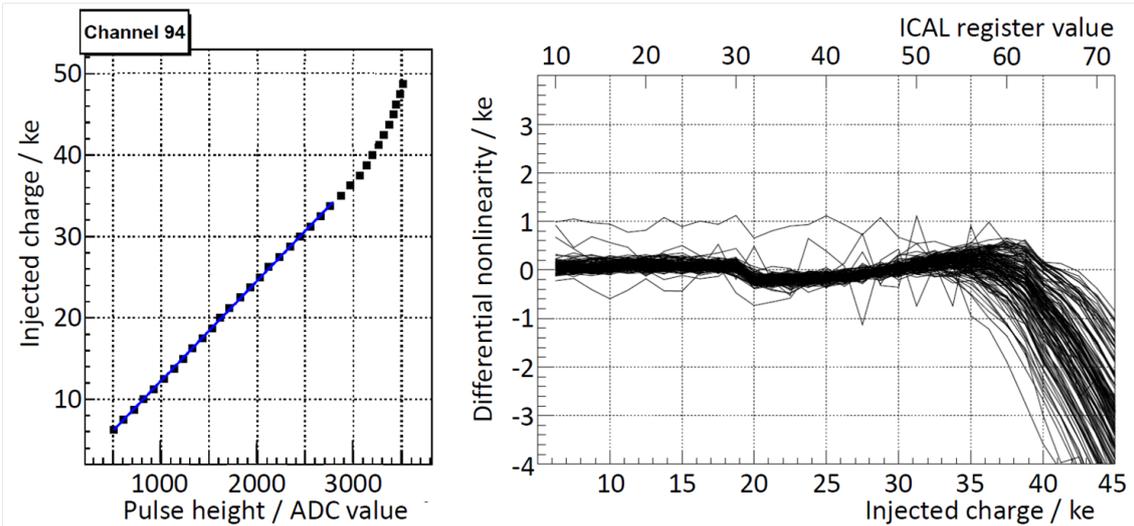


Figure 6: Frontend calibration: Scan of output pulse height versus injected calibration charge measured in thousands of electrons (ke) for a selected single frontend channel (*left*). The procedure is performed for all channels of each frontend chip. Deviations from the linear fit are plotted for all 128 channels of one selected frontend chip (*right*). The register values to be set for nominal input charges are indicated at the top axis above. A good linearity is obtained within a wide range. Deviations at high injected charges are due to saturation effects in the analog part of the frontend chip.

chip provides an internal calibration which was used for this procedure. An on-chip pulse generator can be enabled to inject charge with programmable amplitude into a group of 16 channels [10]. The register values set for the calibration pulse can be translated into a charge quantity using the information given in [11]. Results for one selected channel and the corresponding frontend are shown exemplary in figure 6. Moreover, the noise level for each channel and the leakage current for the DSSD are important for the characterization of individual sensor modules.

Further analysis of both parameters allows a determination of the full depletion voltage at which the depletion zone within the sensor extends over the full thickness. This is illustrated in figure 7 for a selected sensor module. Increasing the applied bias voltage, the mean ENC noise per channel decreases due to the expansion of the depletion zone. At higher voltages, a full depletion of the sensor is obtained and the ENC noise levels out. In addition, a change of slope at full depletion voltage is also observed for the leakage current. The increase of leakage current below the depletion voltage is higher compared to the region above where it is given by purely Ohmic contributions.

Apart from characterization, measurements with external radioactive sources or cosmic radiation allow a variety of complementary studies aiming at information on energy deposition of penetrating particles, cluster sizes and spatial resolution of the system. Figure 8 displays the energy deposition of electrons emitted by a ^{90}Sr source. The spectrum at the left frame contains the energy information of both detector sides and is characteristic for the energy deposit of nearly minimizing ionizing particles which is induced by the high energy β -electrons of the source. The low energy part of the spectrum is oppressed by threshold setting of the scintillator counter and due to absorption of the electrons before reaching the detector.

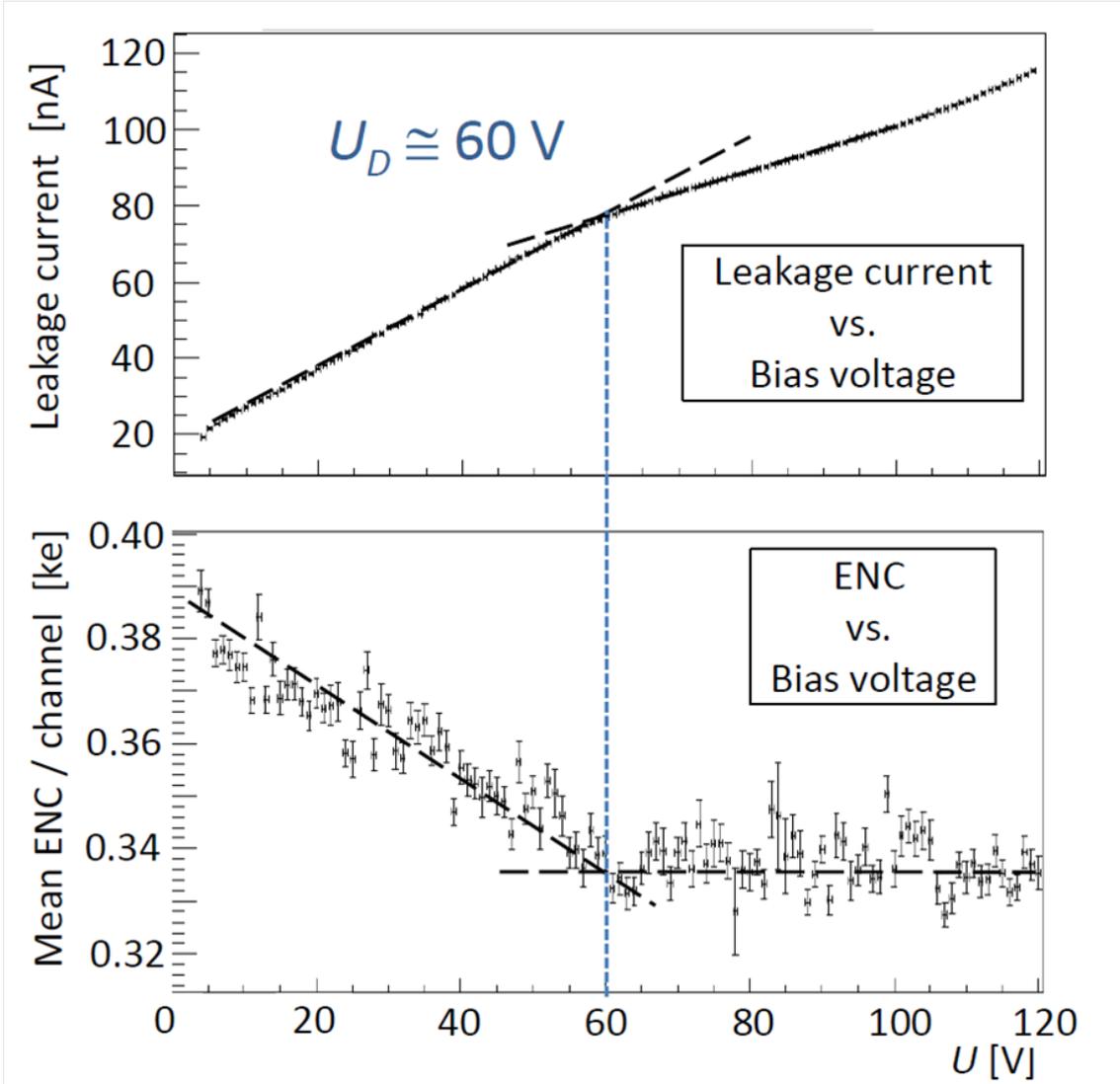


Figure 7: Characterization of the DSSD: Measurement of leakage current and mean ENC noise per channel versus applied bias voltage. Reaching full depletion, the ENC noise arrives at a plateau. In addition, a change of slope at depletion voltage (U_D) is also observed for the leakage current. Further increase at higher voltage is due to Ohmic contributions. (Plotted lines are given to guide the eye.)

The values for the energy deposition E_{dep} are calculated as follows:

$$E_{dep} = \frac{Q_{coll}}{(\epsilon \cdot d)} \cdot \bar{E}_{Si} \quad (1)$$

where Q_{coll} and d are the collected charge and the thickness of the DSSD (300 μm), respectively. Q_{coll} is obtained after the frontend calibration described above which correlates the measured ADC channel with an equivalent charge. $\bar{E}_{Si} = 3.6$ eV corresponds to the average energy needed to create one electron-hole pair in Silicon. In addition, a scaling factor of $\epsilon = 0.5$ is introduced which appeared to be a systematic deviation from the expected values during the energy calibration with different gamma sources. The origin of this factor is still under study. Possible explanations are a lowered charge collection efficiency, a smaller effective depletion zone or most likely uncertainties of the absolute internal APV calibration procedure as indicated also in [10].

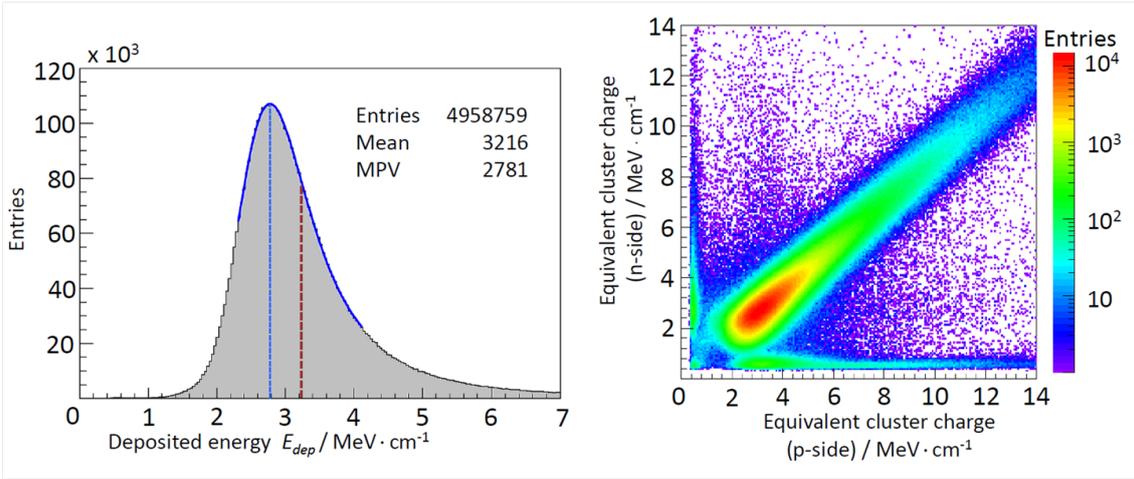


Figure 8: Spectrum of deposited energy obtained for electrons of a ^{90}Sr source (*left*). Data can be fitted with a convolution of a Gauss and a Landau distribution. *Right:* Correlation of the cluster charges for both sensor sides (p-side and n-side).

The shape of the energy distribution can be described with a convoluted function of a Gauß and a Landau distribution. The mean value for the deposited energy is equal to $3216 \text{ keV} \cdot \text{cm}^{-1}$ and in good agreement with literature [16].

In addition to the energy distribution, deconvoluted information of the created charge for both sides is plotted. The charge collection of both sensor sides is linearly correlated indicating a proper operation of the sensor. The slope in figure 8, right frame, is slightly smaller than unity indicating a higher charge collection efficiency for electrons on the n^+ -side than for holes on the p-side.

Figure 9, left frame, shows the cluster multiplicities for both sensor sides, which are given by the number of contributing channels for a single event. Results were obtained in a long-term measurement with ^{90}Sr . The most probable cluster size is two; the mean value for the cluster multiplicity is slightly higher indicating a con-

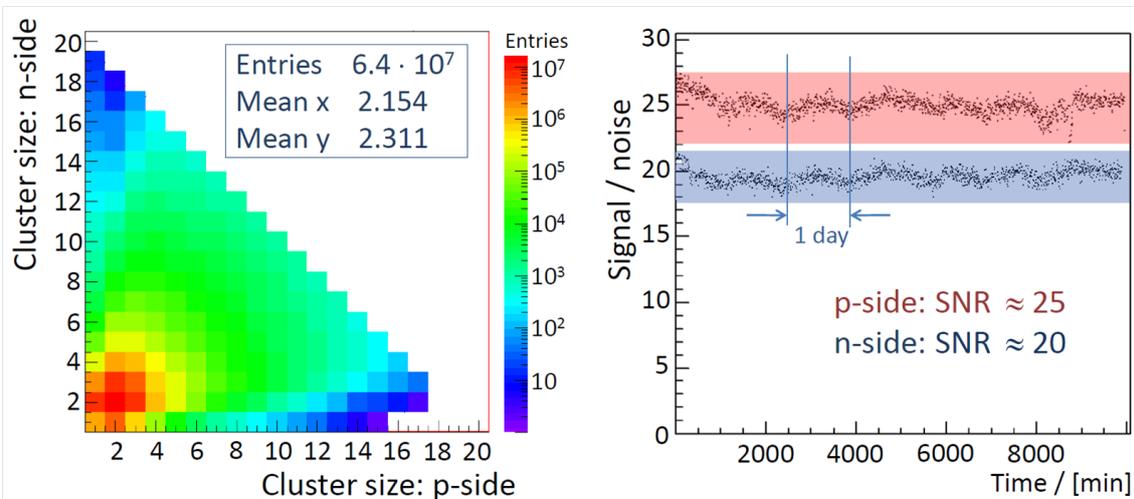


Figure 9: Long-term measurements with ^{90}Sr . *Left:* Cluster multiplicity obtained for both sensor sides. *Right:* Extracted signal-to-noise ratio for the p-side and the n-side, respectively. Relative fluctuations remain within 20% indicating the long-time stability of the system.

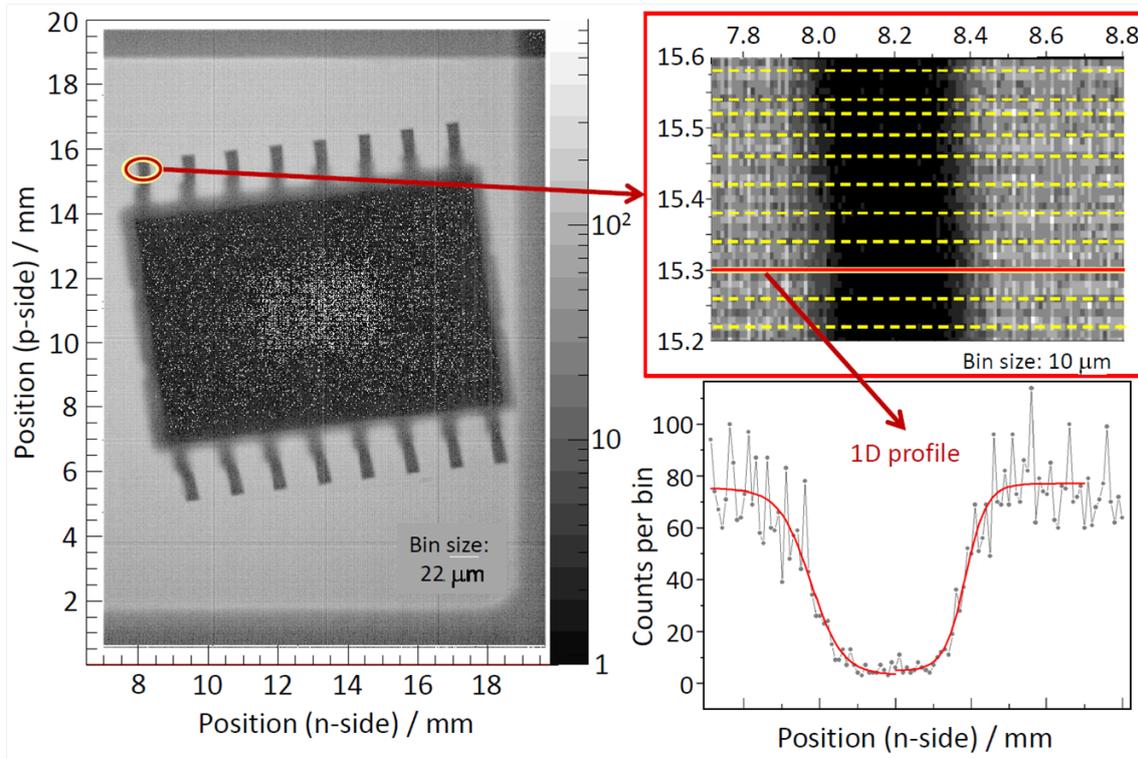


Figure 10: 2D imaging of a SMD device placed on top of the sensor and acting as an absorber for the β -electrons of a ^{90}Sr source (*left*). *Right, top:* Enlarged area under investigation with selected profiles for the resolution studies. *Right, bottom:* Example of an extracted 1D profile fitted with two S-curve functions (red) at the edges. The fit procedure is described in figure 11.

tribution of events with larger cluster sizes. The correlation of both sensor sides does not indicate significant asymmetry. Small deviations result from the different charge carriers collected, which are electrons and holes for the n^+ -side and the p-side, respectively. This fact is also reflected within the signal-to-noise ratio (SNR) extracted from the same measurement. Results are shown in the right frame of figure 9. The SNR on the p-side is 25 on average, for the n-side a value of 20 is obtained. Systematic variations are correlated for both sides and related to changes in environment during the seven days of measurement. A change of the room temperature is the main source of these fluctuations which follow a daily cycle.

Finally, the spatial hit information can be translated into a 2D image as shown in figure 10. In this example an SMD device put on top of the sensor was acting as an absorber for the electrons emitted by a ^{90}Sr source. Due to the charge-weighted averaging within the respective cluster the hit-point for each single event can be extracted with higher precision. Thus, obtaining quasi-analog values for the spatial coordinates, a finer binning compared to the given strip pitch can be chosen for imaging. In order to perform a quantitative analysis of the image resolution, eleven different 1D profiles of a selected area were extracted which include two edges of the mapped object. The fitting procedure for one edge is exemplarily illustrated in figure 11. The image resolution is determined to $49 (\pm 7) \mu\text{m}$ (FWHM) which is the average value of all 22 analyzed edges. The error given is equal to the standard deviation of the average of all measurements and dominated by scattering of the electrons which have rather low momenta. It should be noted that the obtained

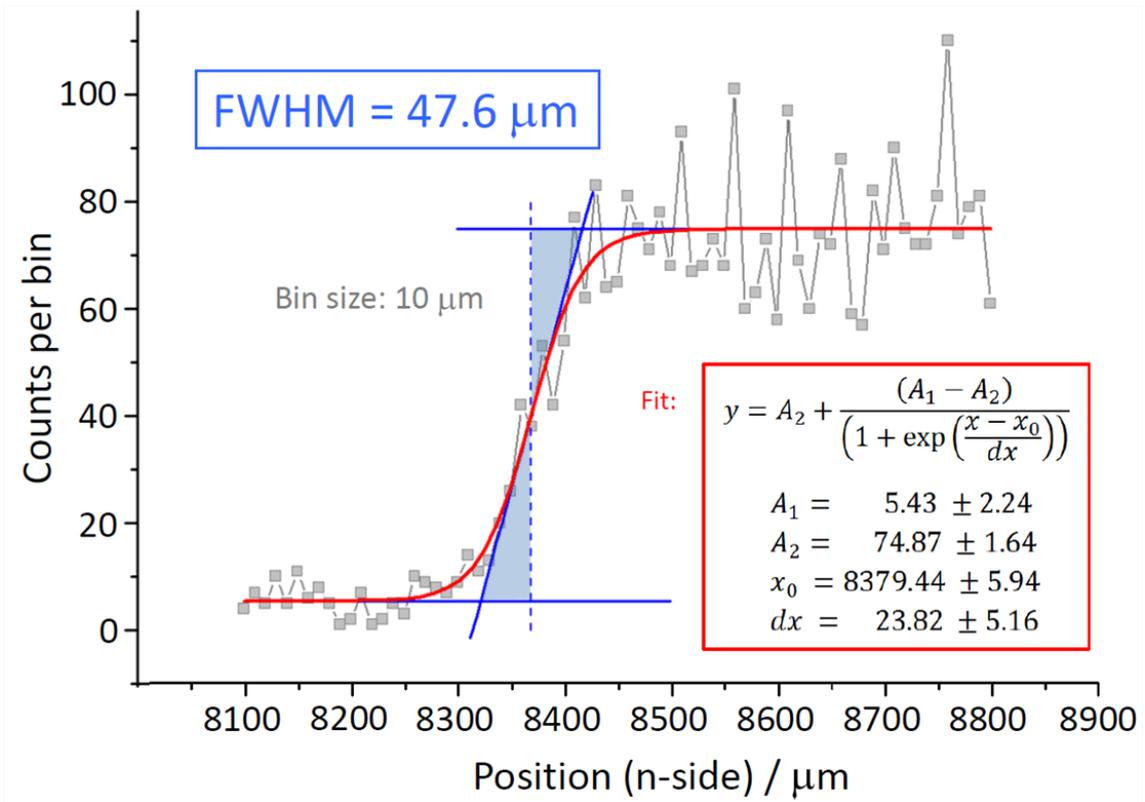


Figure 11: Determination of the image resolution at one edge of an extracted 1D profile. The fit function (red line) allows an extraction of two intensity levels and the slope of the edge (blue lines). The image resolution (highlighted in light blue) is given as the full-width half-maximum (FWHM).

image resolution overestimates the intrinsic detector resolution which is expected to be far better. In order to determine this property an explicit analysis of the hit information of single events is necessary. Therefore, a full tracking station is needed which is built up of several stations equipped with DSSD. The presented test station for a single sensor can be easily implemented in such a system.

6 Summary and Outlook

The described test station allows a full characterization of complete sensor modules including both sensor and frontend electronics. The setup has been successfully installed and an evaluation of first sensor modules has been completed. The tested modules are used in further applications, which are based on the presented concept. These ongoing developments comprise e.g. a tracking station built at the University of Bonn as well as test-setups for the luminosity monitor and the hyper-nuclei program of PANDA. The advanced setups also allow an operation at beam facilities such as the ELSA facility in Bonn, the COSY ring in Jülich or at DESY in Hamburg. First beam times have been delivered already. A modified test setup will be used for the characterization of dedicated PANDA prototypes.

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