TWEPP 2014

Sezione di Torino

The ToPiX v4 prototype for the trigger-less readout of the PANDA Silicon Pixel Detector

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Outline

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- The PANDA Micro Vertex Detector
- Readout architecture
- The ToPiX v4 ASIC
- Test results
- Radiation test results
- Conclusions

The PANDA experiment

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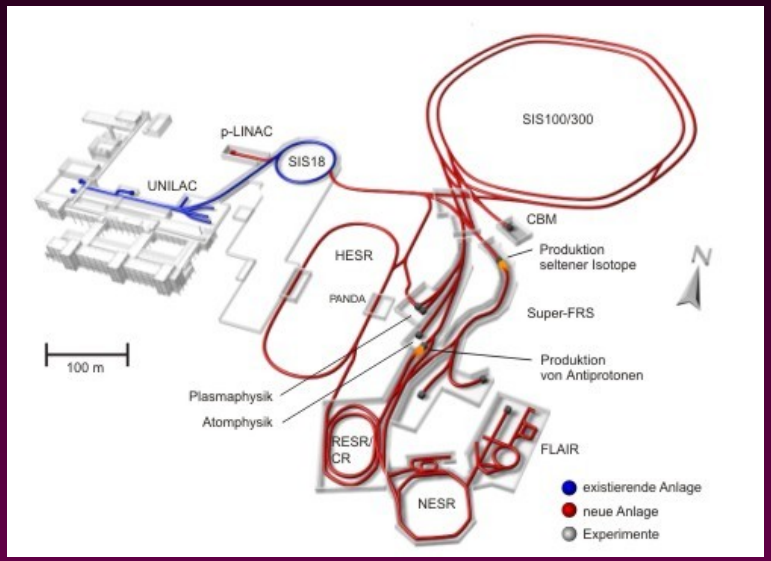

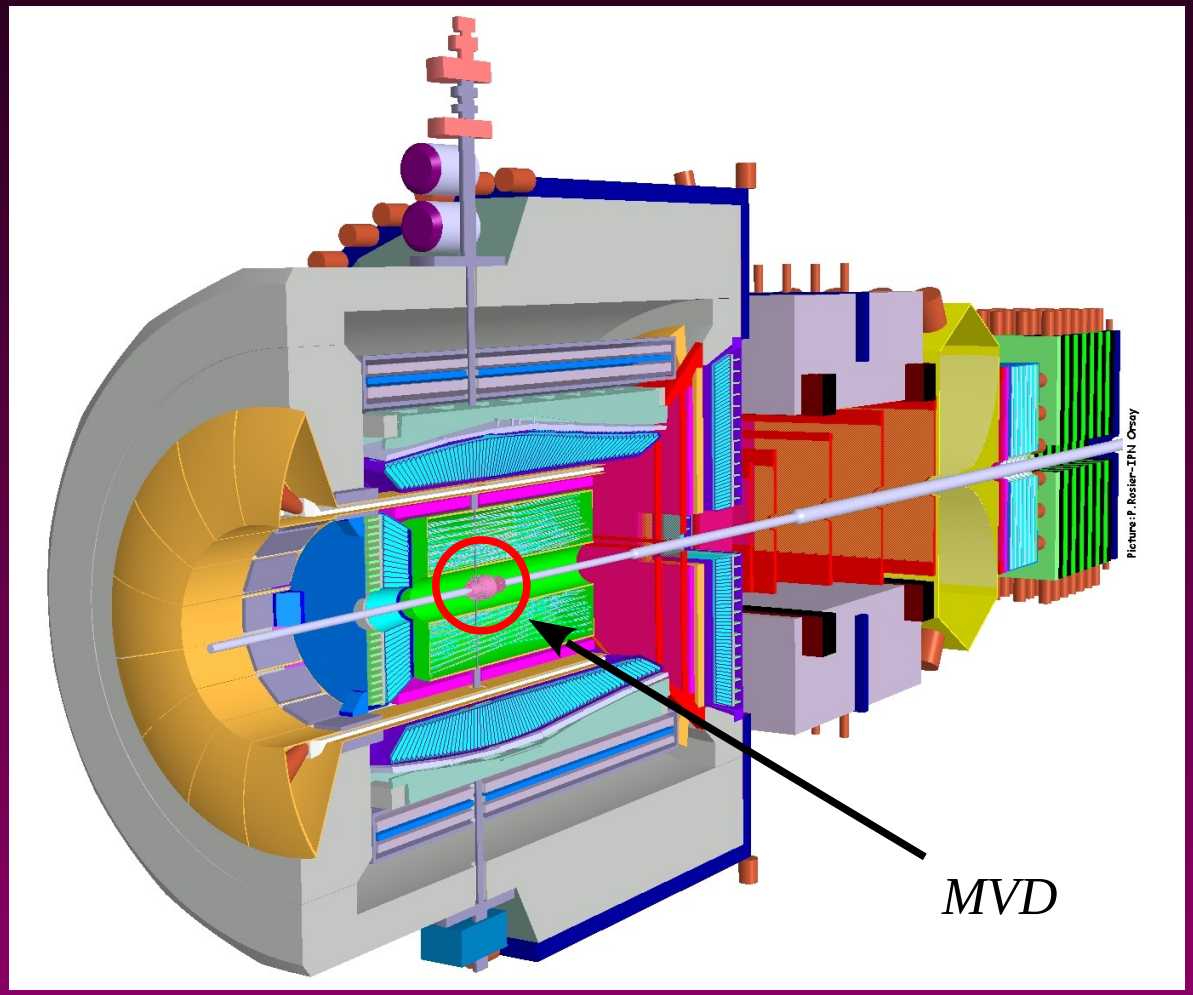

Located at the new FAIR facility

p-p and p-nucleous annihilation reaction

Beam and target pipe

Triggerless experiment

PANDA MVD

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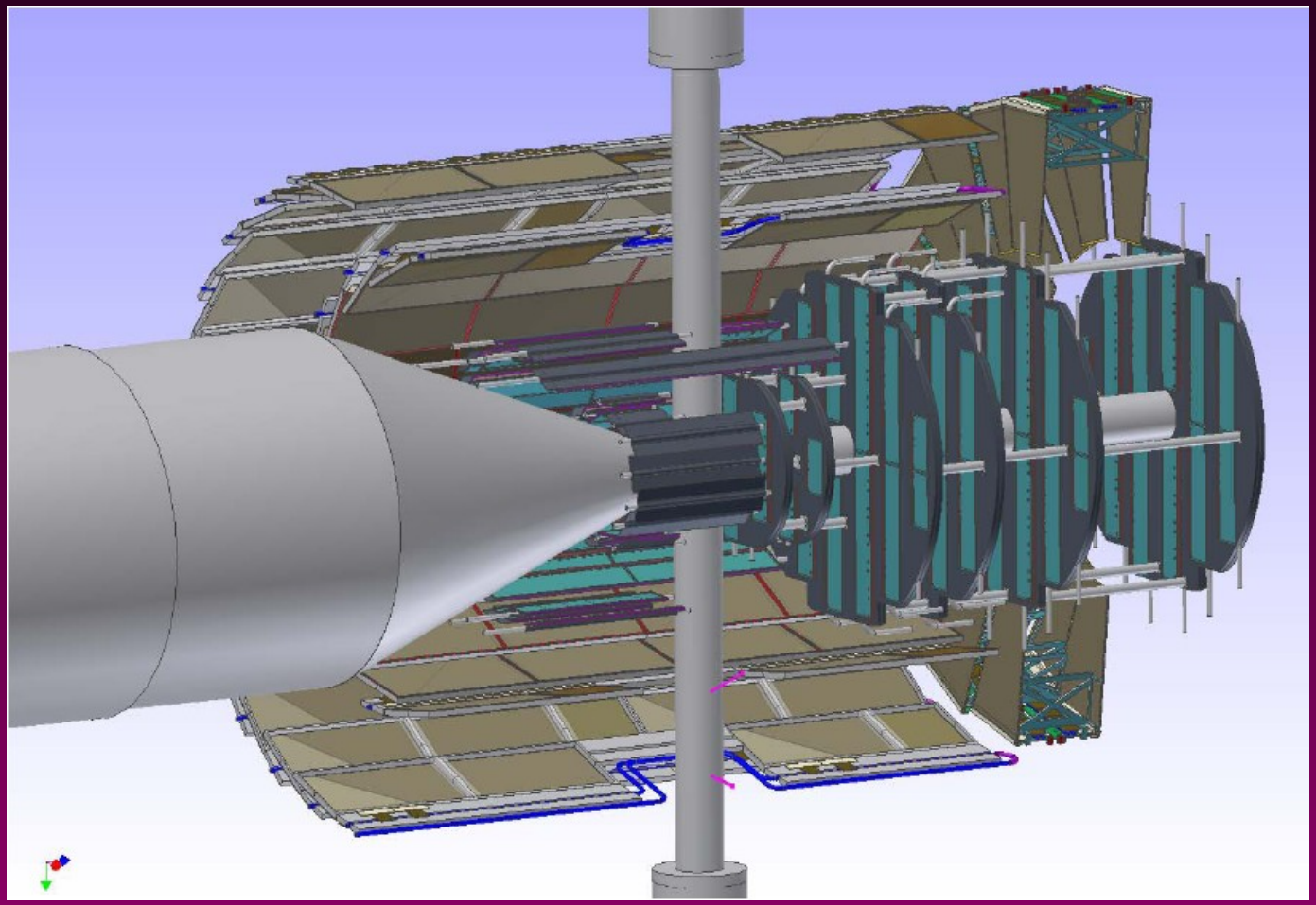

- Barrel :

Layer 1 : radius 28 mm, SPDs

Layer 2 : radius 53 mm, SPDs

Layer 3 : radius 92 mm, SSDs

Layer 4 : radius 120 mm, SSDs

- Forward :

Disks 1-2 : radius 37.5 mm, SPDs

Disks 3-4 : radius 75 mm, SPDs

Disks 5-6 : radius 130 mm, SPDs + SSDs

Pixel Detector

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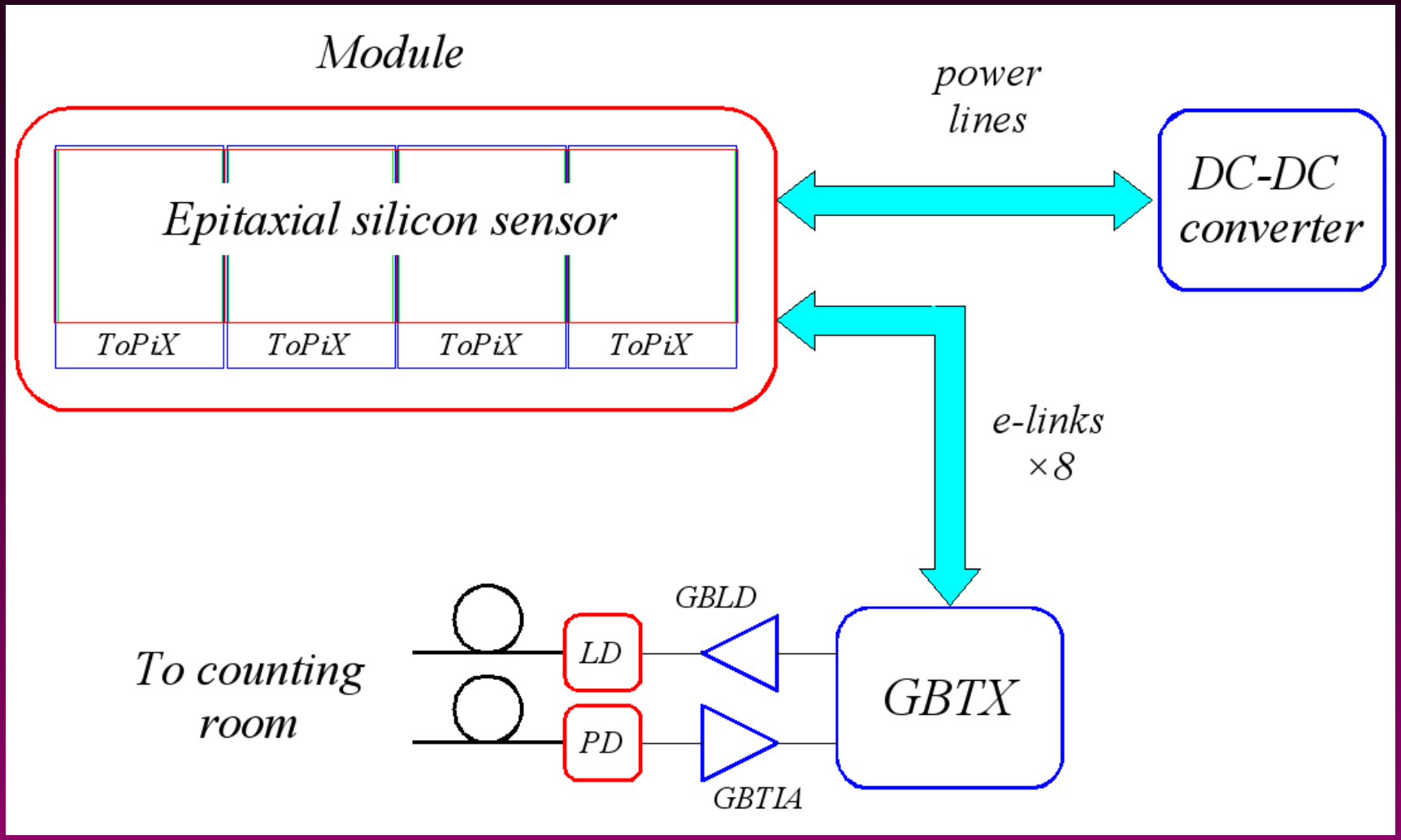
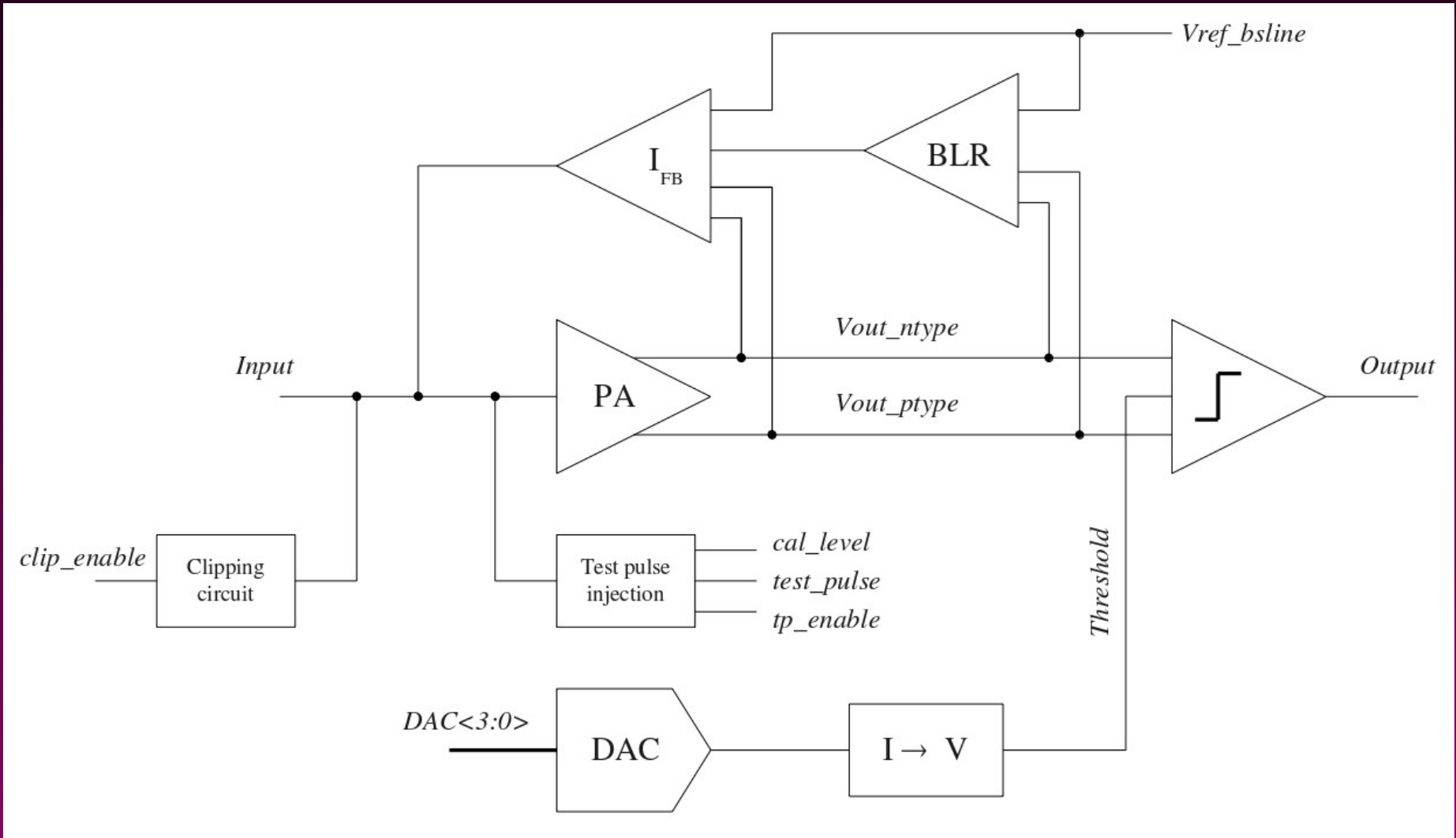
Pixel size	$100 \times 100\ \mu m^2$
Chip active area	$11.4 \times 11.6\ mm^2$ (116 rows, 110 columns)
dE/dx measurement	ToT, 12 bits dynamic range
Max input charge	50 fC
Noise floor (PA noise)	<32 aC (200 e^-)
Input clock frequency	160 MHz
Time resolution	6.25 ns (1.80 ns r.m.s.) 12.5 ns (3.61 ns r.m.s.)
Power consumption	< 800 mW/cm^2
Max event rate	$6.1 \cdot 10^6$
Total ionizing dose	< 100 kGy

Module readout



F/E schematic



Pixel cell schematic

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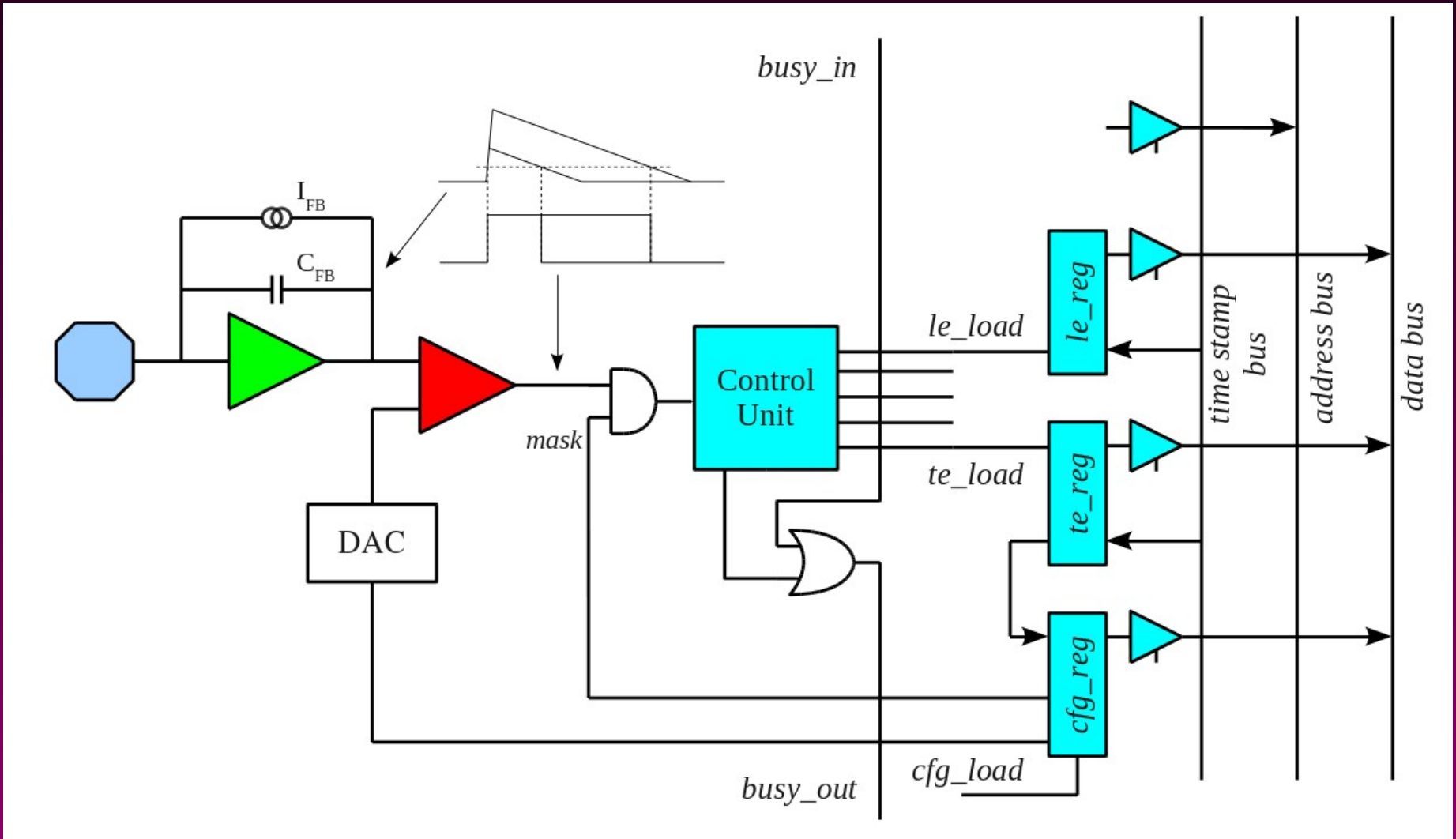
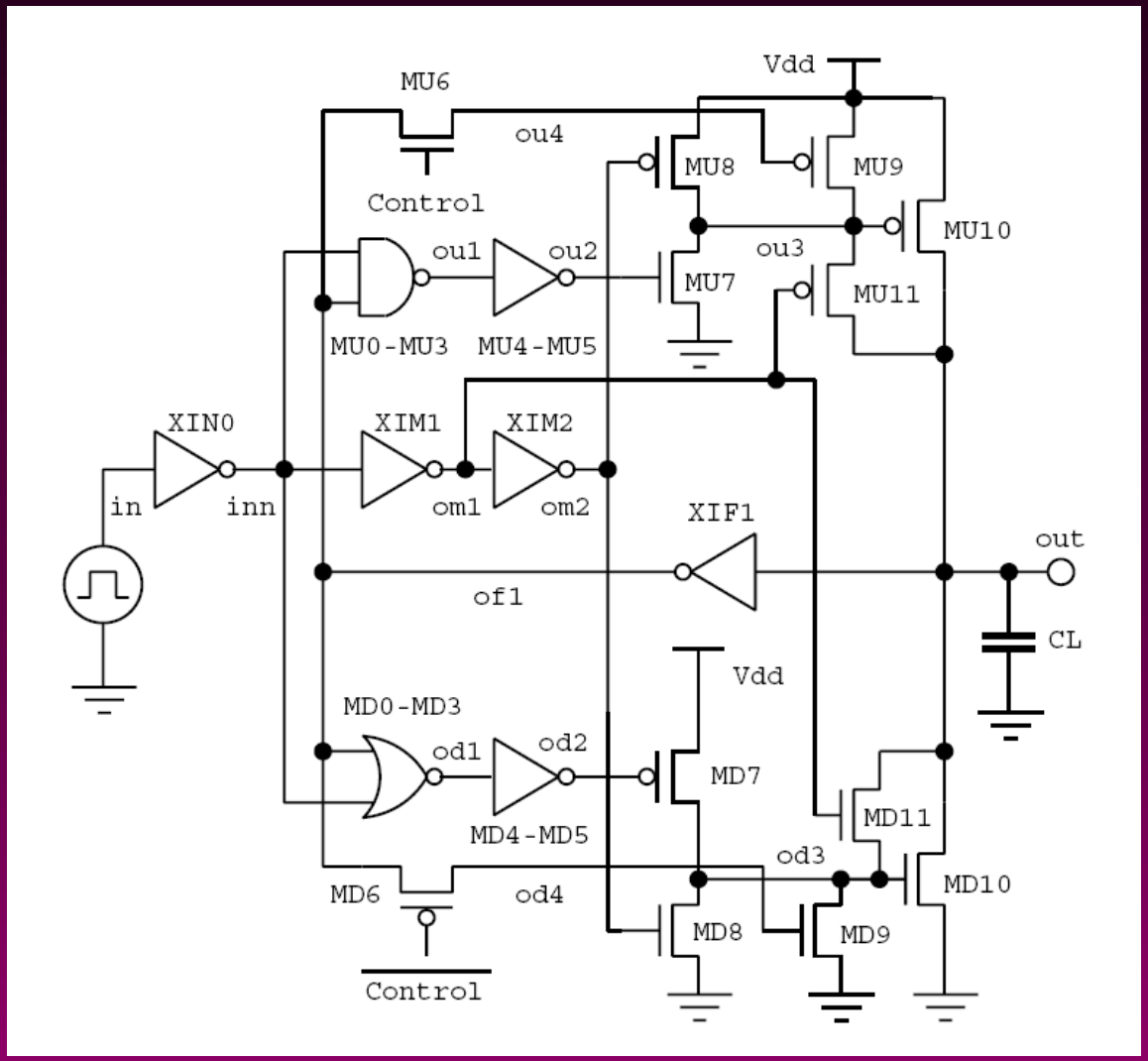


Line driver



Bus capacitance : 49.9 fF/cell
Bus resistance : 9.3 Ω/cell

Provides both reduced voltage swing and pre-emphasis or full voltage swing

J.C.Garcia, J.A.Montiel, S.Nooshabadi
Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects
ISCAS 2007

ToPiX readout architecture

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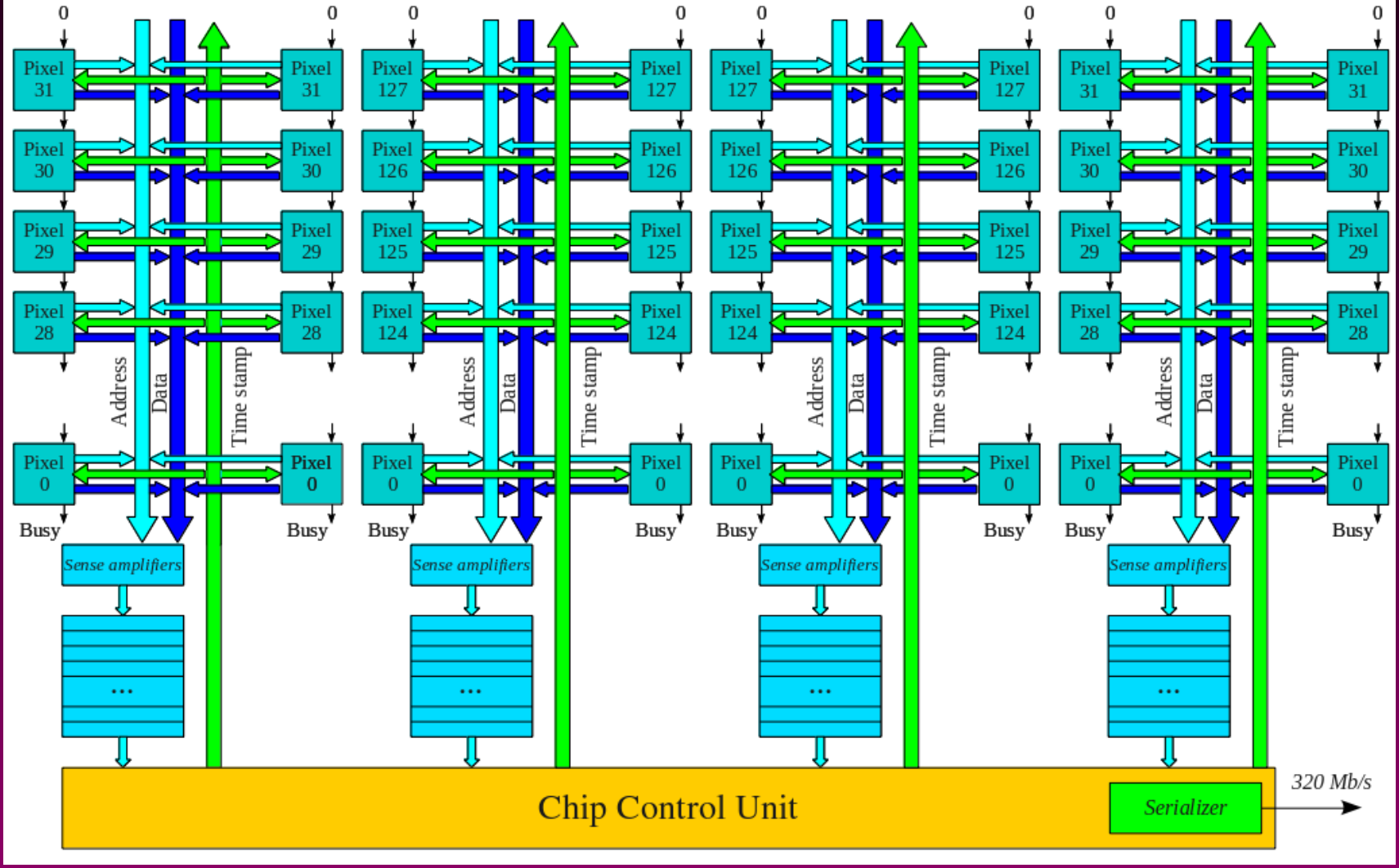

Data format

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2	12	8	12	6
01	Chip address	FC	Not used	ECC

Frame header packet

2	14	12	12
11	Pixel address	Leading edge time	Trailing edge time

Data packet

2	16	16	6
10	# of events	CRC	ECC

Frame trailer packet

2	38
00	idle code (Hex 3A55AA55AA)

Idle packet

ToPiX v4

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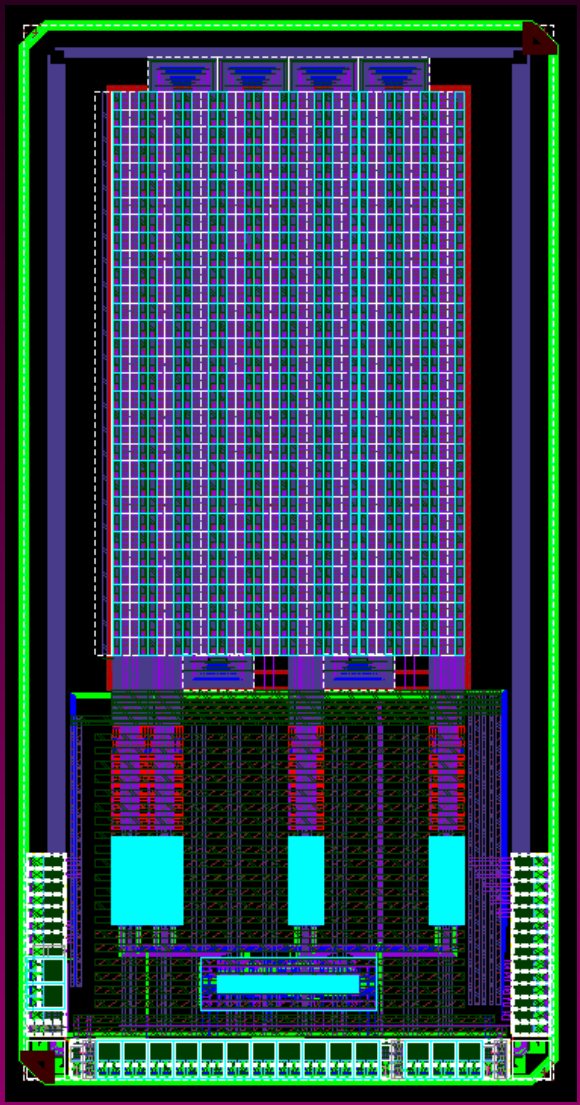
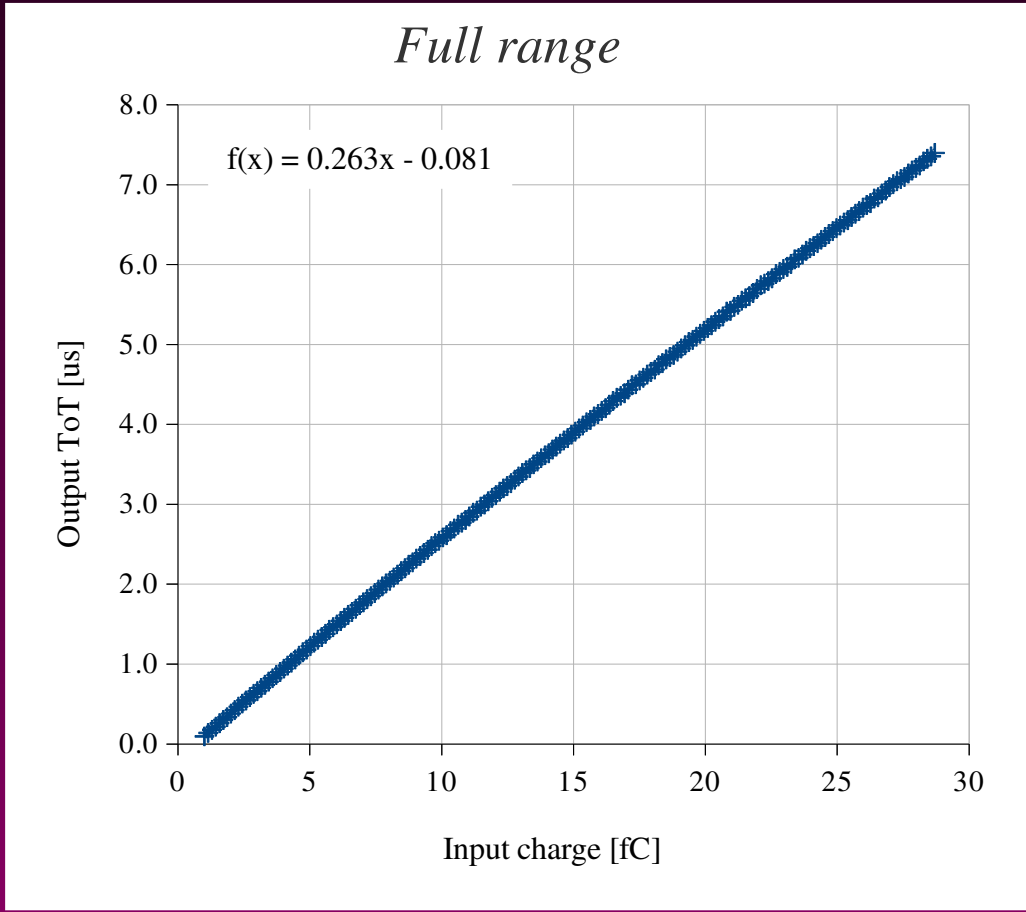
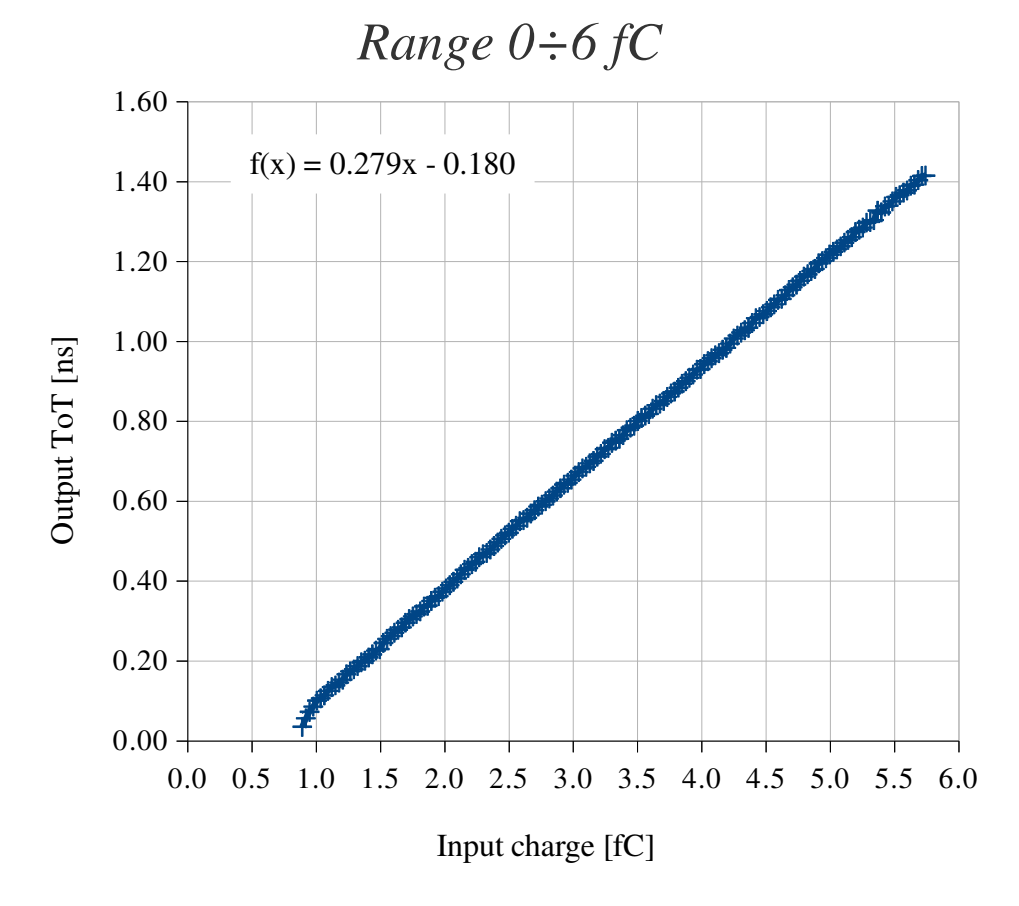


- Size : 3 mm × 6 mm
- CMOS 130 nm
- 640 pixel cells, 2×2×128 and 2×2×32 columns
- Hamming encoding and TMR pixel logic protection schemes
- Clock frequency 160 MHz
- SEU protected EoC
- Serial data output (SDR and DDR)
- GBT-compatible SLVS I/O

ToT measurements

Sezione di Torino





Simulated value : 0.226x + 0.084

Noise measurements

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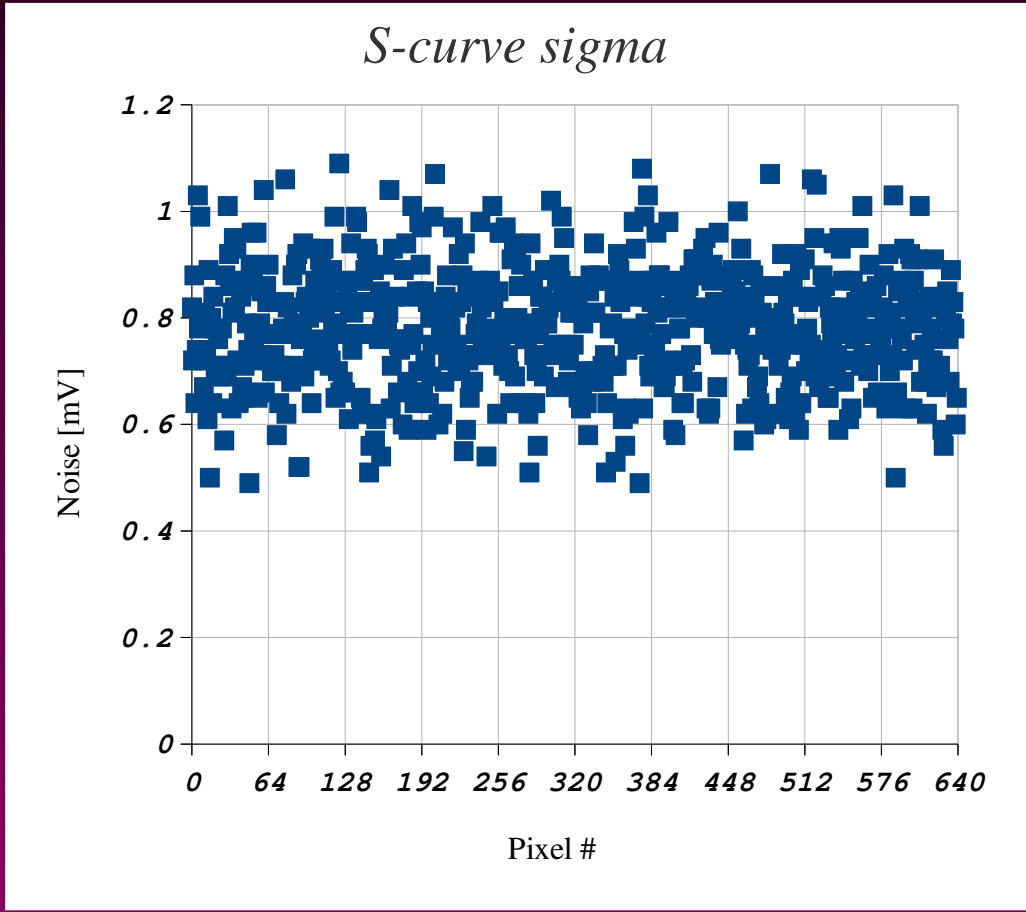

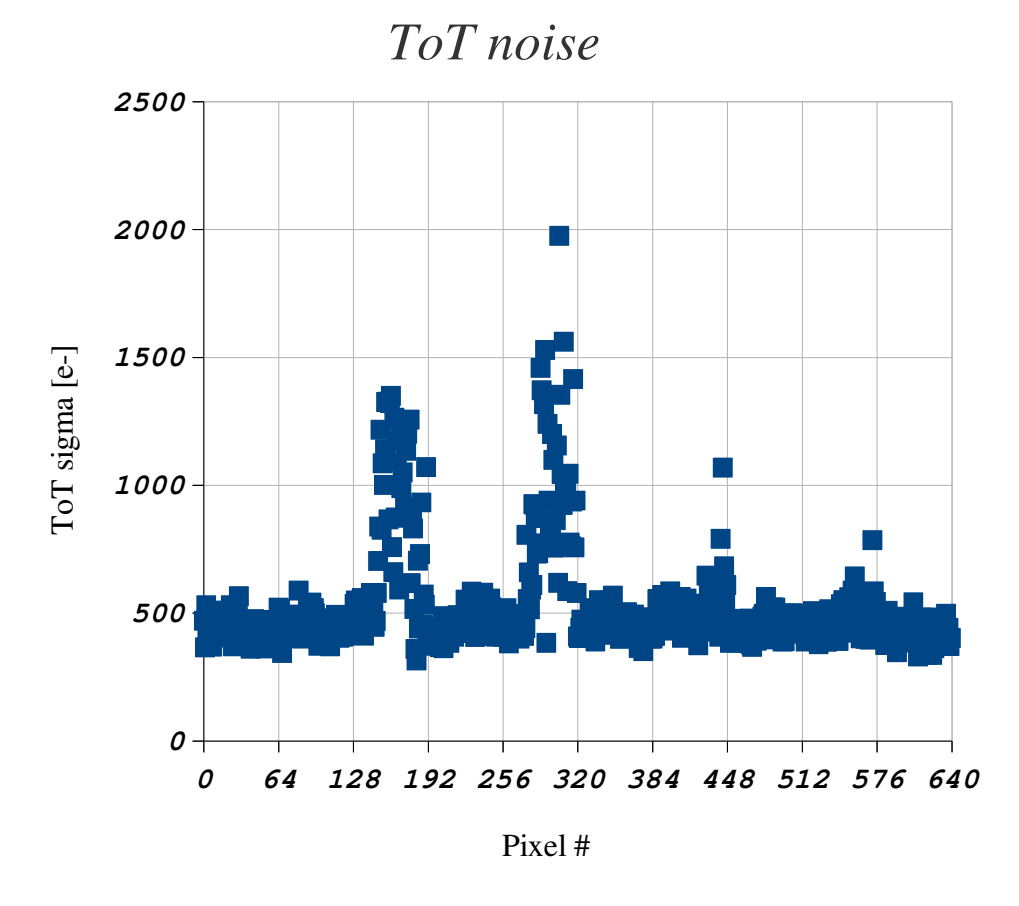

Baseline & ToT

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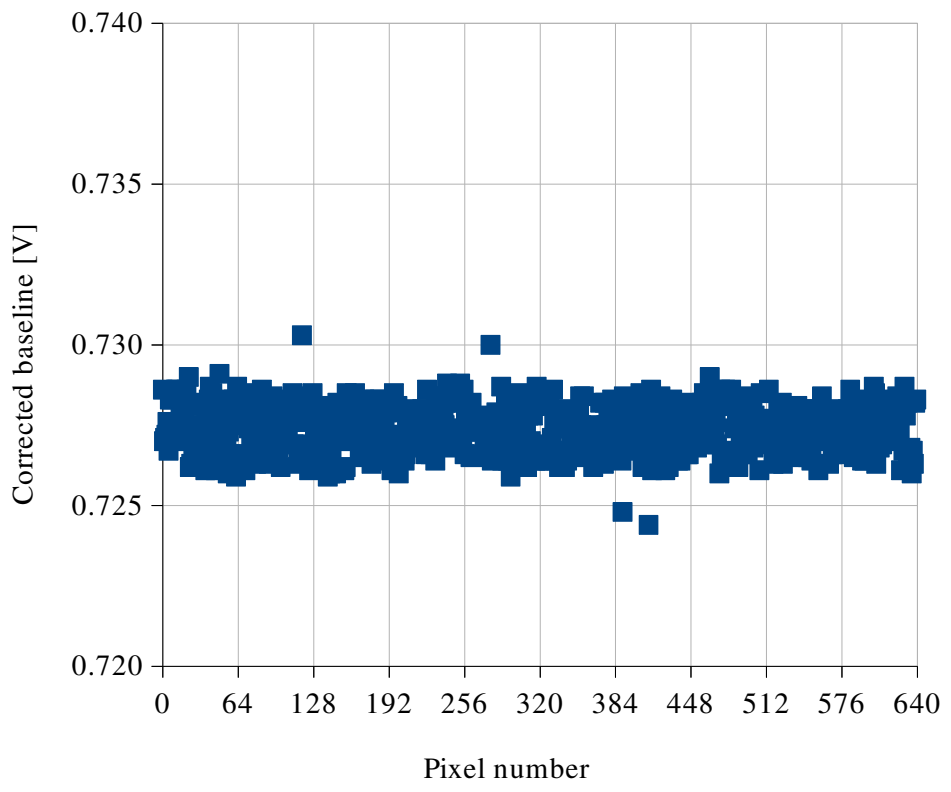
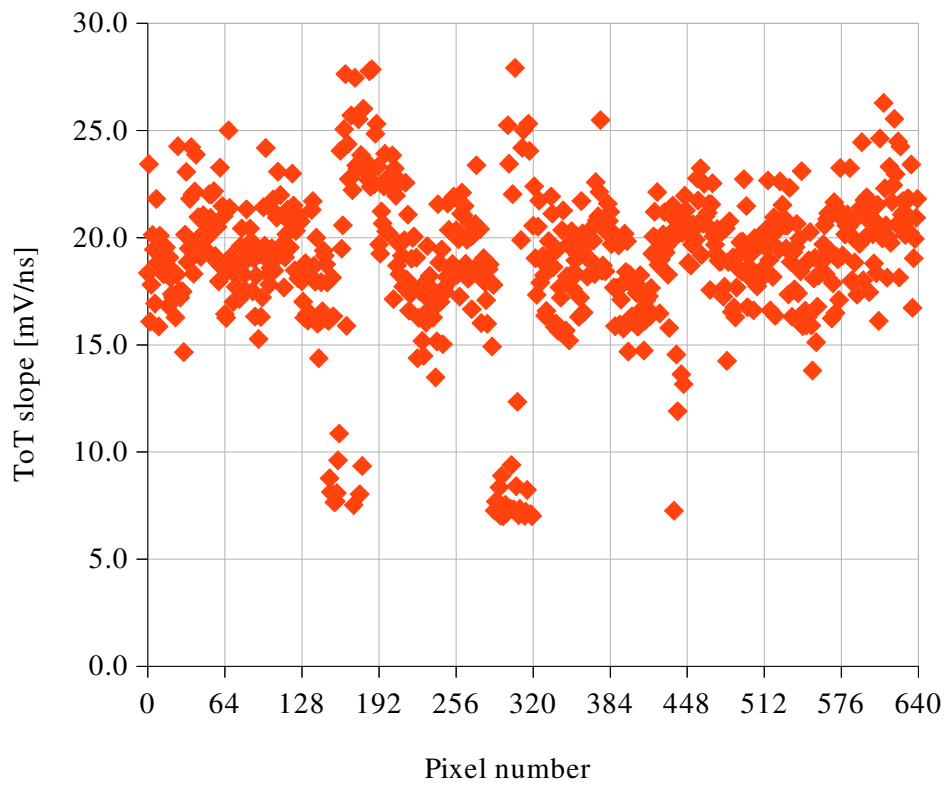
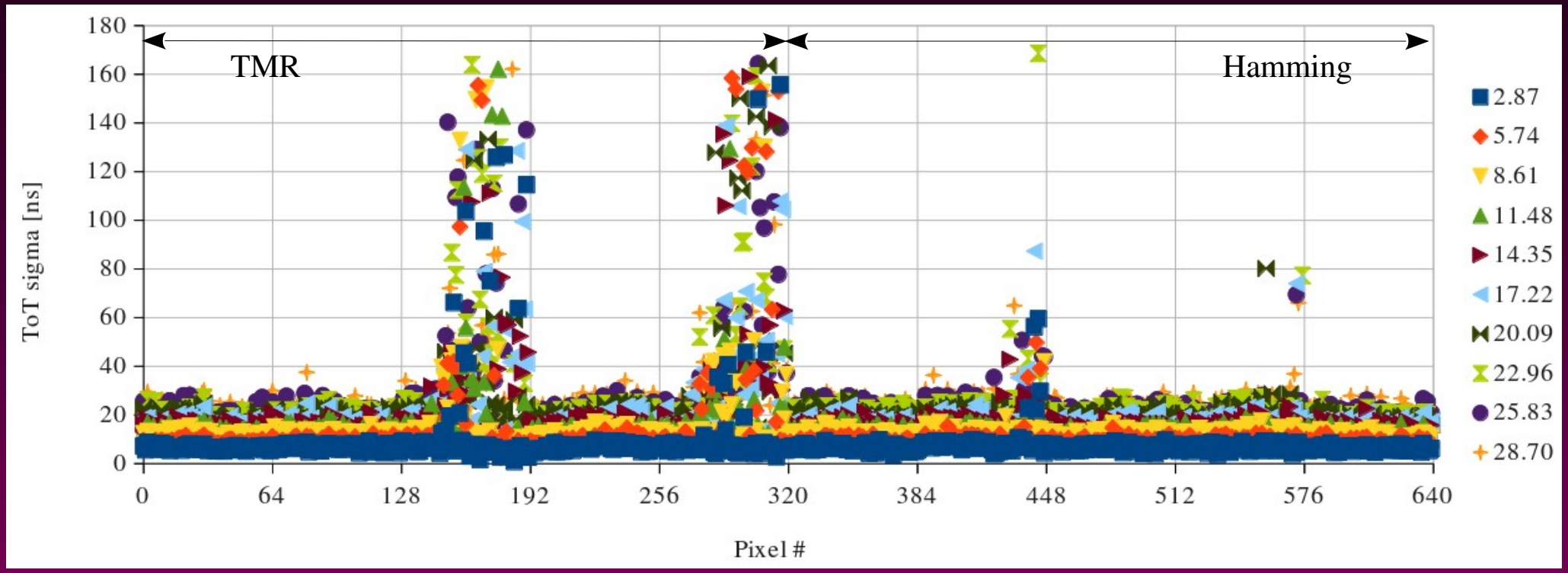




Baseline average value : 727 mV

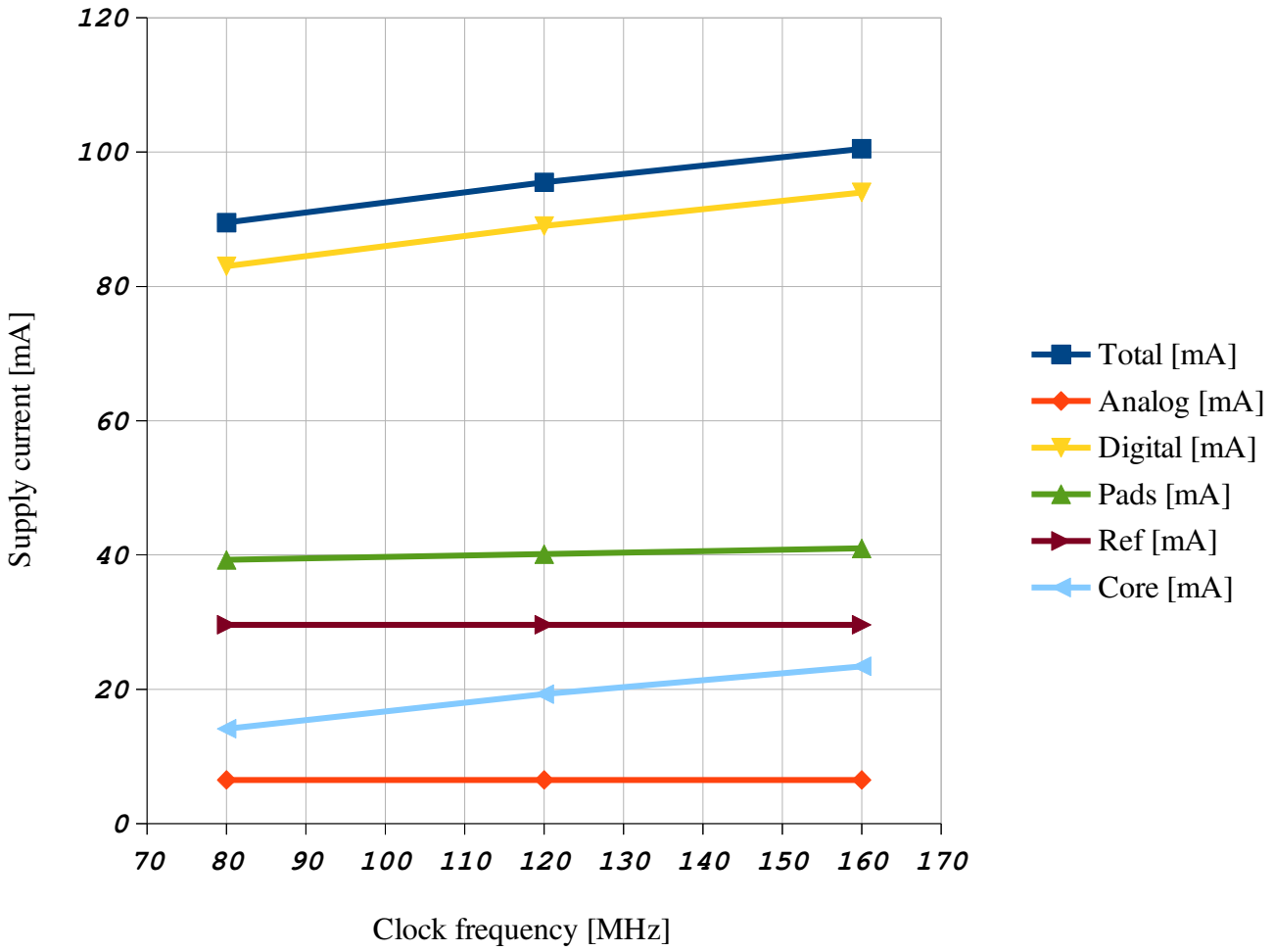
Baseline sigma : 0.73 mV

ToT sigma



Still some issues on the transmission of the data from the last pixels of the column
Larger spread of the ToT (LSB's '0' preferred over '1')
Increasing the power supply (from 1.2 V to 1.5 V) reduces the problem
TMR slower than Hamming

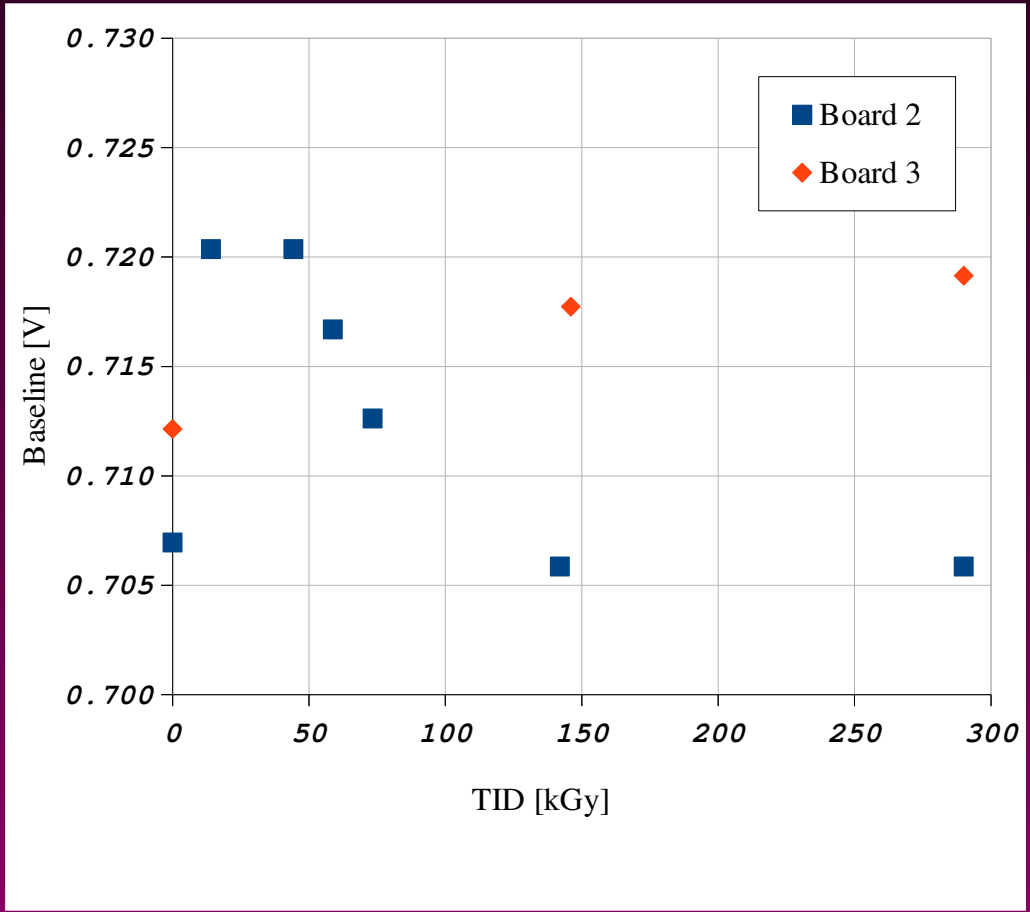
Supply current

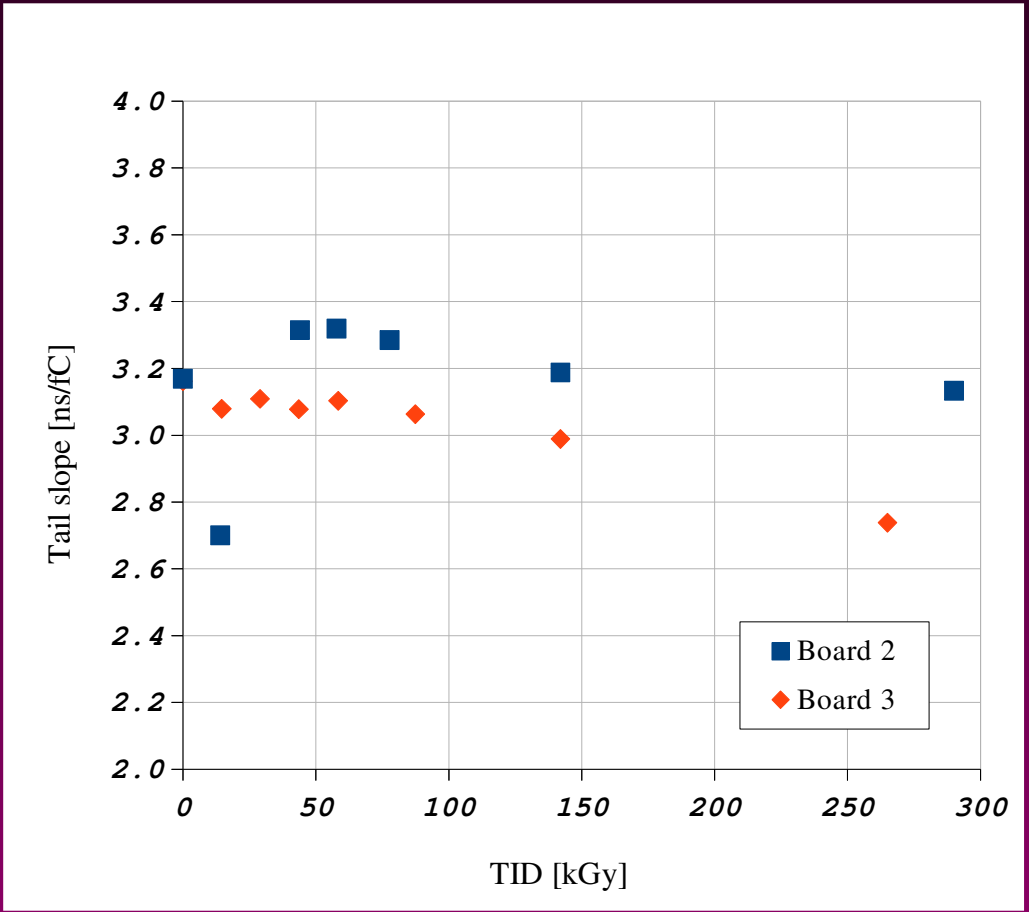


Estimated power density for the full size version :

523 mW/cm^2 @ 80 MHz
666 mW/cm^2 @ 120 MHz
725 mW/cm^2 @ 160 MHz

TID measurements baseline – tail slope





TID measurements noise

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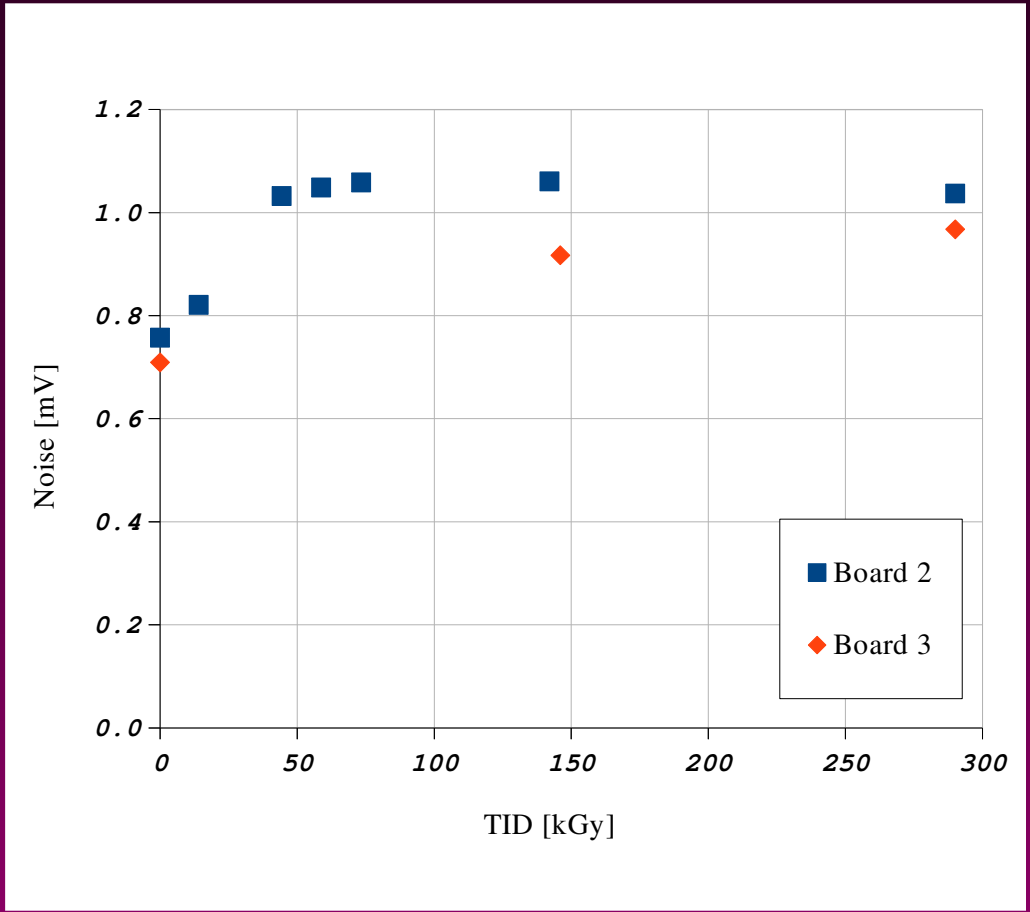
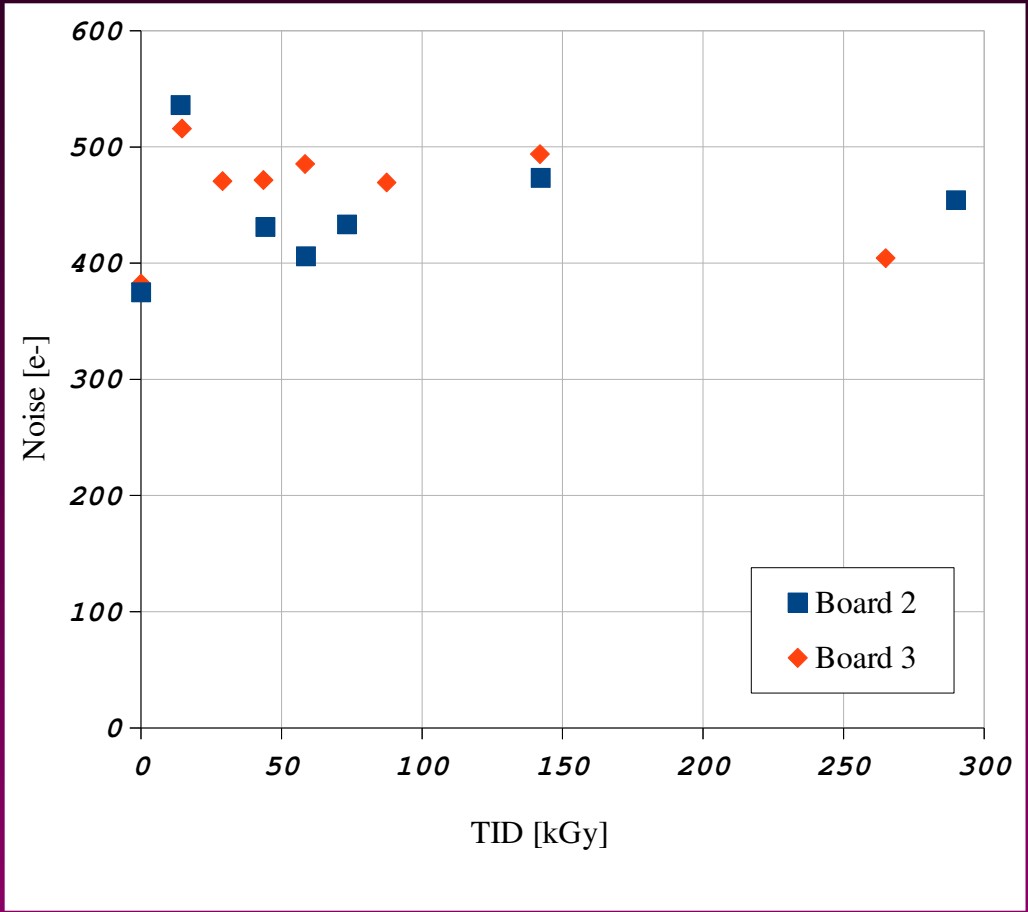
S-curve sigma

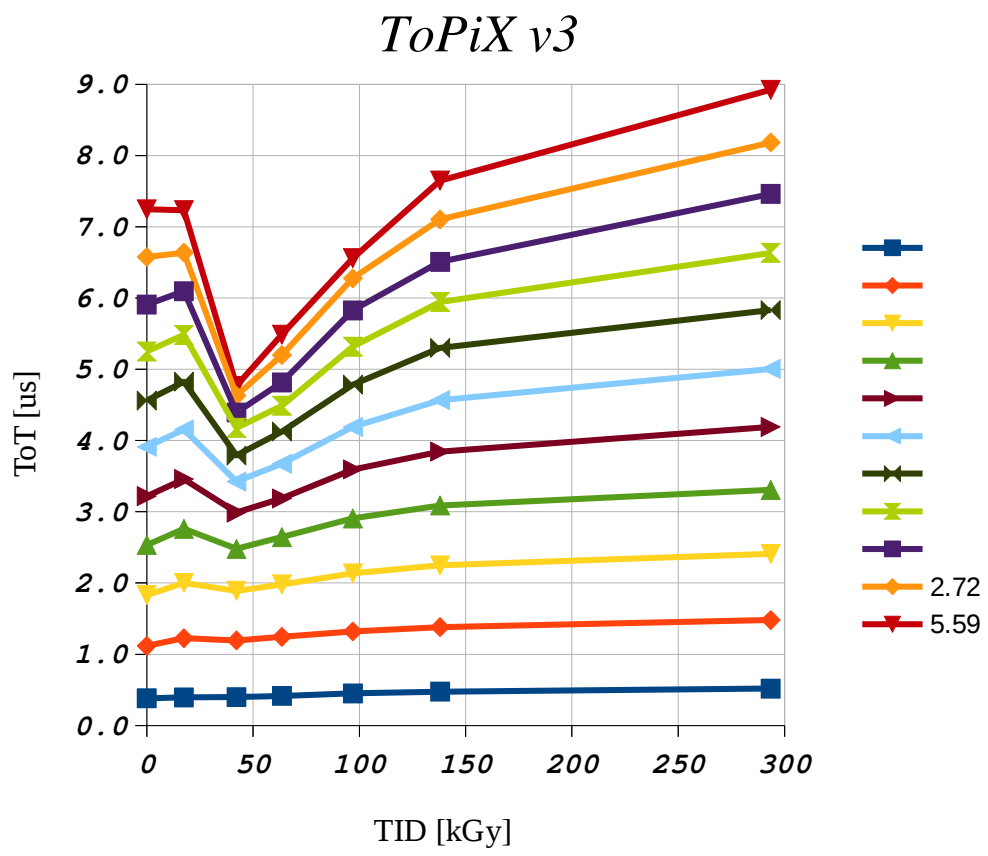


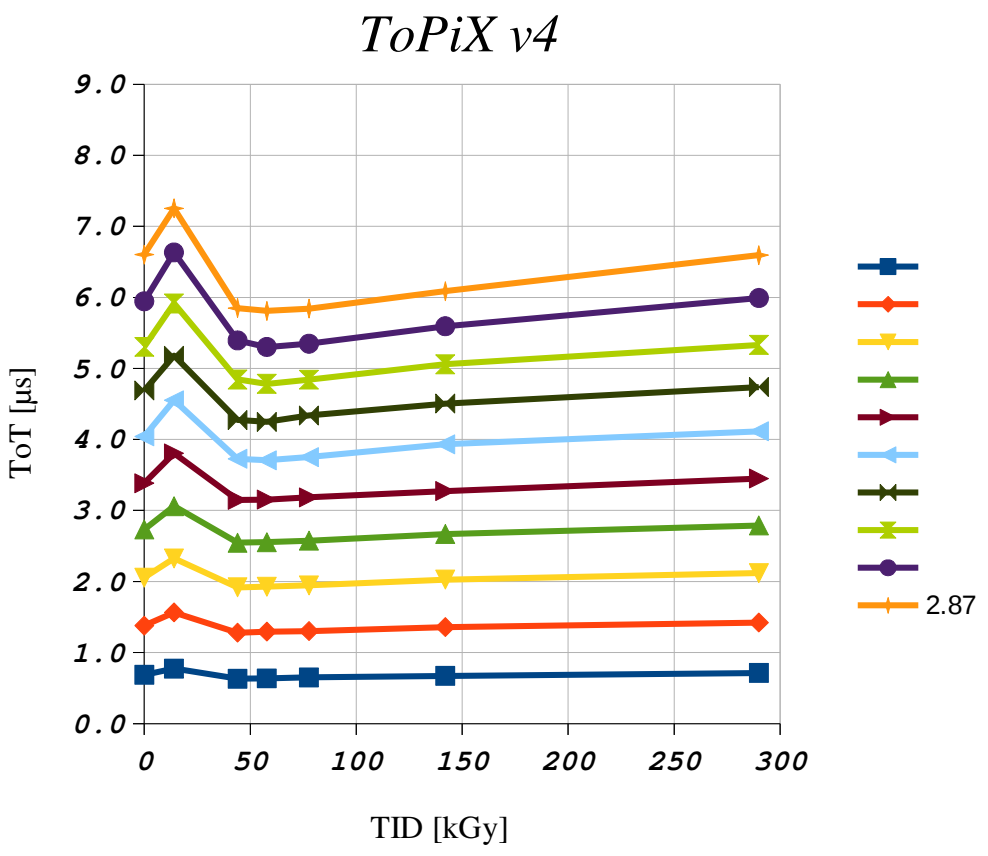
ToT noise



TID measurements ToT

Sezione di Torino





SEU test (preliminary)

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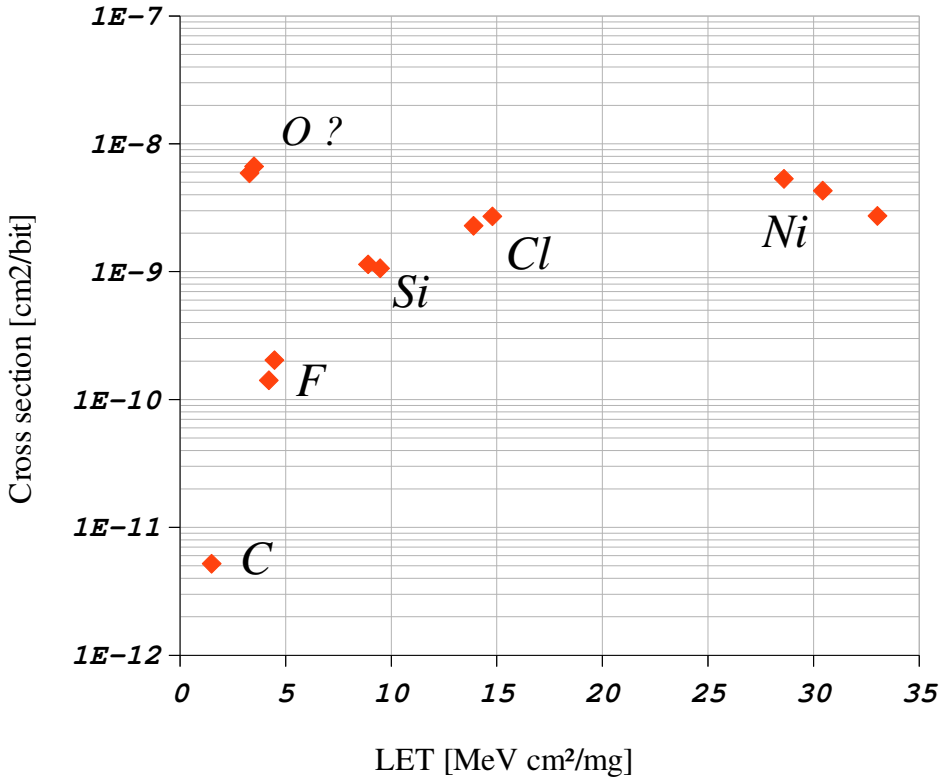
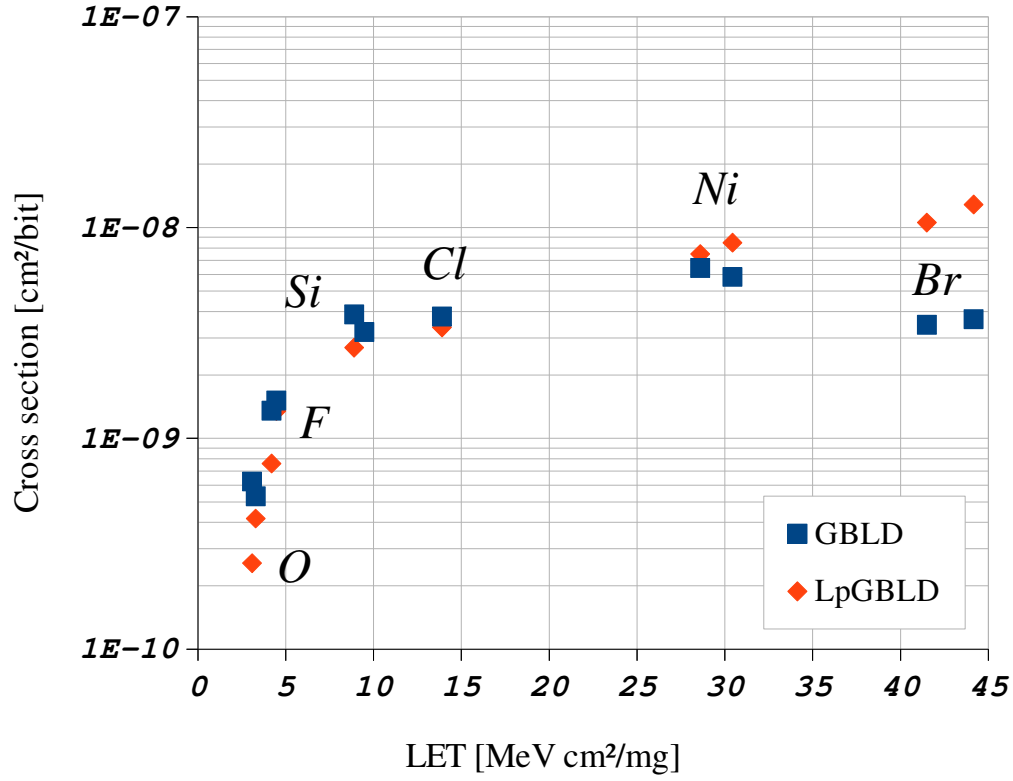


ToPiX pixel configuration registers



GBLD configuration registers

Conclusions

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- The final prototype of the readout ASIC for the PANDA MVD pixel detector has been designed and tested.
- Analogue performances satisfy the requirements.
- Correct operation @ 160 MHz has been proven, albeit column data readout is at the limit – some margin has to be added.
- TID test just completed, v3 problems look solved.
- SEU tests performed, data analysis ongoing.
- Prototypes have been sent for bump-bonding with the detector – beam test foreseen for October 2014 in Jülich.
- Full size ToPiX submission foreseen for 4th quarter 2015.

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Backup slides

Other features

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Output frequency	*160 Mb/s*	*320 Mb/s*
Time stamp counter frequency	*160 MHz*	*80 MHz*
Time stamp mode	*Binary*	*Gray*
Idle packet	*off*	*on*
Analog timeout	*off*	*on*
Detector type	*n-type*	*p-type*
SLVS current control	*0000 (max)*	*1111 (off)*
Driver pre-emphasis	*off*	*on*

ToPiX v3 layout

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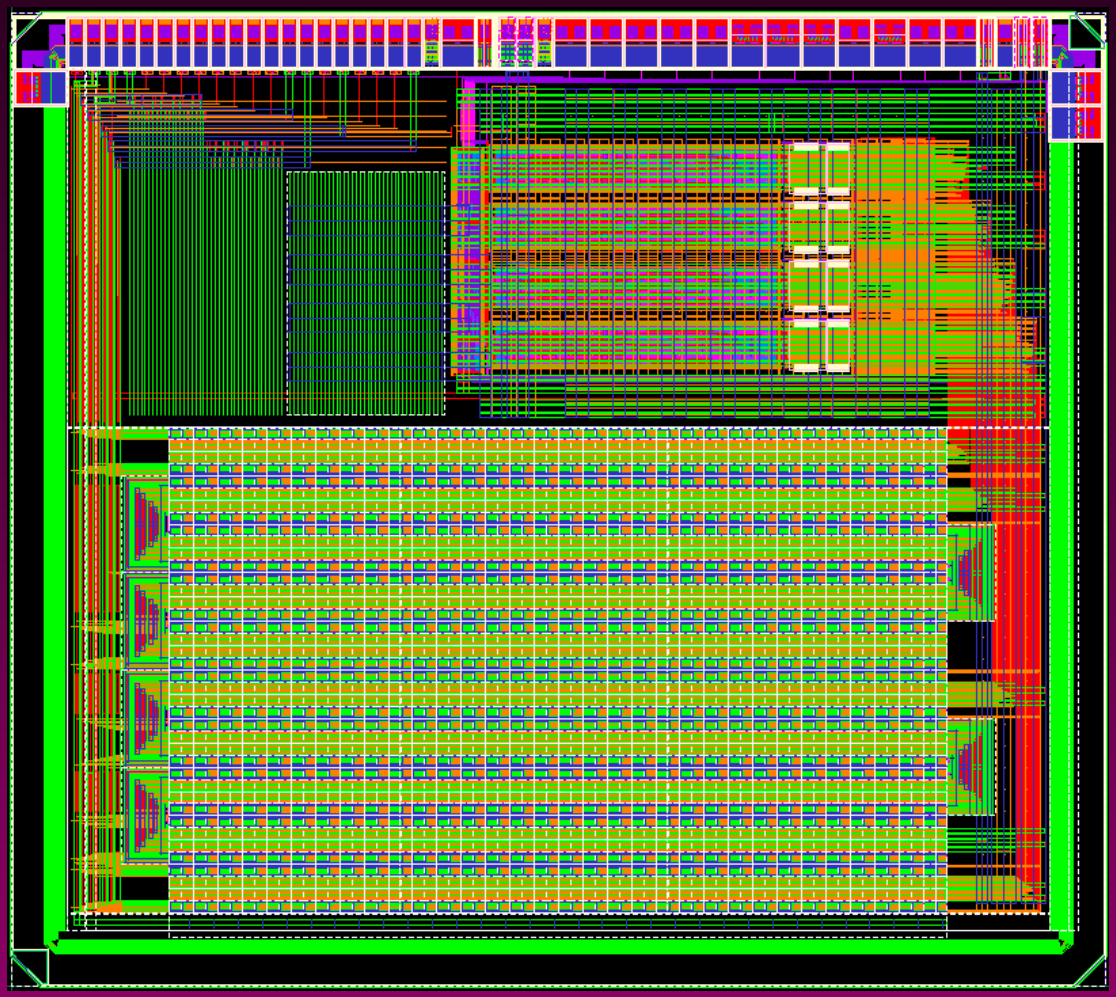

- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

Gianni Mazza