Single-event upset tests of the readout electronics for the pixel detectors of the PANDA experiment

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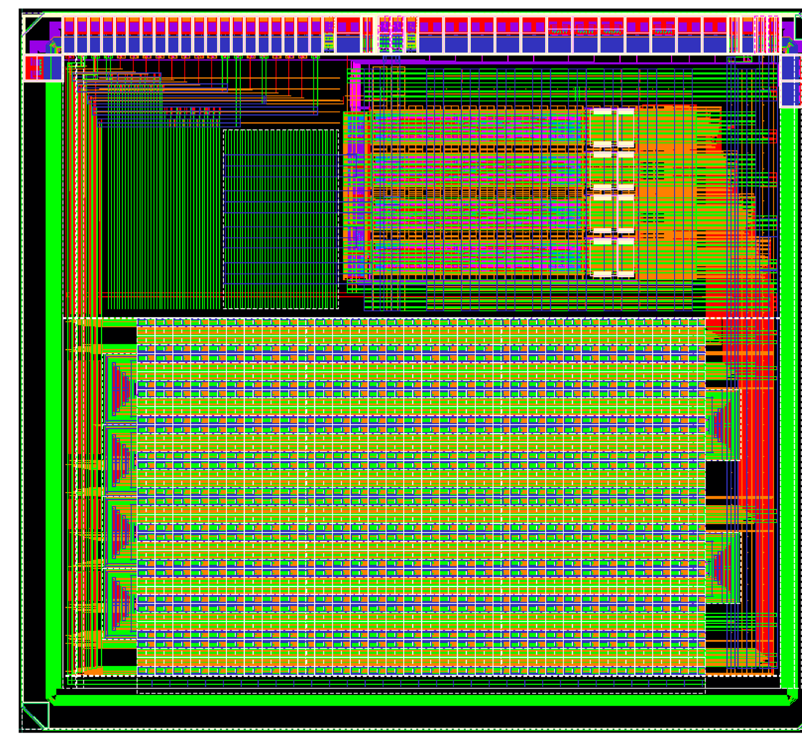
Abstract :The Silicon Pixel Detector (SPD) of the PANDA experiment is the closest one to the interaction point and therefore the sensor and its electronics are the most exposed to radiation. The Total Ionizing Dose (TID) issue has been addressed by the use of a deep-submicron technology (CMOS 0.13 μm) for the readout ASICs. While these technology are very effective in reducing radiation induced oxide damage, they are also more sensitive to Single Event Upset (SEU) effects due to their extremely reduced dimensions. This problem has to be addressed at the circuit level and generally leads to an area penalty. Several techniques have been proposed in literature with different trade-off between level of protection and cell size.

A subset of these techniques has been implemented in the prototypes of the PANDA SPD ToPiX readout ASIC, ranging from DICE cells to triple redundancy. The two prototypes have been tested with several ions at the INFN-LNL facility in order to measure the SEU cross section.

Comparative results of the SEU test will be shown, together with an analysis of the SEU tolerance of the various protection schemes and future plans for the SEU protection strategy which will be implemented in the next ToPiX prototype.

ToPiX

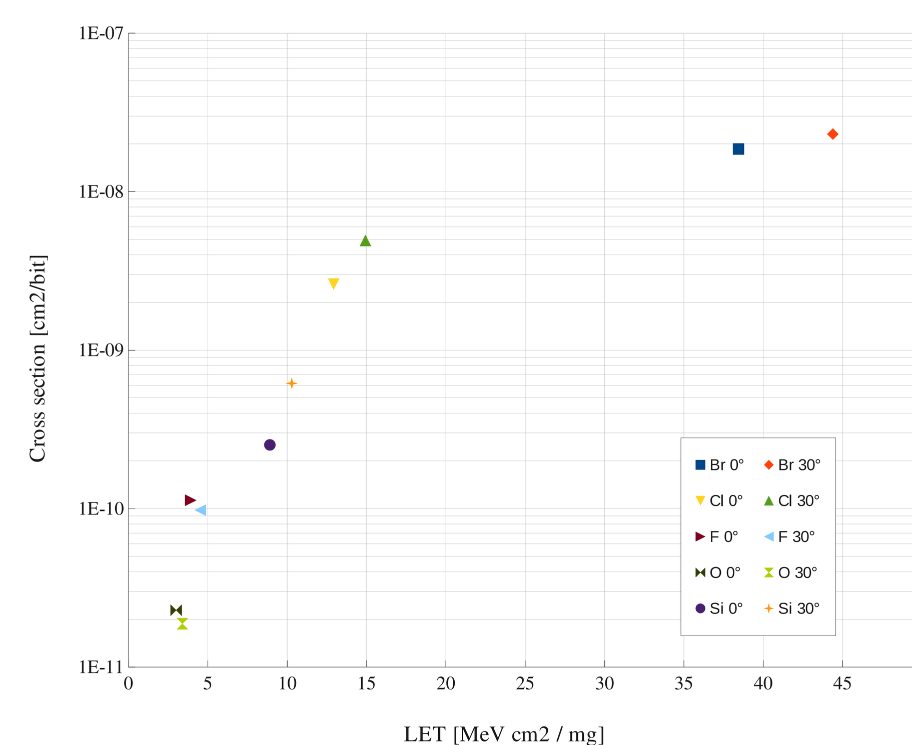


- Die size : 4.5 × 4 mm^2
- Technology : CMOS 0.13 μm
- Single 1.2 V power supply
- Bump bonding pads
- 2 × 2 × 128 cells columns
- 2 × 2 × 32 cells columns
- 32 cells EoC FIFO
- SEU protected logic via TMR (pixel cell) or Hamming encoding (EoC)
- Serial data output
- SLVS I/O

SEU protection circuits used for the ToPiX prototypes :

- Dual Interlocked CEll cell : to change the state of a latch two nodes have to be changed. Very effective in old technologies, probability to have more than one node affected is not negligible.
- Hamming encoding : uses Hamming Single Error Correction (SEC) encoding to detect and correct an error.
- Triple redundancy : all memory cells are triplicated. Actual output is decided by a majority voter.
- Triple redundancy with self correction.

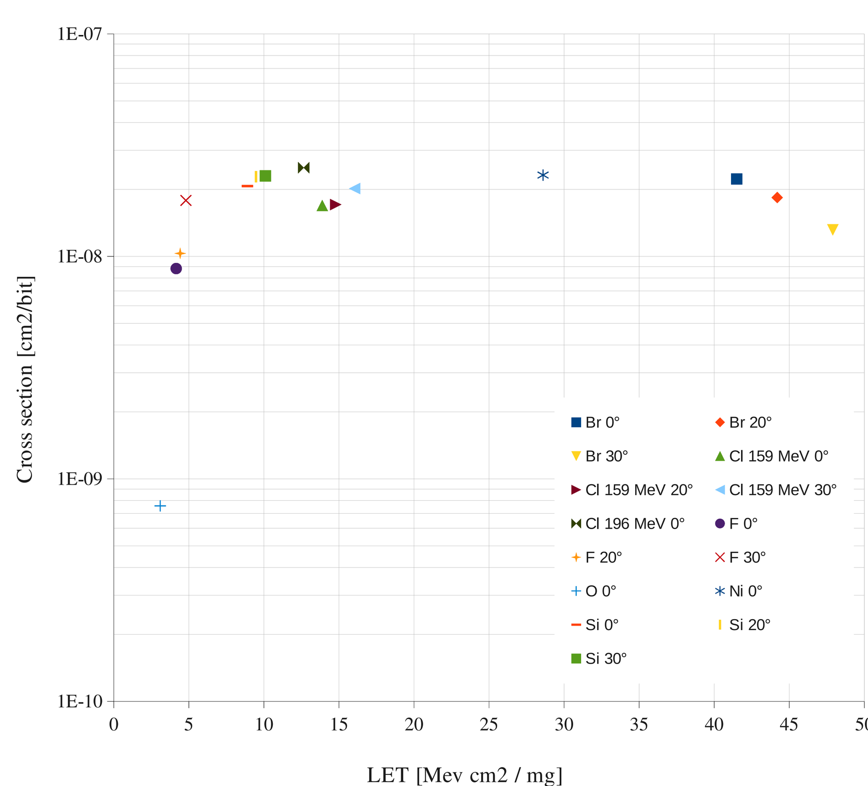
Cross section per bit for the ToPiX v2 configuration register



- 640 × 12 bits latch-based register
- DICE cell protection scheme
- cell area : 5 × 6 μm^2
- LM metal stack

Ion	Angle	E_{INC} [MeV]
^{16}O	0° 30°	101
^{19}F	0° 30°	111
^{28}Si	0° 30°	146
^{35}Cl	0° 30°	159
^{79}Br	0° 30°	215

Cross section per bit for the ToPiX v3 configuration register

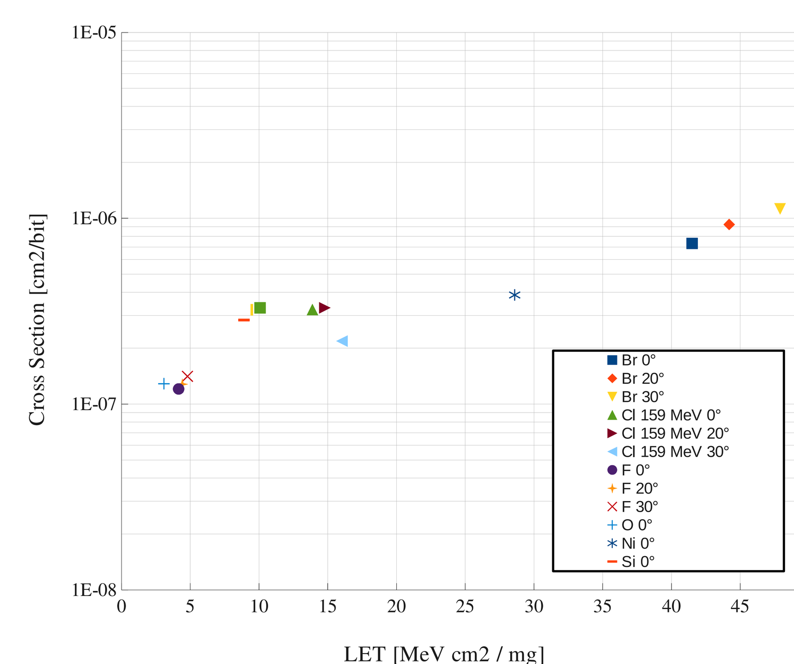


- 640 × 8 bits latch based register
- TMR cell protection scheme with asynchronous error correction
- cell area : 10.2 × 14.4 μm^2

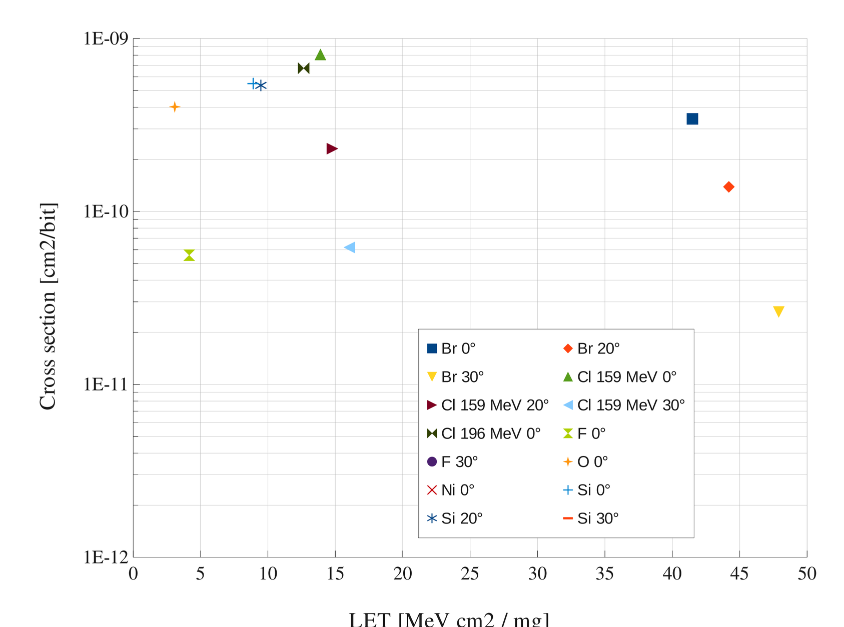
Ion	Angles	E_{INC} [MeV]
^{16}O	0°	101
^{19}F	0° 20° 30°	111
^{28}Si	0° 20° 30°	146
^{28}Ni	0°	223
^{35}Cl	0° 20° 30°	159
^{35}Cl	0° 20°	197
^{79}Br	0° 20° 30°	264

Cross section per bit for the ToPiX v3 FIFO register

- 38 × 32 × 4 bits DFF based registers
- Hamming encoding error protection scheme
- DM metal stack

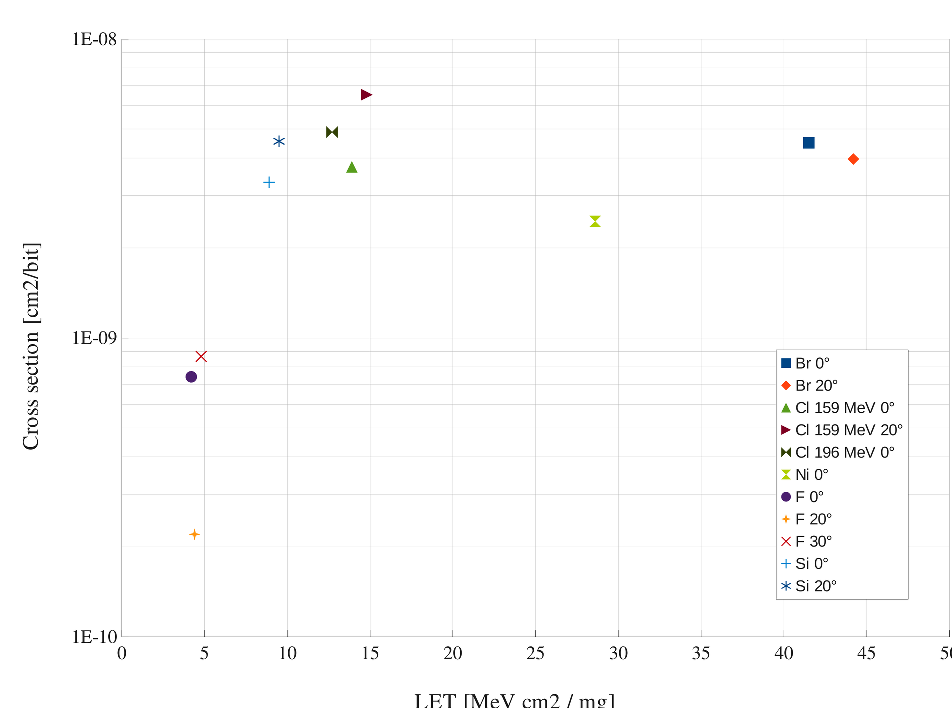


Errors detected and corrected



Errors not detected

Cross section for the GBLD v4 TMR protected registers



- 7 × 8 bits DFF based register
- TMR cell protection scheme with asynchronous error correction
- all control signals are duplicated

It should be noted that part of the logic was not SEU protected since the synthesis tool removed the TMR. However, the registers were TMR protected.

Conclusions and outlook

- Tests on various SEU protection schemes have been performed
- A significant probability of multiple node change has been observed, expecially for the pixel cell registers where the small space available for the circuitry led to a compact latch design
- Differences has been observed between the two metal stack options of the same technolgy, due to the different metal thickness
- A tests with the same circuit designed in the two metal stack is foreseen in November

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