A custom pixel detector for the PANDA experiment

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Overview

introduction – standard hybrid technology

epitaxial silicon devices - results

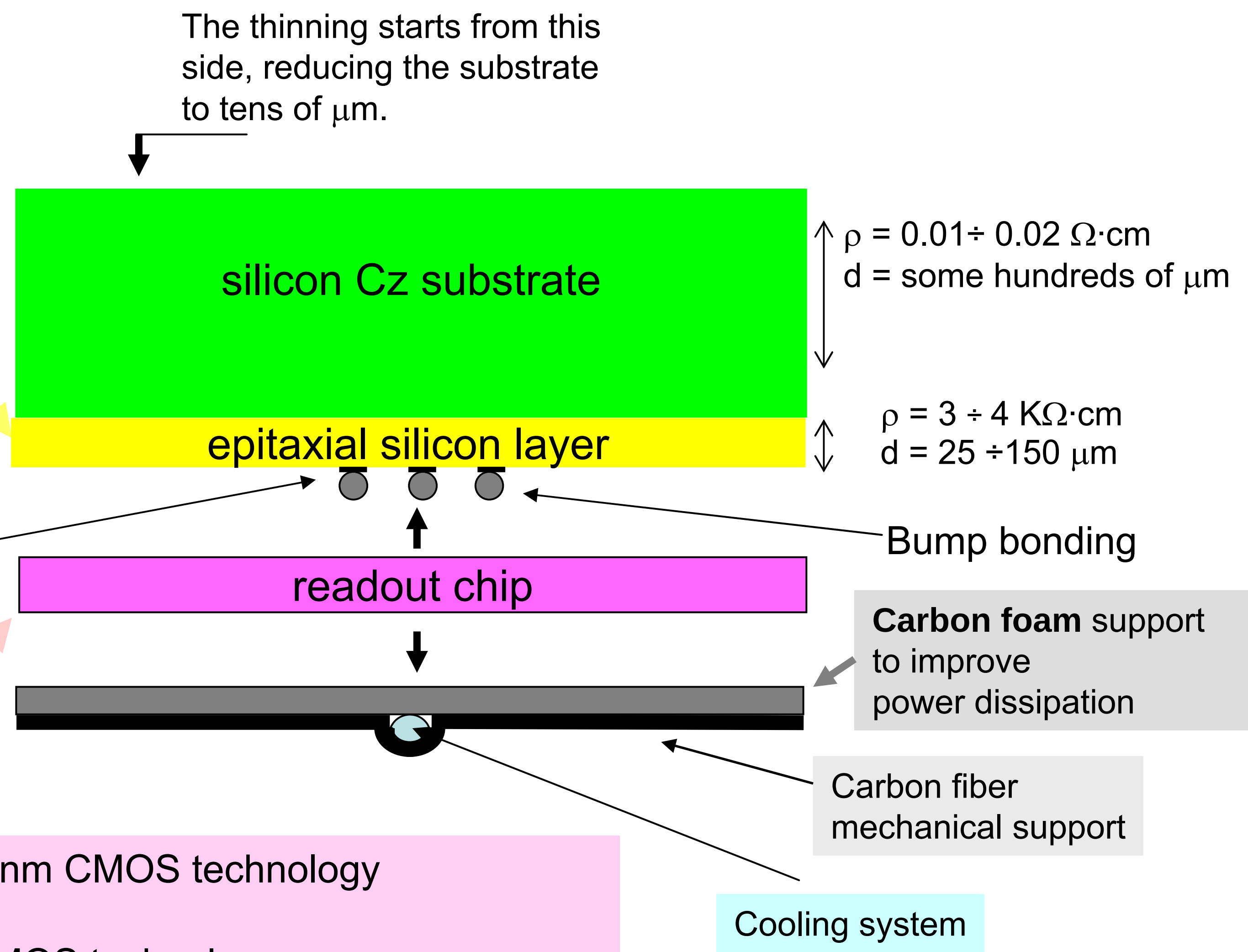
pixel readout prototype - results

conclusion

Standard hybrid technology

THIN PIXEL SENSORS (< 150 μm) realized with EPITAXIAL SILICON material.
(At LHC experiment Si sensors 200 μm thick. At RD50 epitaxial silicon material only for diodes)

Several processes for defining geometry and for obtaining pixel sensors are made on this side



ASIC developed by the 130 nm CMOS technology with triggerless readout.
Up to now only in 250 nm CMOS technology (see LHC experiment with trigger)

Epitaxial silicon devices

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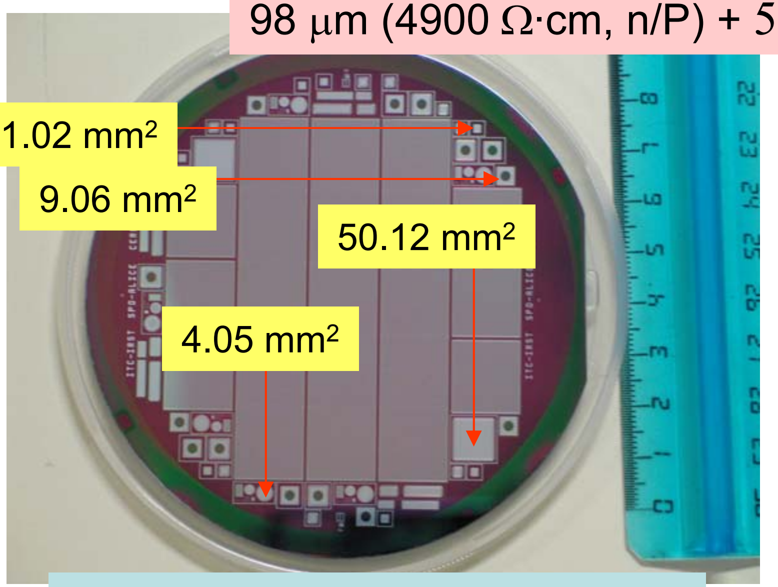
Diodes and single chip sensor from epi-wafers

49 μm (4060 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 100 μm
74 μm (4570 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 120 μm
98 μm (4900 Ω·cm, n/P) + 500 μm Cz substrate (0.01-0.02 Ω·cm, n^+/Sb) → 150 μm

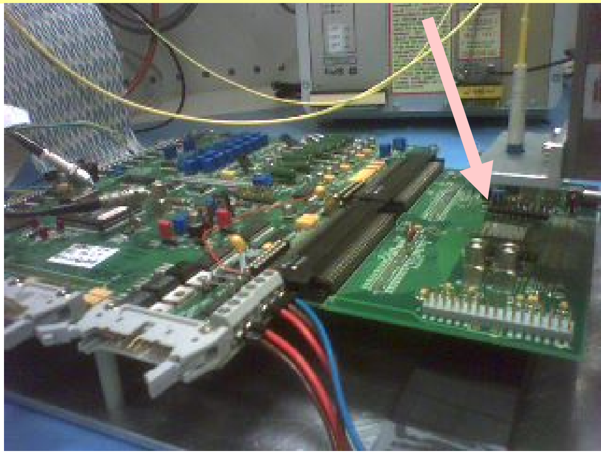


with the ALICE layout at FBK

300 μm FZ wafer have been used as reference

Single chip assembly

- ✓ pixel obtained with the ALICE masks (50 μm x 425 μm)
- ✓ test performed using ALICE pixel readout chip and test system in collaboration with P. Riedler

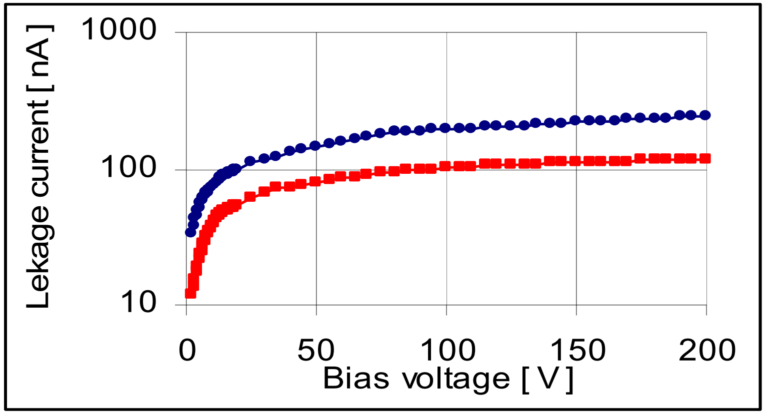


Diodes

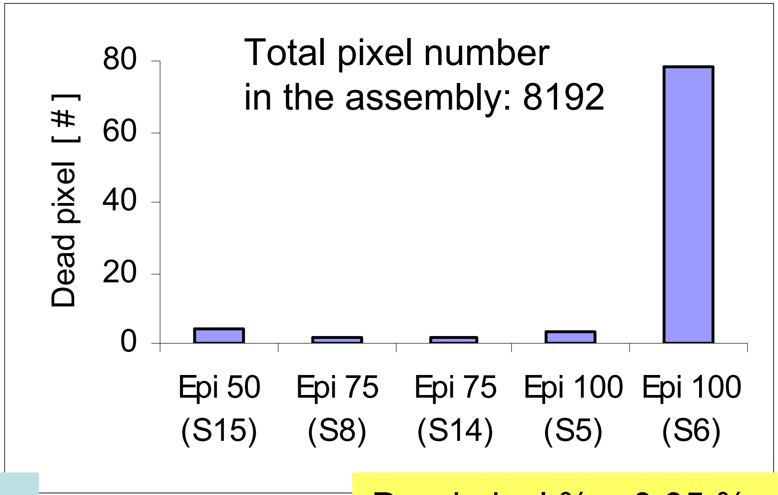
Test of radiation damage with neutrons from Pavia nuclear reactor. Equivalent fluence values on the diodes : 5.13×10^{13}, 1.54×10^{14}, 5.13×10^{14} n(1MeV_{eq})/cm^2 corresponding to 1, 3 and 10 years of PANDA lifetime

Results from thin Si-epitaxial pixel assemblies

Epi 75 and Epi 50

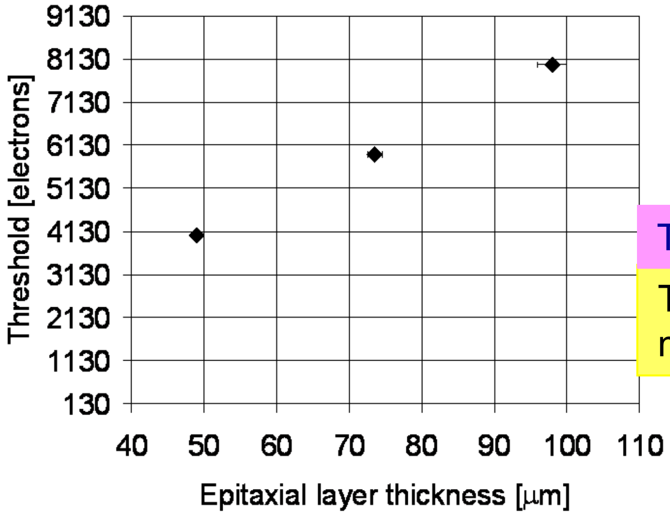


Test performed with a ^{90}Sr source to verify the bump bonding process



NIM A594 (2008) 29–32

Dead pixel % ≤ 0.05 %; ≤ 1% (worst case)



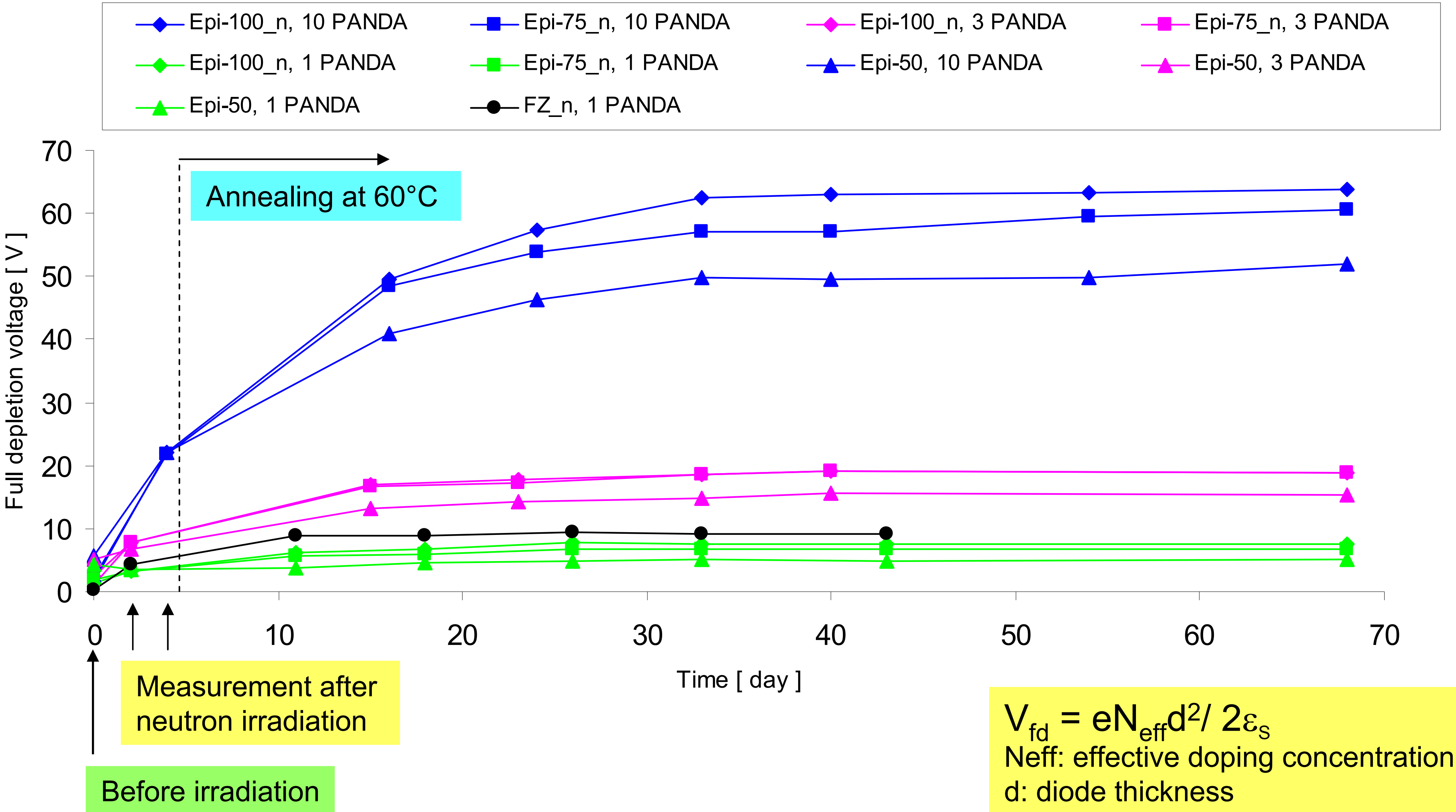
Test performed with a ^{90}Sr source

Threshold values in electrons corresponding to the Landau most probable value for the different epitaxial layer thicknesses

Results from radiation damage test:

full depletion voltage normalized to epi50

Equivalent fluence values on the diodes : 5.13×10^{13} 1.54×10^{14} 5.13×10^{14} $n(1MeV_{eq})/cm^2$
corresponding to 1 3 and 10 years of PANDA lifetime



$V_{fd} = eN_{eff}d^2/ 2\varepsilon_S$

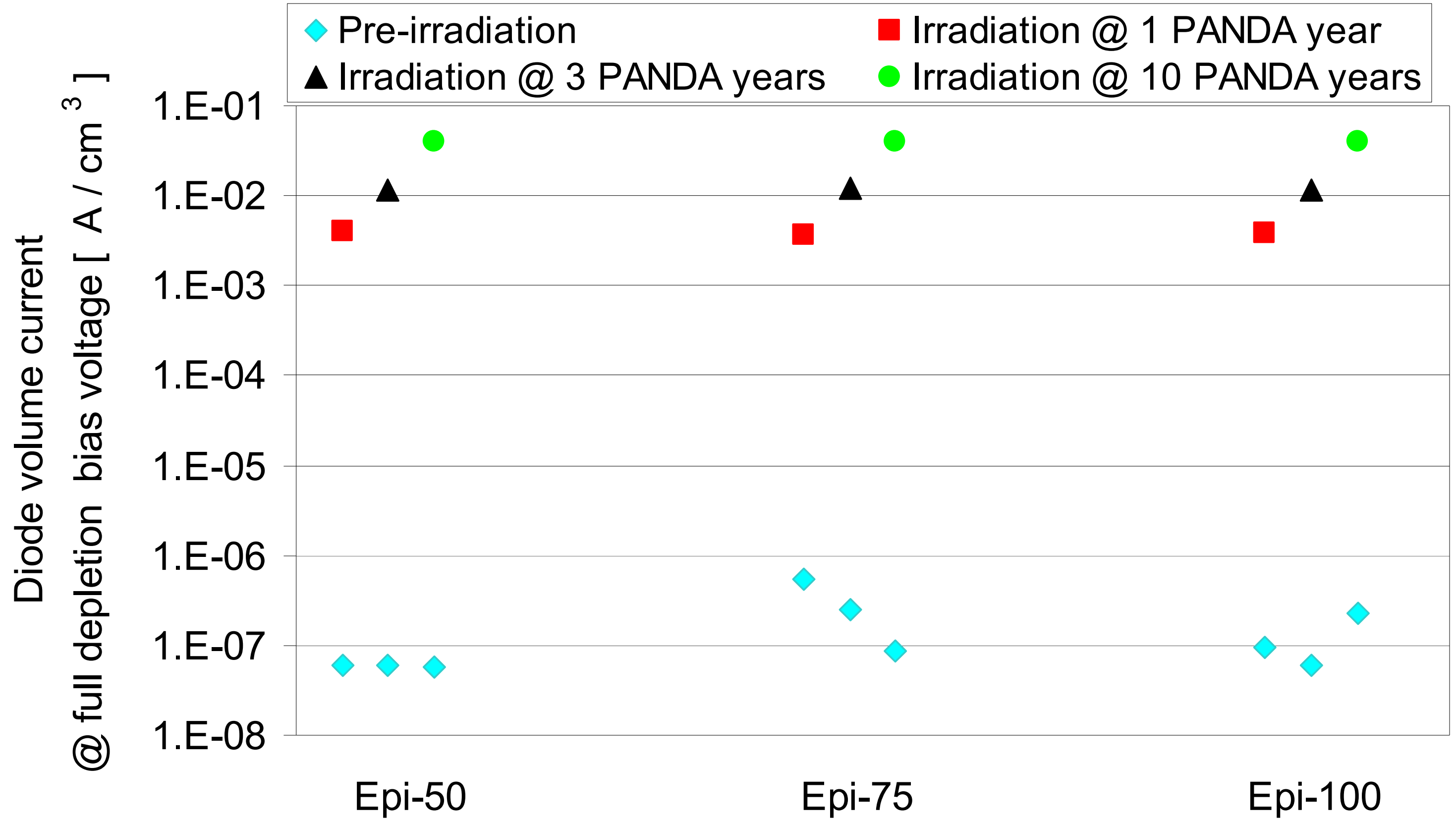
Neff: effective doping concentration

d: diode thickness

ε_S : silicon dielectric constant

Results from radiation damage test:
the radiation damage constant

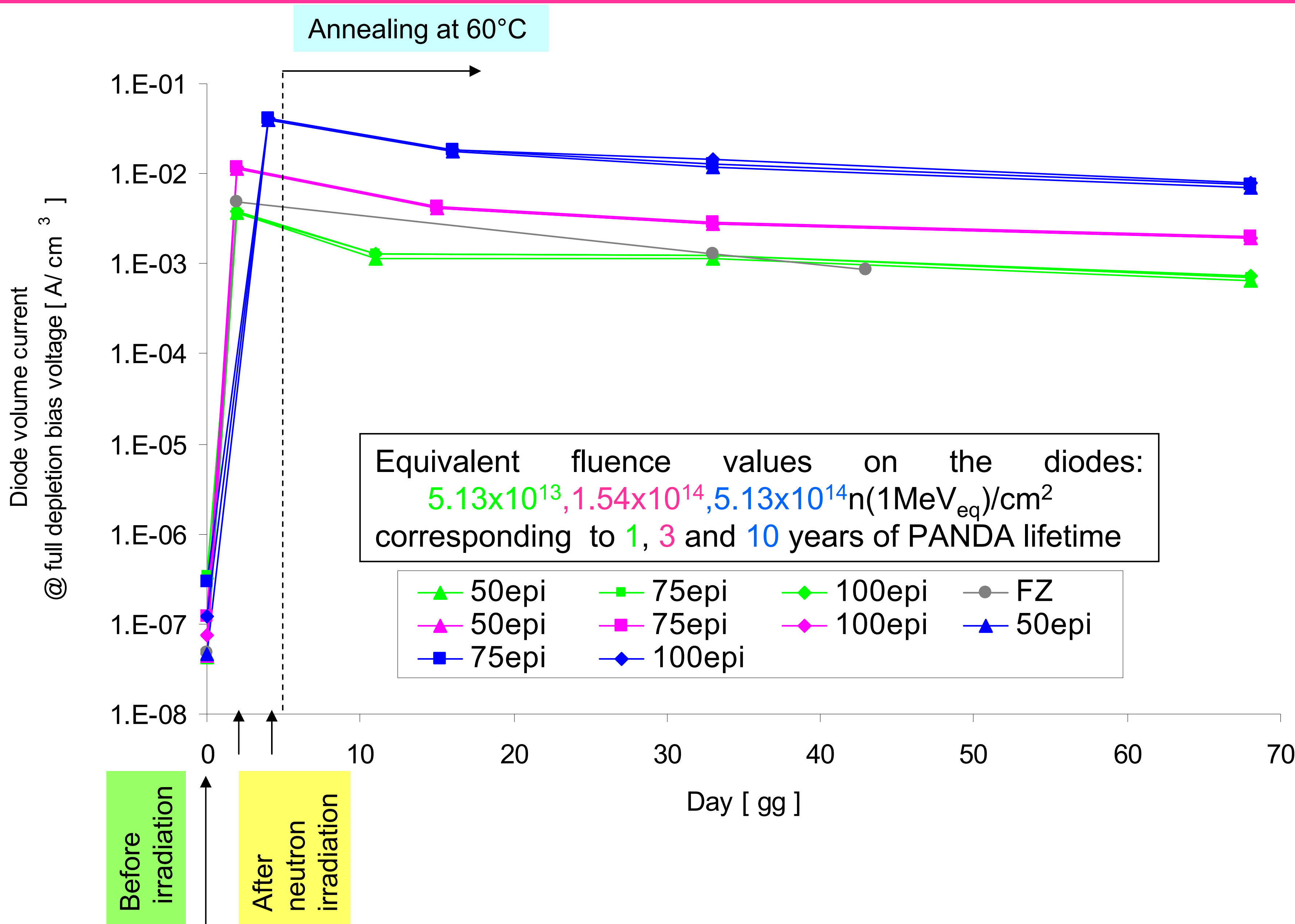
Equivalent fluence values on the diodes : 5.13×10^{13}, 1.54×10^{14}, 5.13×10^{14} $n(1MeV_{eq})/cm^2$ corresponding to 1, 3 and 10 years of PANDA lifetime



The radiation damage constant is
$\alpha = \Delta J/\Phi = 7.6(\pm0.3)\times10^{-17}$ A/cm for all diodes.

Lekage current < 50 nA/pixel (100 μmx100μm size, 100 μm thick)

Results from radiation damage test:
diode volume current @ full depletion voltage



ASIC prototype

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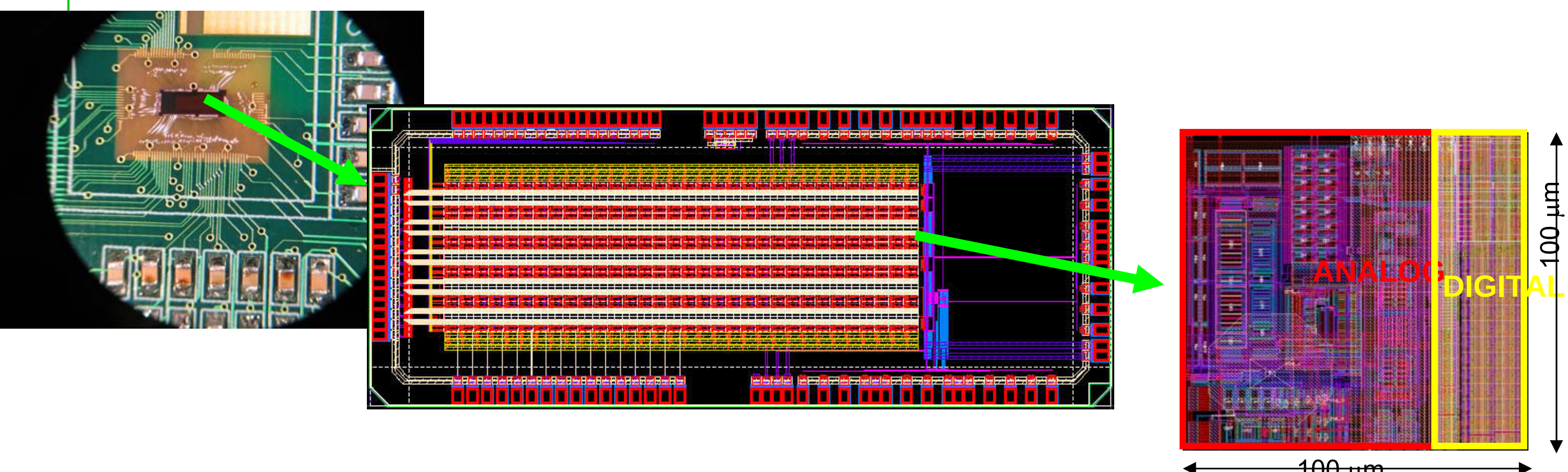
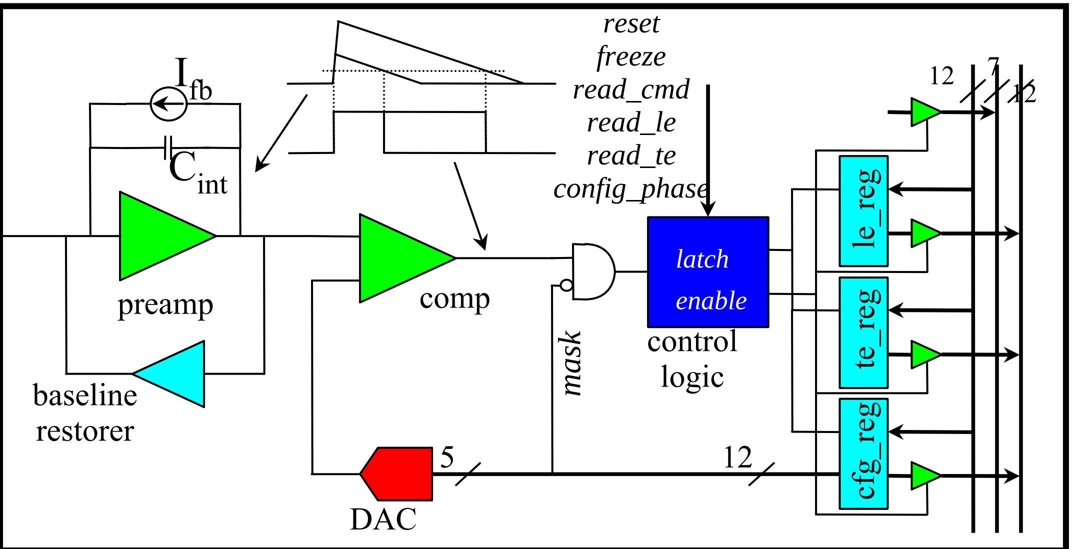
Second pixel readout prototype

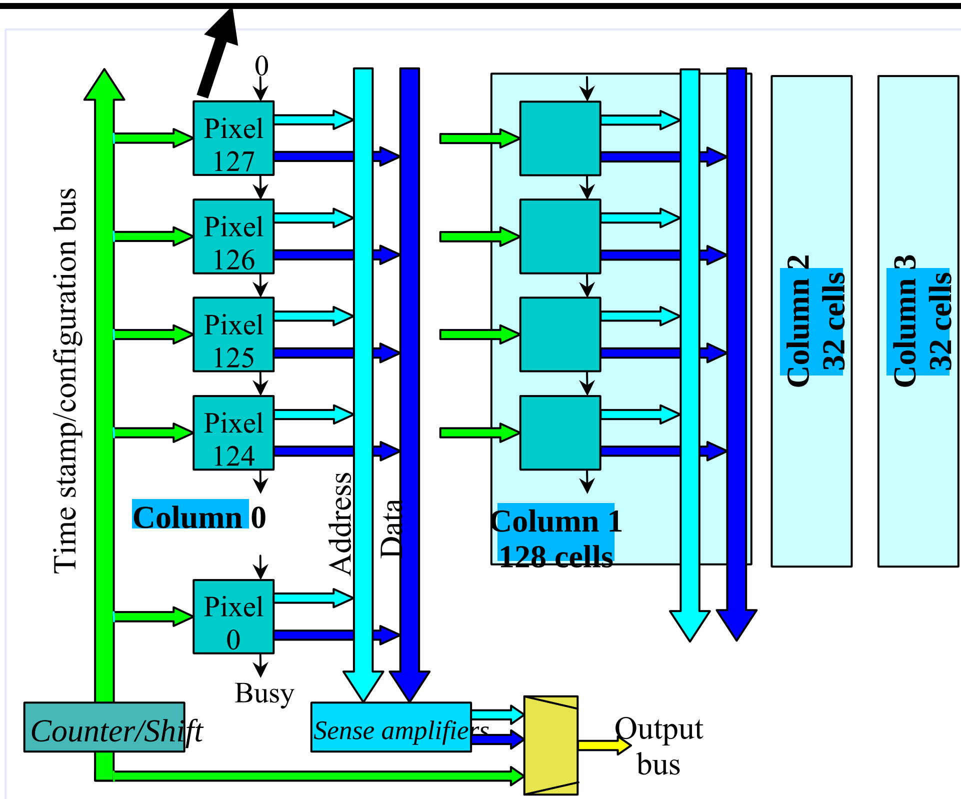
ToPix_2, CMOS 130 nm technology

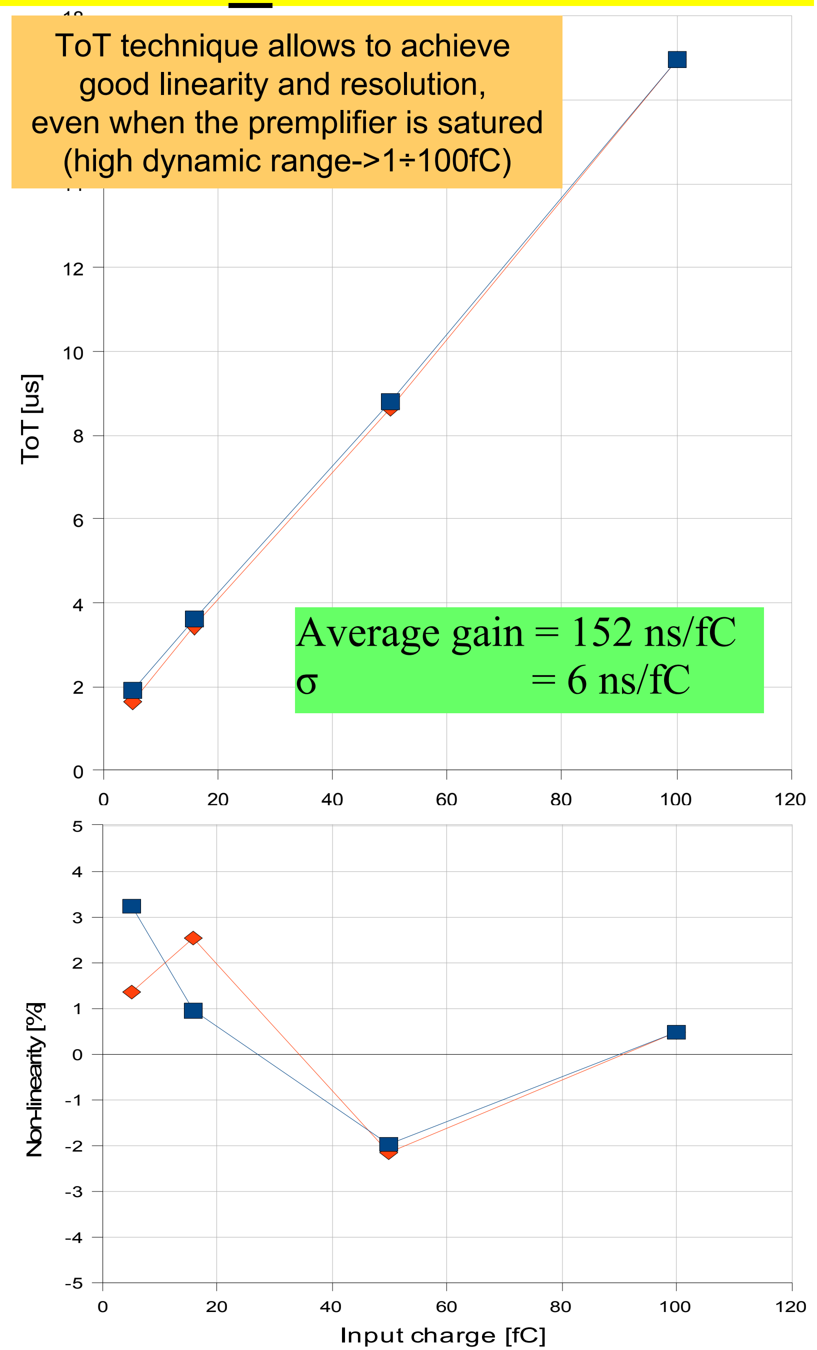
- 5x2 mm^2 area with 4 folded columns with a total of 320 readout cells of 100x100μm^2 size
- analogue + digital circuits (analog power consumption below 12μW @1.2V)
- Time over Threshold technique implemented to obtain a energy loss measurement
- SEU-hardened memory cells (Dice layout)
- absence of enclosed structures to study the radiation tolerance of the 130nm CMOS technology
- inputs for connecting external sensors
- selectable input polarity
- comparator threshold controlled by DAC (5 bits)
- 12 + 12 bits leading and trailing edge, 12 bits configuration registers
- 12 bits bus for time stamp and 12+7 bits output bus for data + address



The architecture of ToPix_2



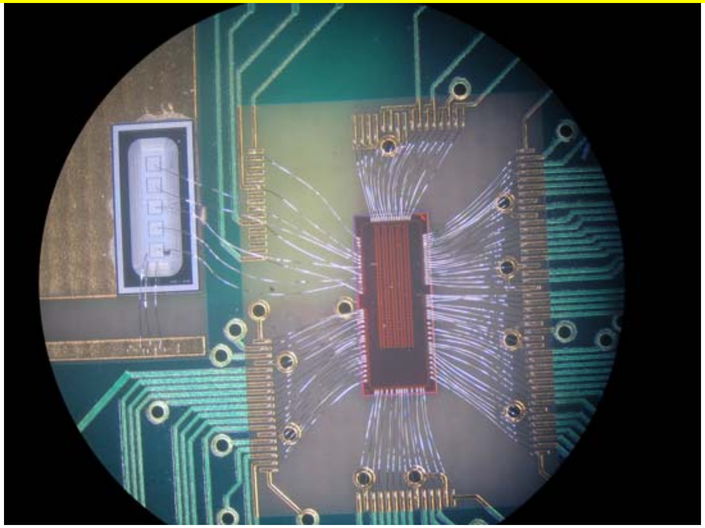




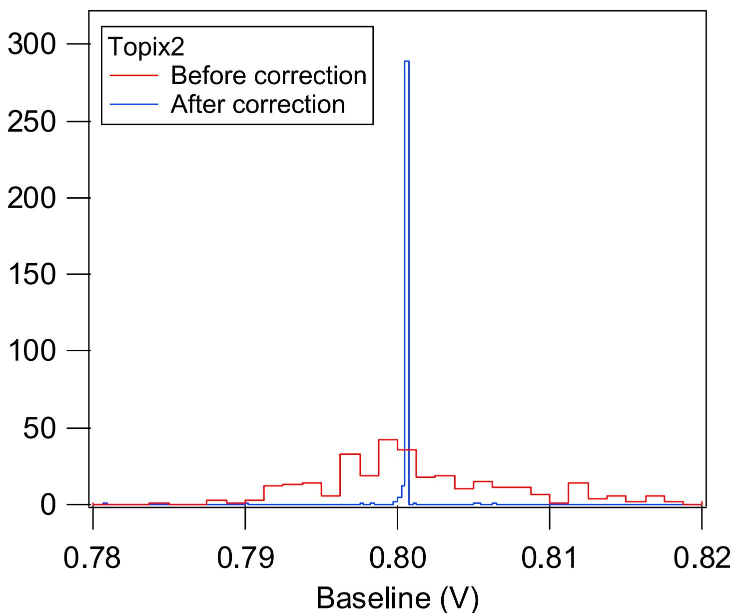
ToT technique allows to achieve good linearity and resolution, even when the premplifier is satured (high dynamic range->1÷100fC)

Average gain = 152 ns/fC
σ = 6 ns/fC

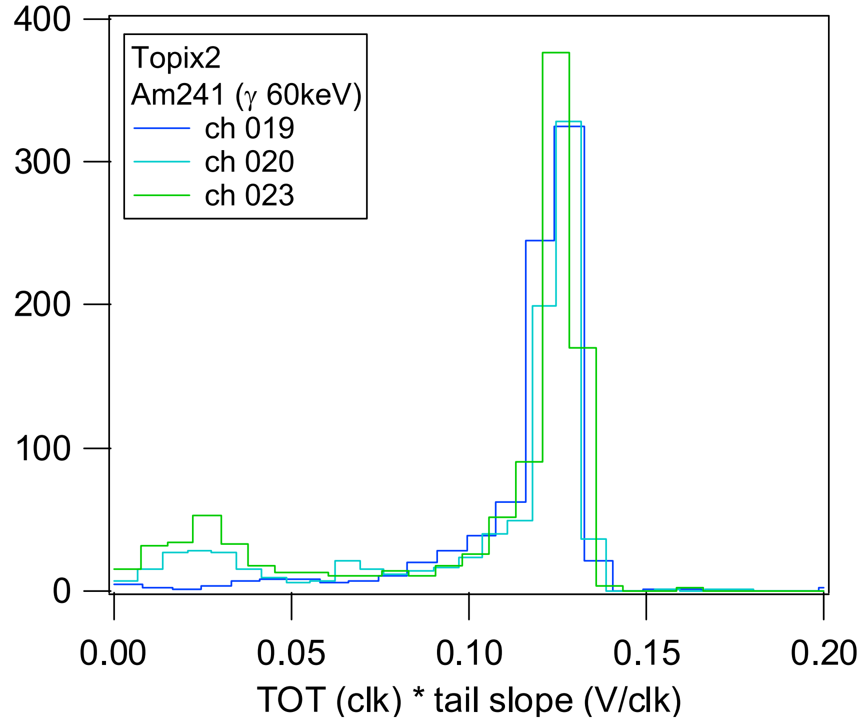
ToPix_2 and sensor



- ToPix_2 - FZ diode (400μm x 400μm, 200 μm thick) connection using wire bonding
- test with gamma rays (60 KeV) from ^{241}Am radioactive source



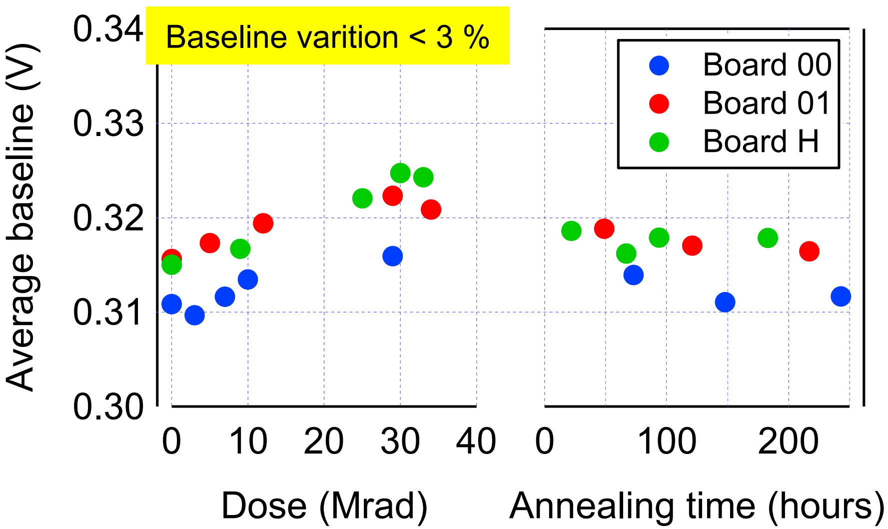
Individual pixel DAC baseline correction

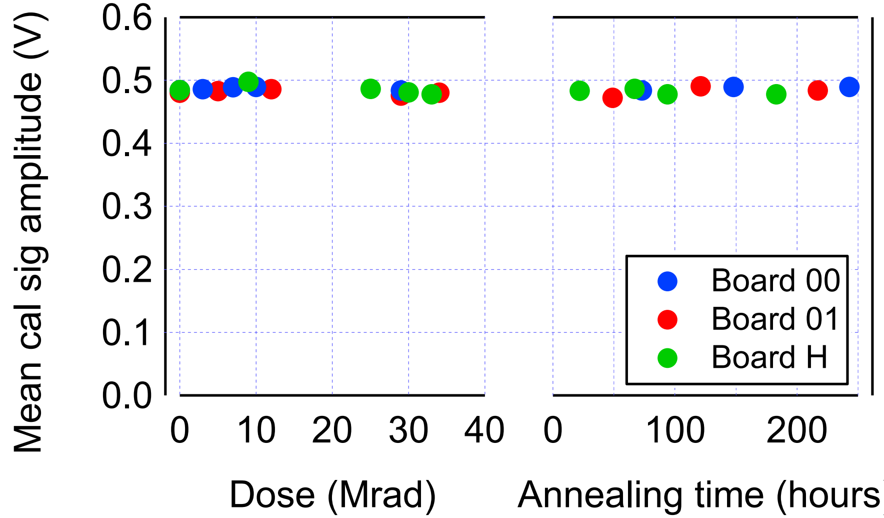


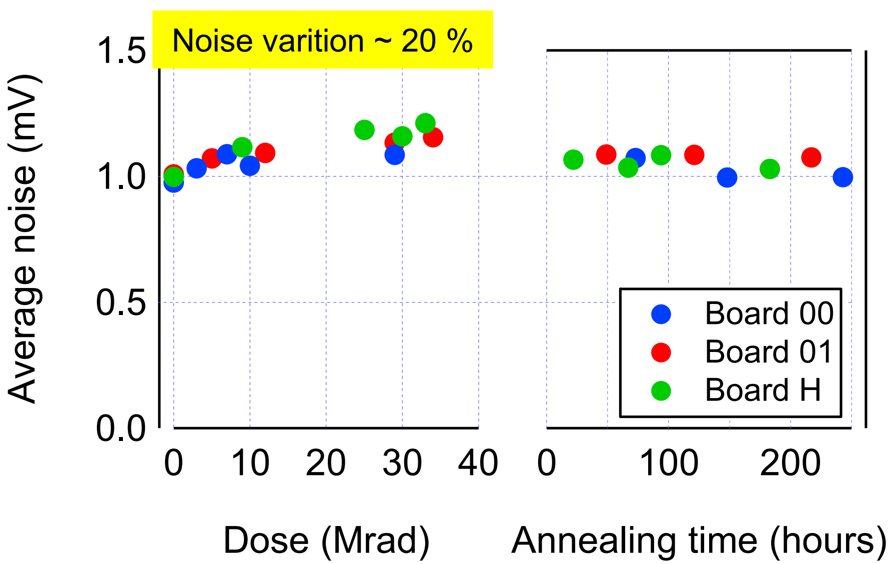
TOT calibration

TID test on ToPix_2

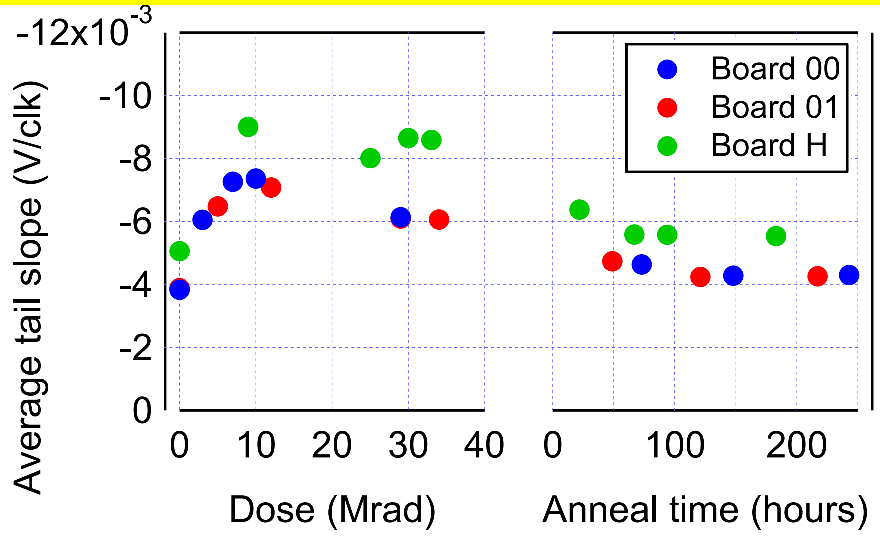
Total Ionizing Dose test with the X ray source at CERN (Thanks to F. Faccio) followed by an annealing phase at 100°C





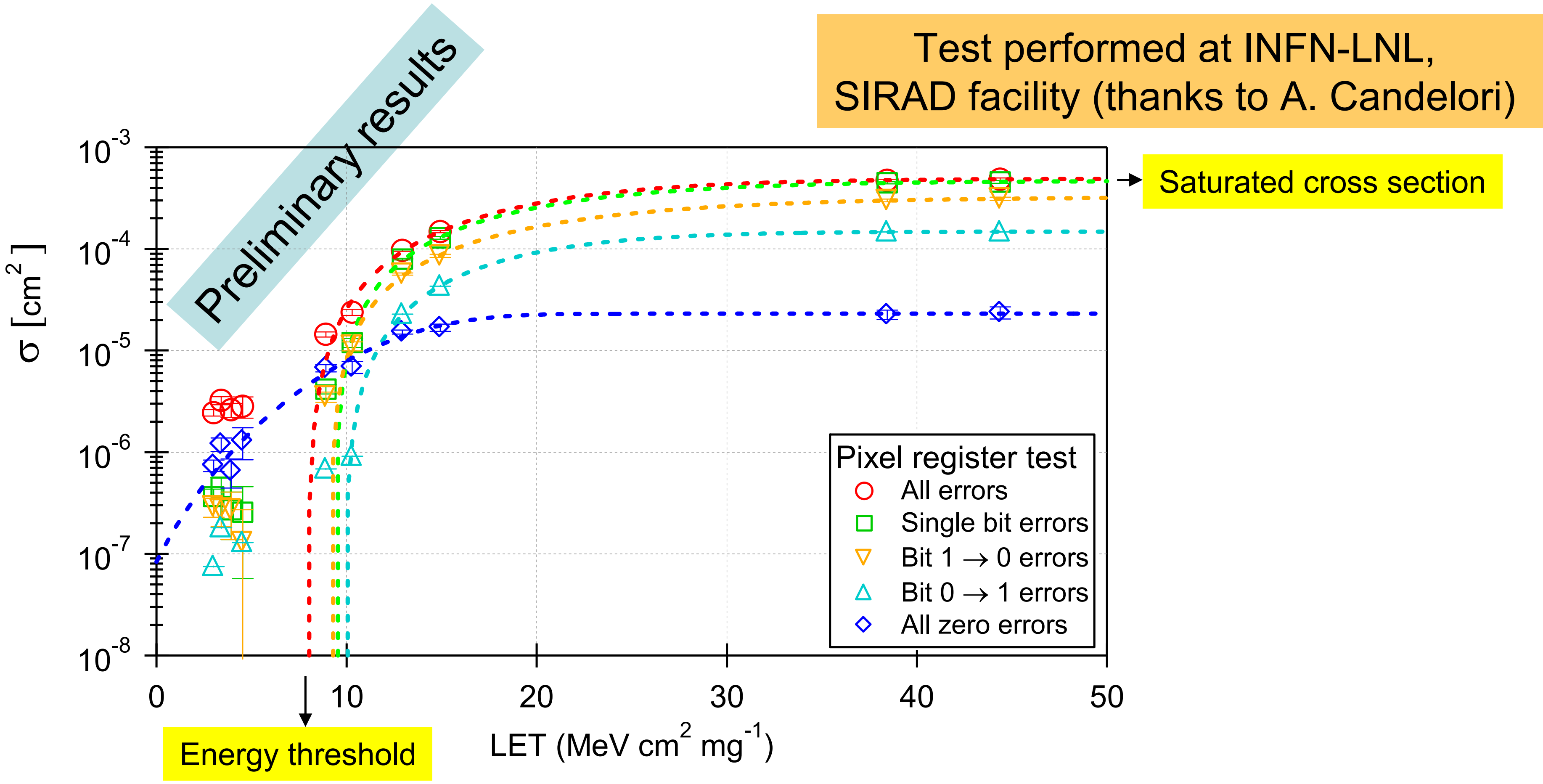


Average tail slope variation ~ 2 times, sigma tail slope ~ 6 times



SEU test on ToPix_2

Test performed at INFN-LNL, SIRAD facility (thanks to A. Candelori)



Conclusions

❖ the use of epitaxial silicon material could be very promising , also in term of radiation damage

❖ the tuning of the epitaxial layer resistivity, taking into account the short and long terms of annealing, has to be investigated for the full depletion voltage optimization

❖ the 130 nm CMOS technology is suitable to develop the pixel readout for:

- ❖ limited power consumption
- ❖ smaller pixel with many functionalities, but
  - ❖ enclosed gate layout is needed for the critical transistors of the discharge circuit
  - ❖ seu hardened cells are needed