Contributions to the PANDA MVD Strip Detector Readout (FAIR-019)

R. Schnell, CANU 2014, Bad Honnef - December 15/16, 2014
The PANDA MVD Strip Detector

- Innermost detector of the PANDA Target Spectrometer
- Located at the crossing of beam pipe and target pipe

- Tracking of charged particles
- Vertex reconstruction for primary and secondary vertices
- Improvement of momentum resolution and PID
The PANDA MVD Strip Detector

- Hybrid silicon pixel sensors
- Double-sided silicon strip sensors
  - 4 barrel layers
    • 2 pixel barrels
    • 2 strip barrels
  - 6 disk layers
    • 4 pixel disks
    • 2 mixed disks
      (inner pixel, outer strips)
The PANDA MVD Strip Detector

- Hybrid silicon pixel sensors
- Double-sided silicon strip sensors
  - 4 barrel layers
    • 2 pixel barrels
    • 2 strip barrels
  - 6 disk layers
    • 4 pixel disks
    • 2 mixed disks
      (inner pixel, outer strips)
  - Requirements
    • low material budget (<10% $X_0$)
    • high radiation tolerance
    • self-triggering readout!
Strip DAQ Chain

Double-Sided Silicon Strip Sensor → Front-End → Data Concentrator → DAQ

- PASTA
- MDC
- GBT MMB CN
Strip DAQ Chain

Double-Sided Silicon Strip Sensor

MDC (Module Data Concentrator ASIC)

GBT

MMB (MVD Multiplexer Board)

Compute Node

SODANET

DAQ

GBTs

R. Schnell, CANU 2014, Bad Honnef - December 15/16, 2014
Strip Detectors

- Barrel sensors
  - rectangular 60x35 mm²
    896+512 strips
  - square 35x35 mm²
    512+512 strips
- 65 µm strip pitch
  → 130 µm readout pitch

- Disk sensors
  - trapezoidal
    58 mm high, 37 mm long side
  - 768+768 strips
  - 15° stereo angle
  - 45 µm strip pitch
  → 90 µm readout pitch
Strip Detectors

- **Barrel sensors**
  - rectangular 60x35 mm²
    - 896+512 strips
  - square 35x35 mm²
    - 512+512 strips
  - 65 µm strip pitch
    → 130 µm readout pitch

- **Disk sensors**
  - trapezoidal
    - 58 mm high, 37 mm long side
    - 768+768 strips
    - 15° stereo angle
    - 45 µm strip pitch
    → 90 µm readout pitch

First Sensor Batches for PANDA ordered by JLU Gießen and IKP Jülich.
PASTA Front-end

- 200,000 channels need to be read out
- **PASTA - PANDA Strip ASIC**
  - Measurement concept inspired by TOFPET architecture
    - ASIC for SiPM readout from EndoTOFPET-US collaboration
    - self-triggering, fully digital back-end
  - Complete redesign of analog stage for strip detectors
  - Time-over-Threshold (ToT) using analog interpolators
    - multiple ToT stages to reduce pile-up
    - low power consumption
    - precise time resolution
  - Joint development of:
    - University Gießen
    - Forschungszentrum Jülich
    - INFN Torino
PASTA Front-end

- Architecture of the chip
  - 2 discriminators for each of the 64 channels
  - 4 time-to-analog converters (TAC) per discriminator

V. Di Pietro  A. Riccardi  A. Goerres

technical advisors: A. Rivetti, M. Rolo
PASTA Front-end

- Dual threshold concept
  - time information $t_1$ from lower threshold $V_{\text{th}_T}$ → reduce time-walk
  - hit validation from higher threshold $V_{\text{th}_E}$
  - ToT: $t_1$ to $t_3$

- Time measurement
  - coarse time from chip clock
  - fine time from interpolation (interpolation factor 128x @160 MHz → 50 ps bin size)
PASTA Front-end

- Linearity
  - charge up to 40 fC (10 MIPs)
  - good linearity at low input charges
  - deviations compensated by calibration
PASTA Front-end

- Noise (ENC) from simulations
  - designed for input capacitance 5 pF to 25 pF

**Note:** 1uA leakage current contributes additional 500 electrons
PASTA Front-end

- Noise (ENC) from simulations
  - designed for input capacitance 5 pF to 25 pF
  - p-side: approx. 350 e- @ 10 pF
  - n-side: approx. 550 e- @ 17 pF

Note: 1uA leakage current contributes additional 500 electrons
PASTA Front-end

Layout screen-shots

complete channel

2069 µm (1862 µm)

70.9 µm

200 µm gap with Pminus shell
to increase resistance of substrate

R. Schnell, CANU 2014, Bad Honnef - December 15/16, 2014
PASTA Front-end

Layout screen-shots

2.07 mm (1.86 mm)

4.54 mm (4.09 mm)

64 channels
(without global control)
PASTA Front-end

- Submission in commercial 110nm technology beginning 2015
  - design in 130nm – channel pitch 70.9 µm
  - shrinking by foundry, factor 0.9 → channel pitch 63.8 µm
- Mitigation of Single-Event-Upset (SEU)
  - triple modular redundancy
  - Hamming encoding
- Power consumption based on simulations

<table>
<thead>
<tr>
<th>front-end</th>
<th>TDC</th>
<th>TDC ctrl</th>
<th>global ctrl</th>
<th>drivers</th>
<th>total</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 mW/ch</td>
<td>0.4 mW/ch</td>
<td>0.25 mW/ch</td>
<td>60 mW</td>
<td>4 x 8.5 mW</td>
<td>3.12 mW/ch</td>
</tr>
</tbody>
</table>

- target value: <4.0 mW/ch
- (LVDS drivers instead of SLVS)
Strip DAQ Chain

- PASTA
- MDC (Module Data Concentrator ASIC)
- GBT
- MMB (MVD Multiplexer Board)
- Compute Node
- SODANET

Double-Sided Silicon Strip Sensor

R. Schnell, CANU 2014, Bad Honnef - December 15/16, 2014
Module Data Concentrator (MDC)

- Data Concentrator ASIC at the stave level
  - Multiplexes all front-ends of one sensor
    - up to 12 front-ends per MDC
    - needs galvanic isolation of data lines, DC-balanced code
  - Slow control interface to front-end chips
  - Data concentration and feature extraction
Module Data Concentrator (MDC)

H. Sohlbach
FH Iserlohn
Module Data Concentrator (MDC)

- Power estimation
  - basic design: 72 mW
  - full design: 204 mW
  - SLVS-I/Os: 34 mW
  - Total basic: 106 mW
  - Total full: 236 mW

- Chip size estimation
  - 4.7 MGates → 20 mm²
  - 118 pads

- Use same commercial 110nm technology as PASTA
  - triple modular redundancy for all critical components
GBT

- Additional data concentration level
  • Multiplexes several MDCs connected via e-link protocol
  • Placed close to MVD
    • reduce length of electrical links
  • Fast optical links towards off-detector electronic
    • 3.2 Gbps user data rate
GBT boards

beam pipe

MVD
**MVD Multiplexer Board (MMB)**

- Off-detector electronics of the MVD
  (Developed in the Helmholtz Association of German Research Centers)

- **MTCA.4 compatible AMC module**
  - based on Xilinx Kintex-7 FPGA
  - 4 SFP/SFP+ cages (GTX transceiver)

- Connection to PANDA time distribution system (SODANET)

- Sends data to global PANDA DAQ system (Compute Nodes)
Test Tools – Laser Test Stand

- Recently set up by two Master students in Giessen
  
  - Laser
    - 1060 nm
    - internal or external trigger
  
  - X-Y-table
    - travel: 100 x 100 mm²
    - position resolution better than 1 µm
  
  - Data acquisition
    - Tracking-Station DAQ
Test Tools – Test Beams

- Test beam times at COSY
  • Tests of
    - sensors
    - readout electronics
    - DAQ
  • Synchronized data taking of pixel and strip systems
  • Soon: test of PASTA readout
Thank you for your Attention