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A Read-out System for the PANDA MVD Prototypes

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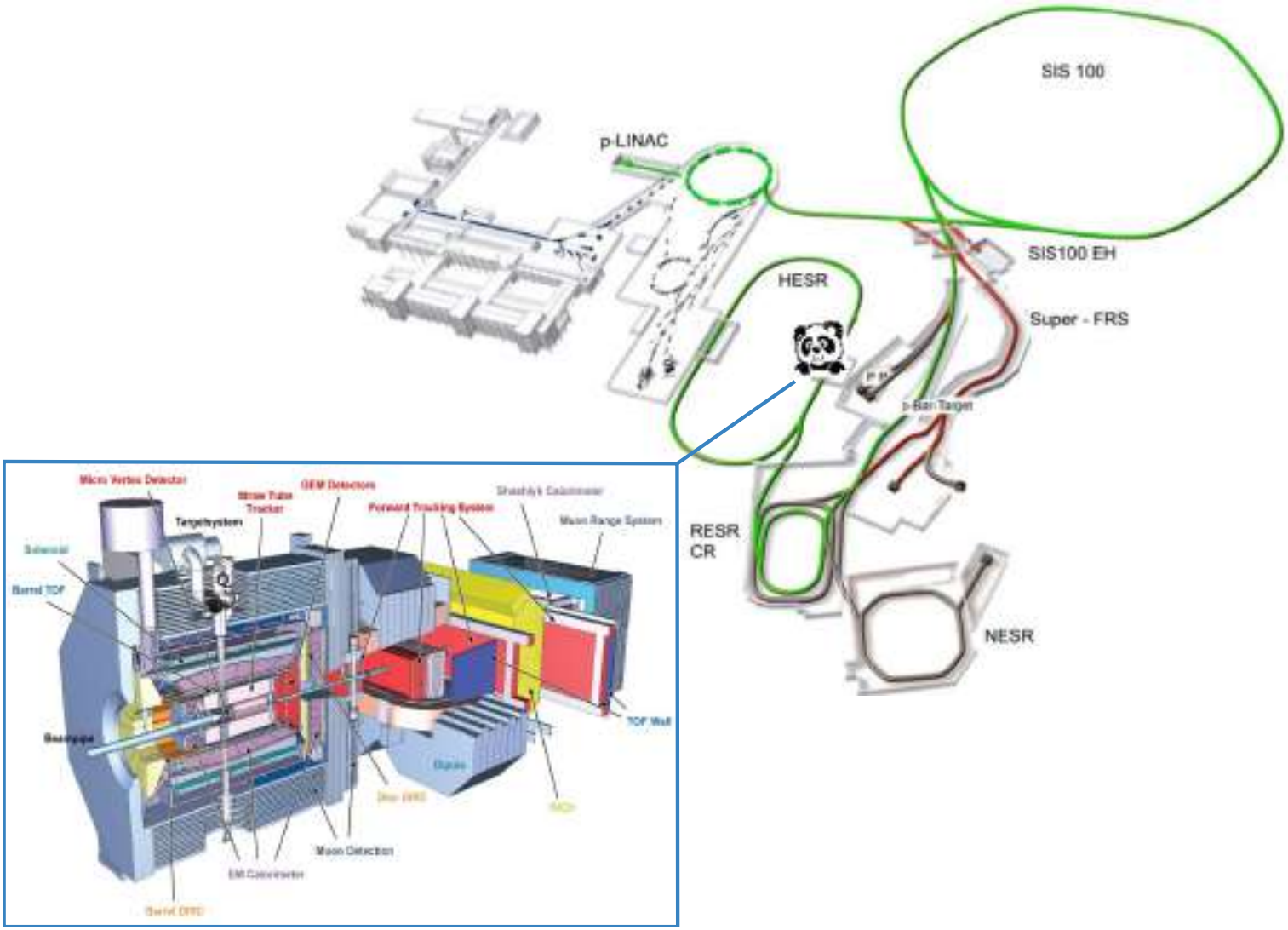
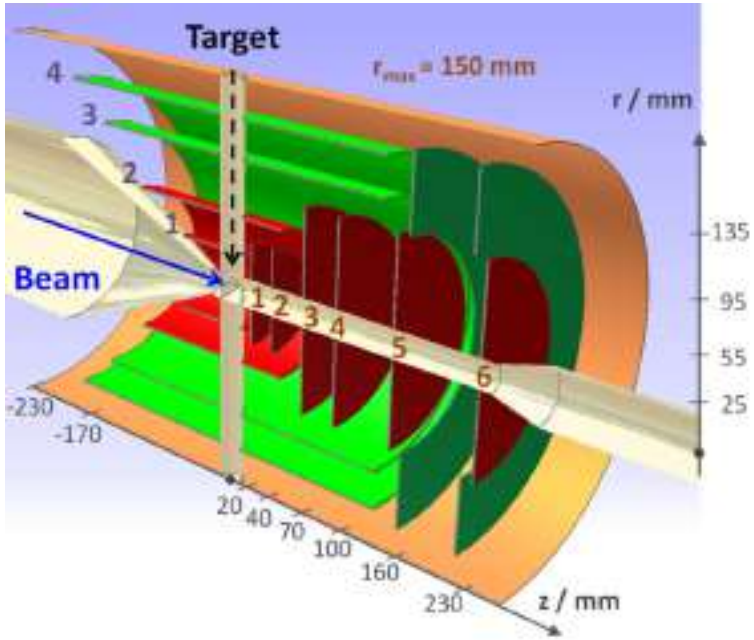
PANDA@FAIR

Facility for Antiproton and Ion Research



MVD: Micro Vertex Detector

- free running readout @clk freq 160 MHz
- vertex resolution $< 100\ \mu$m



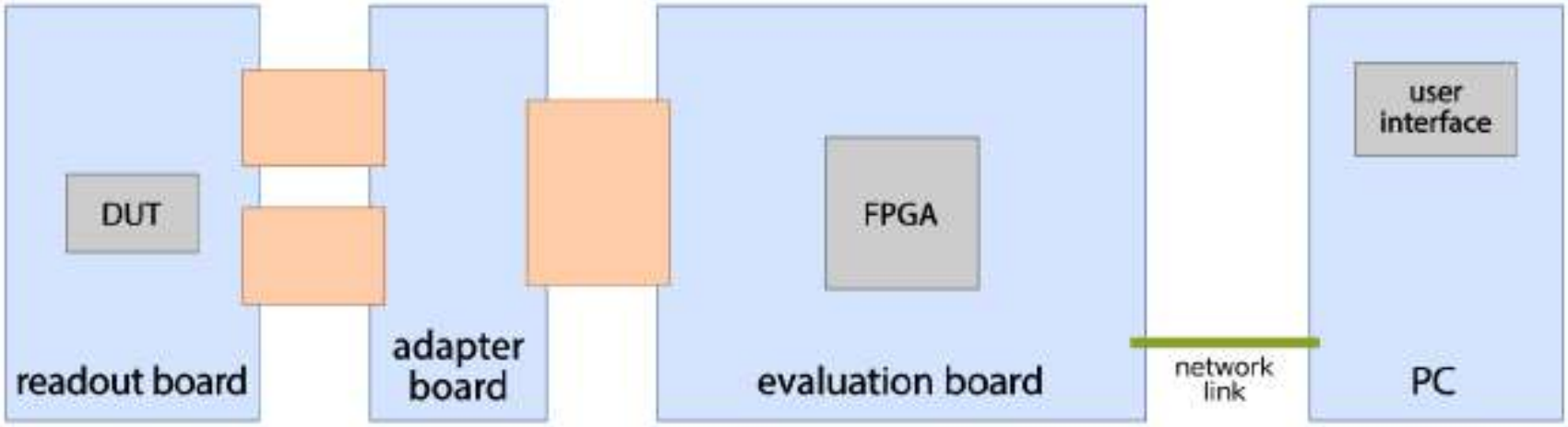
- time information < 10 ns
- deposited energy information for PID with dE/dx

- four barrel layers
- six disk layers in the fw direction
- pixel detectors in the inner part
  $\longrightarrow$ front-end chip: ToPix
- double-sided strip detectors in the outer part
  $\longrightarrow$ front-end chip: PASTA

High performance and flexible DAQ needed for ToPix and PASTA.

JDRS: Jülich Digital Readout System

The basic components



Data conversion and communication with the PC:

- DUT: ToPix, PASTA
- evaluation board: Xilinx ML605 (Virtex-6 FPGA)
- firmware: VHDL

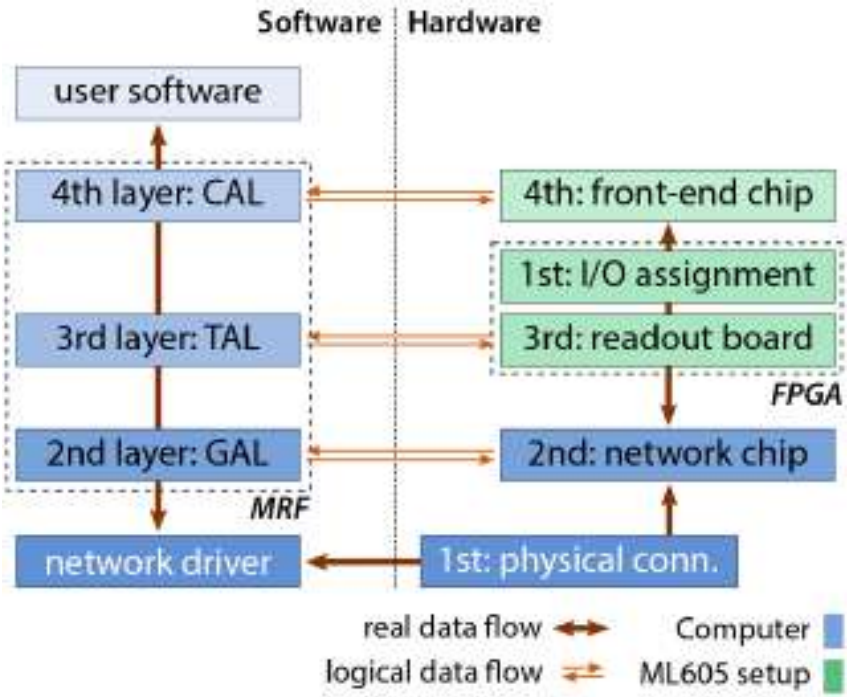
Configuration and data handling:

- PC
- software: C++
- MVD Readout Framework (MRF)
- Qt-based GUI

MRF: MVD Readout Framework

Four abstraction layers isolate low level from higher level functions:

- Physical Layer
  $\longrightarrow$ ethernet connection between ML605 and PC
- Generic Access Layer
  $\longrightarrow$ data transfer and formatting
  e.g. open a connection, send and receive data packages...
- Transport Access Layer
  $\longrightarrow$ board-specific functions
  e.g. the clock generation, flush of data buffers...
- Chip Access Layer
  $\longrightarrow$ DUT-specific functions
  e.g. configuration and data readout...



PASTA: PANDA Strip Asic

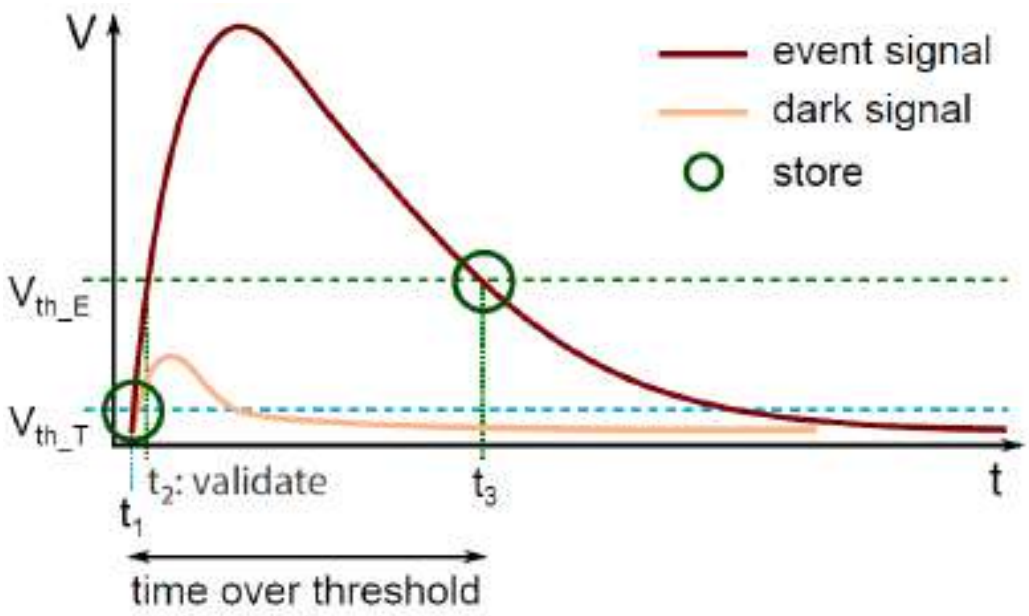
Free running readout chip for the strips

Concept based on TOFPET ASIC.

- Developed for medical application.
- Readout of SiPM.

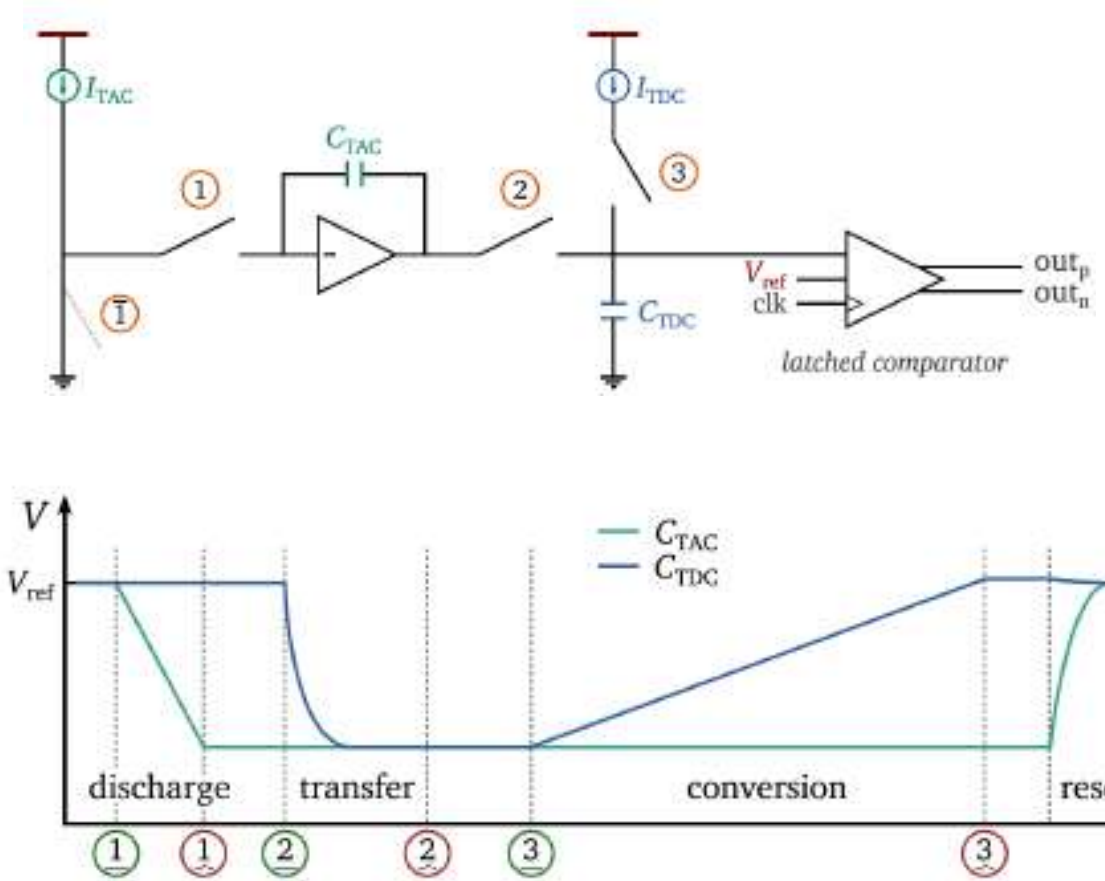
Time over threshold measurement based on two leading-edge discriminators.

- Low threshold - time branch: resolve leading edge of pulse(time stamp resolution).
- High threshold - energy branch: reduce jitter on the falling edge.



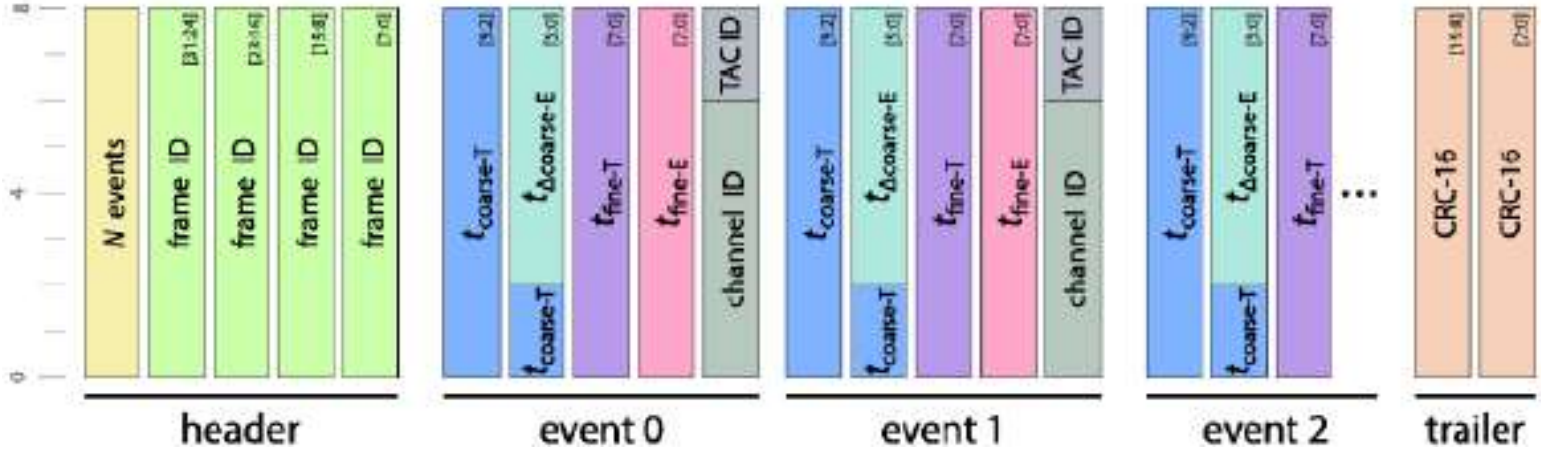
Timestamps

- Clock resolution: 6.25 ns (@160 MHz) - coarse timestamp.
- Enhanced resolution: up to 50 ps - fine timestamp.



Data Collection and Transfer

- Event data is stored in frames.
- Formatted with header/trailer.
- Continuous stream of data over the tx lines.
- 8b/10b encoding to ensure a DC-balanced line.
- Use of control symbols(comma words) between frames.



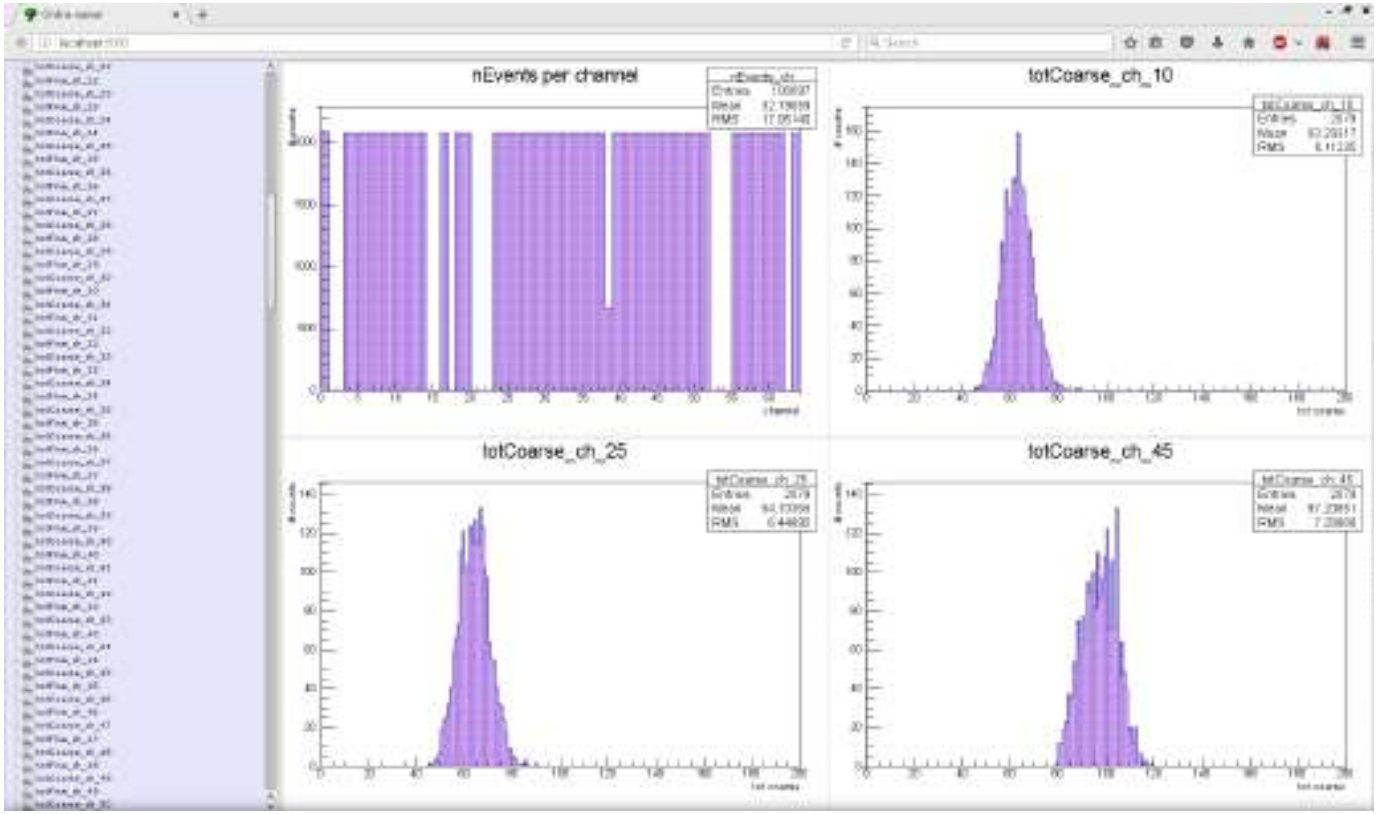
Data Handling

- FPGA data handling:
  - 10b/8b decoded data stored in FIFO.
- Software data handling:
  - request data from fifo;
  - store raw data on disk;
  - convert data word into usable object.

- Suppress comma words.
- Display frame indicator.
- Suppress empty frames.

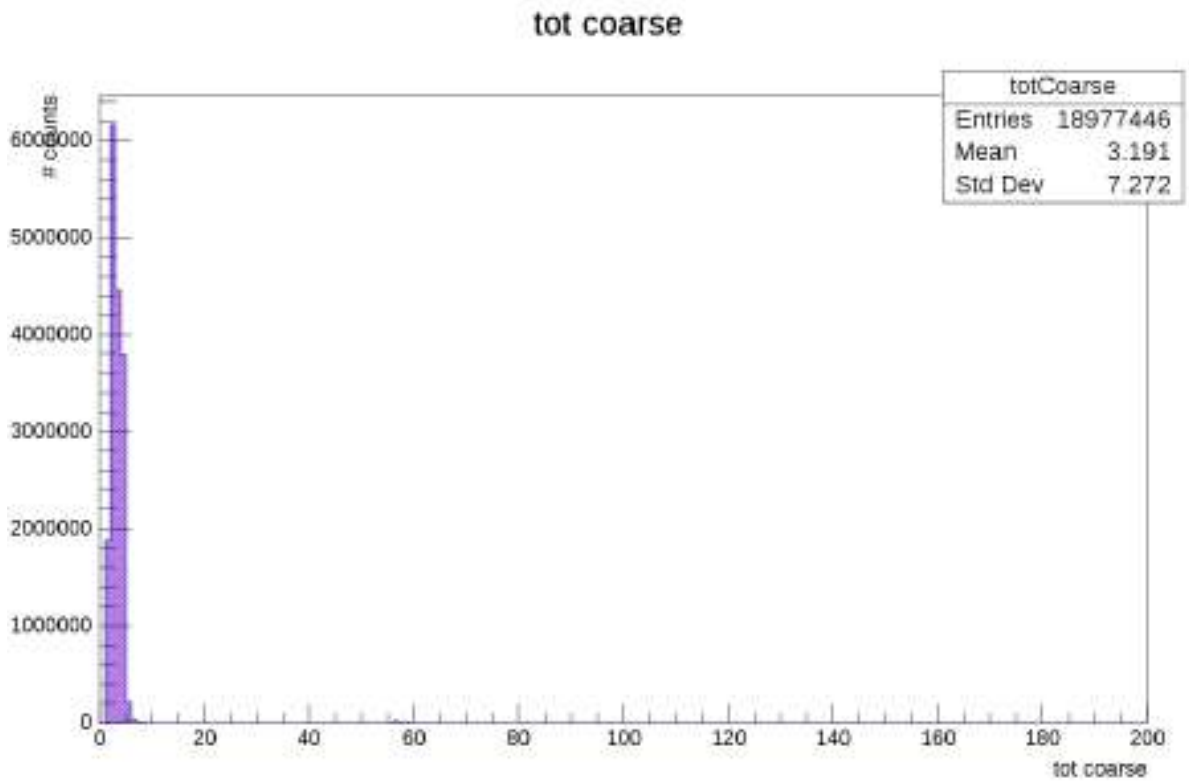
Online Monitoring

The data is decoded online.
The results are published on a web server using the *THttpServer* class from ROOT.



Online Monitoring

Energy spectrum — beta source



Configuration of the Internal Test Pulse

PASTA can generate a test pulse internally.
Two possibilities:

- test pulse used directly instead of the discriminator output (digital signal);
- test pulse fed throught the analog calibration circuit (analog signal).

Configure Internal TP

	Item	Pos	Len	Min	Max	Set Value
1	NPulses	0:9	10	0	1023	0
2	Pulse Lenght	10:17	8	0	255	0
3	Pulse Spacing	18:25	8	0	255	0

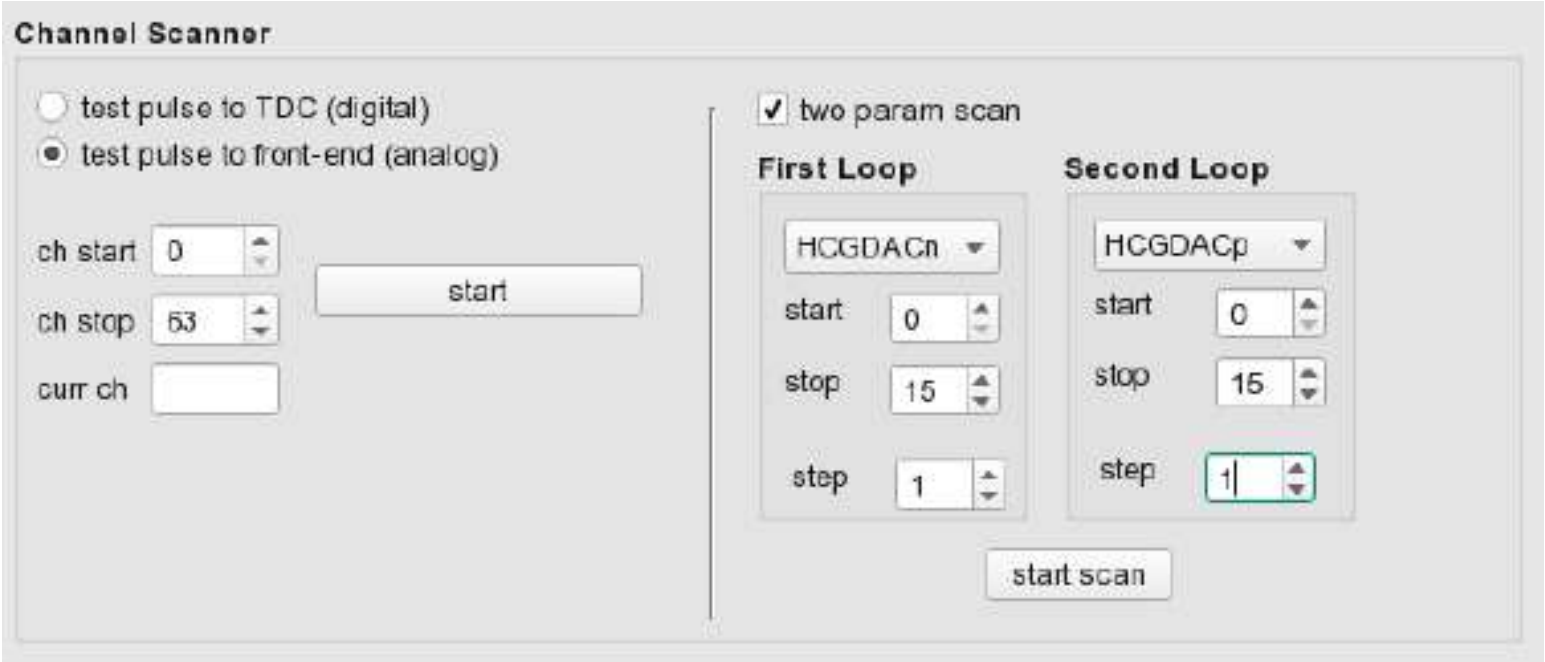
Configure Global TP

	Item	Pos	Len	Min	Max	Set Value
1	Channel address	8:13	6	0	53	0
2	Enable cal circuit	0	1	0	1	0
3	Probing signals from ch to pad	7	1	0	1	0
4	Pulse amplitude	1:6	6	0	53	0

Channel Scan

- PASTA has 46 global and 22 local free parameters.
- Automatize the measurements for the optimization of such parameters.

1. Define the type of injection.
2. Scan a user define range of channels.
3. Choose up to two parameters to sweep.



Summary & Outlook

- The PANDA MVD will use pixel and strip detectors.
- Two front-end chips: the Torino Pixel ASIC (ToPix) and the PANDA Strip ASIC (PASTA).
- A DAQ system able to perform systematic lab measurement and to work on a beam test environment is under development (JDRS).
- The system is designed such that the modifications required when passing from one prototype to another are minimal.

- The DAQ will be operating, together with PASTA, under beam this spring.

Backup

Time amplification

i.e. how to get the enhanced resolution.

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5.5.1.2 Time Amplification

The ASIC has an internal counter incremented by the clock to generate time stamps. Just using this counter to time events would lead to a precision based on the clock's period, or 6.25 ns for an input clock of 160 MHz. With the chosen scheme of converting the phase between a trigger and the clock into a proportional voltage drop and then recharge this, a time amplification is gained.

Two factors influence this amplification: a larger capacitance for the second capacitor

$$C_{\mathrm{TDC}} = 4 \cdot C_{\mathrm{TAC}} \tag{5.2}$$

and a lower recharging current

$$I_{\mathrm{TDC}} = 1/32 \cdot I_{\mathrm{TAC}} \,. \tag{5.3}$$

Using the relation for charge in a capacitor and constant currents

$$C \cdot U = Q = I \cdot t$$

one gets the gain of this method for the time after the process (t_{TDC}) versus the time before (t_{TAC}) by assuming the voltage level is equal after connecting both capacitors:

$$\begin{aligned} \frac{I_{\mathrm{TAC}} \cdot t_{\mathrm{TAC}}}{C_{\mathrm{TAC}}} &= U_{\mathrm{TAC}} = U_{\mathrm{TDC}} = \frac{I_{\mathrm{TDC}} \cdot t_{\mathrm{TDC}}}{C_{\mathrm{TDC}}} \\ \Rightarrow \quad t_{\mathrm{TDC}} &= t_{\mathrm{TAC}} \cdot \frac{I_{\mathrm{TAC}}}{I_{\mathrm{TDC}}} \cdot \frac{C_{\mathrm{TDC}}}{C_{\mathrm{TAC}}} \\ \overset{(5.2)\&(5.3)}{\Rightarrow} \quad &= t_{\mathrm{TAC}} \cdot 32 \cdot 4 = t_{\mathrm{TAC}} \cdot 128 \,. \end{aligned} \tag{5.4}$$