

# The PANDA Strip ASIC: PASTA

*DIRC 2017*

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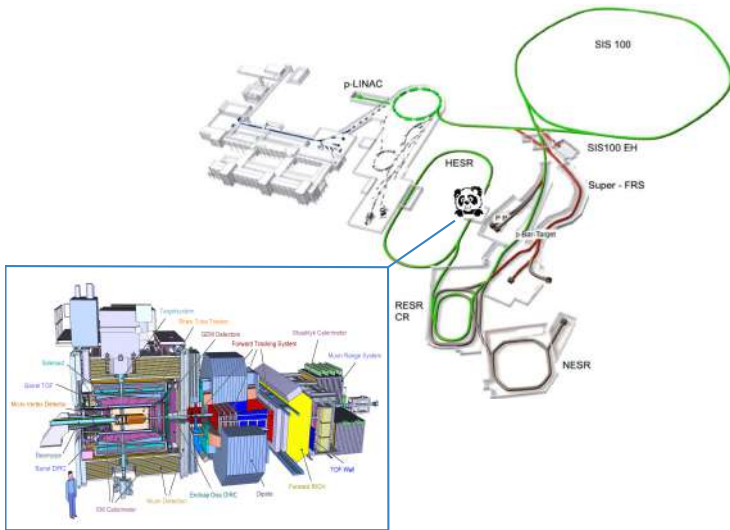
PANDA @FAIR

The PASTA chip

JDRS: Jülich Digital Readout System for the MVD

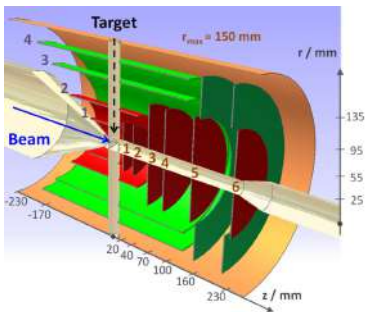
Quantitative Measurements

Summary



# MVD: Micro Vertex Detector

- free running readout @clk freq 160 MHz
- vertex resolution  $< 100 \mu\text{m}$



- time information  $< 10 \text{ ns}$
- deposited energy information for PID with  $dE/dx$
- four barrel layers
- six disk layers in the fw direction
- pixel detectors in the inner part  
→ front-end chip: ToPix
- double-sided strip detectors in the outer part  
→ front-end chip: PASTA

# PASTA: PANDA Strip ASIC

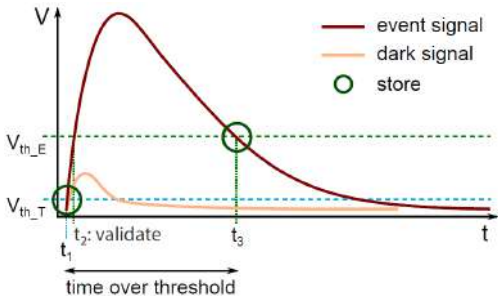
*Free running readout chip for the strips*

Concept based on TOFPET ASIC.

- Developed for medical application.
- Readout of SiPM.

Time over threshold measurement based on two leading-edge discriminators.

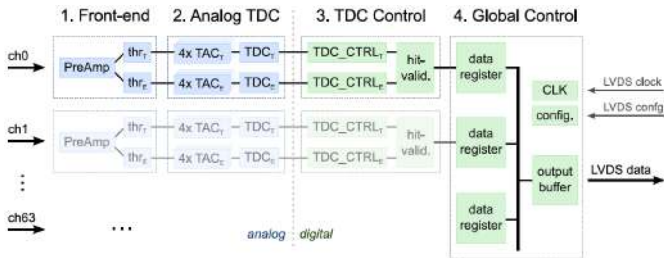
- Low threshold - time branch: resolve leading edge of pulse (time stamp resolution).
- High threshold - energy branch: reduce jitter on the falling edge.



	TOFPET v1	PASTA v1
Input capacitance/charge	SIPM: 320 pF / 300 pC	Si Strips: 50 pF / 38 fC
Power consumption	7-8 mW/ch	< 4 mW/ch
Channel pitch	104 $\mu\text{m}$	63 $\mu\text{m}$
Radiation tolerance	n/a	100 kGy
Efficiency gap	ca. 6% evt loss	no evt loss
Charge resolution	less important	8 bit dyn. range

Additional changes:

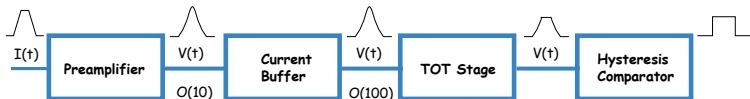
- Switch to area optimized technology (110 nm).
- Rewritten control logic.



- 1 Amplification and discrimination.
- 2 Time interpolation.
- 3 Control charge conversion and initiate timestamp storing.
- 4 Handle configuration and channel data.

## Auxiliary circuits:

- Calibration circuit: configurable test pulse generation.
- Output drivers: conversion of outgoing signals to LVDS standard.
- Bias cells: voltage levels for analog components.

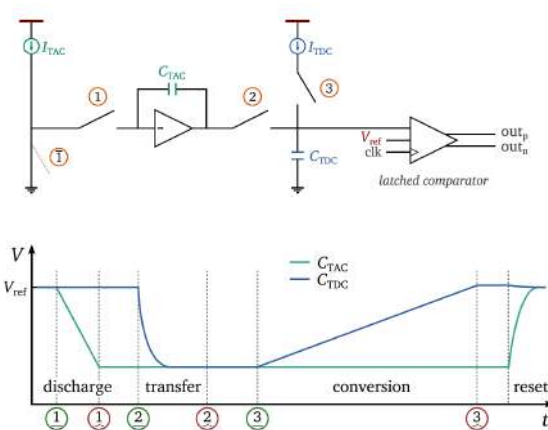


- Preamplifier: amplification of small current signal from sensor.
- Current buffer: second amplification and impedance adjustment.
- TOT stage: third amplification, improved linearity of the system, saturated amplifier.
- Hysteresis comparator: comparison with threshold voltage (different for rising and falling edge).

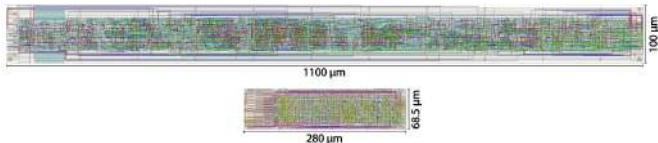


# Analog Time to Digital Converter (TDC)

- Clock resolution: 6.25 ns (@160 MHz) - coarse timestamp.
- Enhanced resolution: up to 50 ps - fine timestamp.



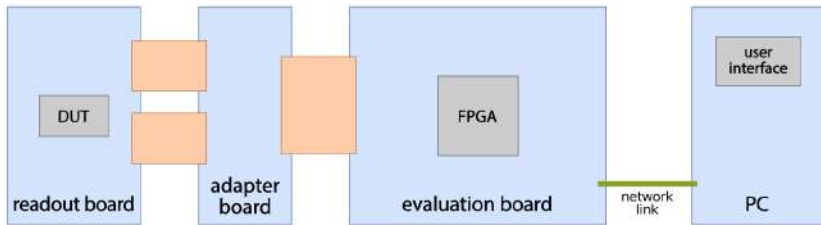
- TDC controller:
  - interface between analog circuitry and digital storing/transmission of data;
  - detects valid events and store measurement for them;
  - size reduced by 80% wrt TOFPET;
  - power consumption reduced by half wrt TOFPET;
  - radiation-hard logic for Single Event Upset (SEU) protection.



- Global controller:
  - configuration interface;
  - clock distribution;
  - global time counter;
  - test pulse generation;
  - channel multiplexing;
  - data collection and transfer.

# JDRS: Jülich Digital Readout System

*The basic components*



Data conversion and communication with the PC:

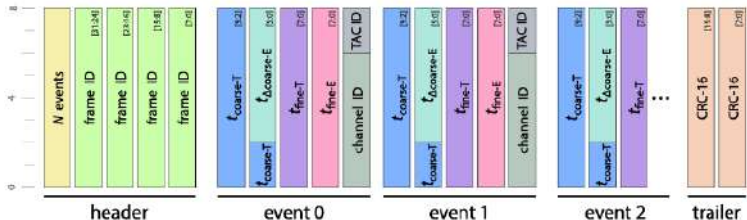
- DUT: ToPix, **PASTA**
- evaluation board: Xilinx ML605 (Virtex-6 FPGA)
- firmware: VHDL

Configuration and data handling:

- PC
- software: C++
- MVD Readout Framework (MRF)
- Qt-based GUI

# Data Collection and Transfer

- Event data is stored in frames.
- Formatted with header/trailer.
- Continuous stream of data over the tx lines.
- 8b/10b encoding to ensure a DC-balanced line.
- Use of control symbols (comma words) between frames.



# Data Handling

- FPGA data handling:
  - 10b/8b decoded data stored in FIFO.
- Software data handling:
  - request data from fifo;
  - store raw data on disk;
  - convert data word into usable object.

DAQ FIFO data

pathname:  
software/GUI\_modules/daqReader/readoutData/decode/

filename:  
test.dat

Save using:  
 ASCII  
 boost serial.

suppress comma words  
 display frame indicator  
 suppress empty frames

readout iterations: 200

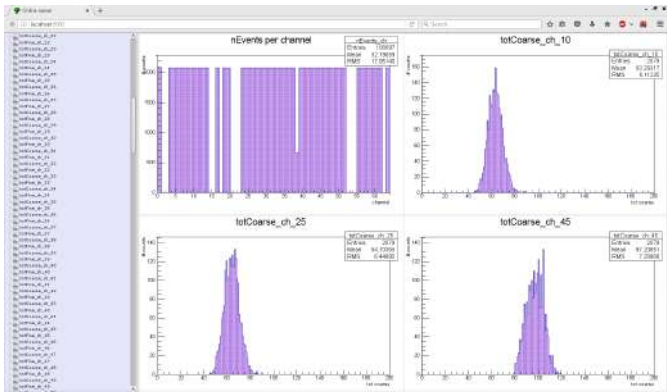
current iteration:

start readout stop readout

- Suppress comma words.
- Display frame indicator.
- Suppress empty frames.

The data is decoded online.

The results are published on a web server using the *THttpServer* class from ROOT.



# Configuration of the Internal Test Pulse

PASTA can generate a test pulse internally.

Two possibilities:

- test pulse used directly instead of the discriminator output (digital signal);
- test pulse fed through the analog calibration circuit (analog signal).

Configure internal TP

Item	Pos	Len	Min	Max	Set Value
1 NPulses	0:9	10	0	1023	0
2 Pulse Length	10:17	8	0	255	0
3 Pulse Spacing	18:25	8	0	255	0

Configure Global TP

Item	Pos	Len	Min	Max	Set Value
1 Channel address	0:13	6	0	63	0
2 Enable cal circuit	0	1	0	1	0
3 Probing signals from ch to pad	7	1	0	1	0
4 Pulse amplitude	1:6	6	0	63	0

# Channel Scan

- PASTA has 46 global and 22 local free parameters.
  - Automatize the measurements for the optimization of such parameters.
- 1 Define the type of injection.
  - 2 Scan a user define range of channels.
  - 3 Choose up to two parameters to sweep.

**Channel Scanner**

test pulse to TDC (digital)  
 test pulse to front-end (analog)

ch start    
 ch stop   
 curr ch

two param scan

<p><b>First Loop</b></p> <p>HCGDACn ▾</p> <p>start <input type="text" value="0"/></p> <p>stop <input type="text" value="15"/></p> <p>step <input type="text" value="1"/></p>	<p><b>Second Loop</b></p> <p>HCGDACp ▾</p> <p>start <input type="text" value="0"/></p> <p>stop <input type="text" value="15"/></p> <p>step <input type="text" value="1"/></p>
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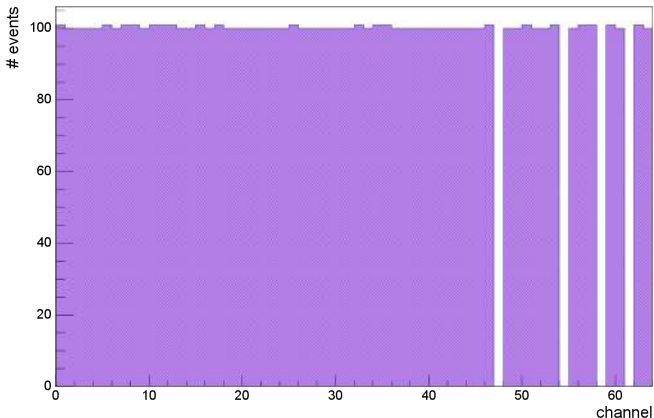
# Performance Measurements

Measurement to characterize the chip are currently ongoing:

- in the laboratory;
  - under beam (next fall).
- 
- Focus on the coarse information for both time and energy branch.
  - No detailed studies on the TDC yet.
  - Operation frequency is half of the nominal one (i.e., 80 MHz).

# Channel Response

Scan of all the channels for fixed amplitude.

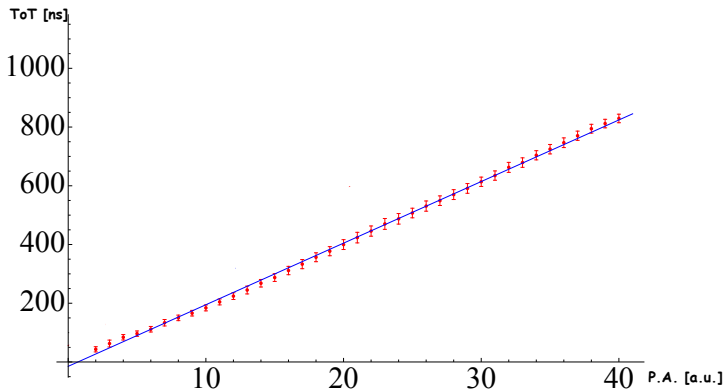


Not all the channels are responsive.

# ToT Linearity

Scan of all the channels within a given amplitude range.  
Only coarse information used.

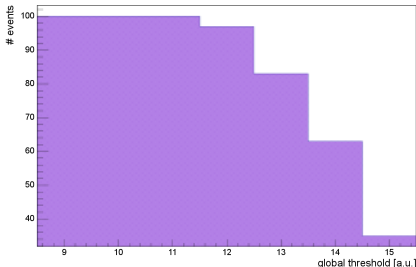
$$ToT = t_{coarse_E} - t_{coarse_T}$$



# Threshold determination

Amplitude incoming signal  $>$  threshold  $\rightarrow$  signal detected

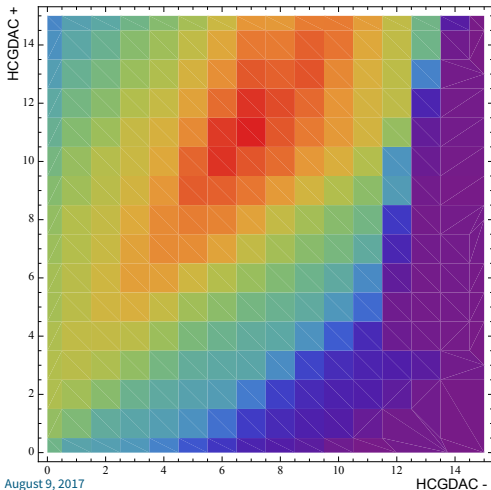
- Global threshold:  $\Delta_{th} = HCGDAC_+ - HCGDAC_-$   
 $\rightarrow$  midvalue of an interval with predefined amplitude.
- Local threshold: fine tuning.
- Sweep over  $\Delta_{th}$  at fixed pulse amplitude  $\rightarrow$  expected: S-curve shape.



- S-curve structure only for some channels  
 $\rightarrow$  box distribution even for small amplitudes.
- Different optimal values for different channels.

# Threshold distribution

Find the combination of  $HCGDAC_+$  and  $HCGDAC_-$  to maximize nEv.  
Fixed pulse amplitude.



- The PANDA MVD will use pixel and strip detector.
- For the strip, part the PASTA chip was designed.
- It is inspired from the TOFPET ASIC, but it fulfills specific requirement of the MVD.
- A dedicated readout system is under development at FZJ.
- Measurement to assess the performances of the chip have started and are still ongoing.
- Preliminary results hint to the fact that the measurement principle is working in PASTA.
- More optimization is needed: aim for a PASTA version 2.

# Backup

# Time amplification

*i.e. how to get the enhanced resolution.*

## 5.5.1.2 Time Amplification

The ASIC has an internal counter incremented by the clock to generate time stamps. Just using this counter to time events would lead to a precision based on the clock's period, or 6.25 ns for an input clock of 160 MHz. With the chosen scheme of converting the phase between a trigger and the clock into a proportional voltage drop and then recharge this, a time amplification is gained.

Two factors influence this amplification: a larger capacitance for the second capacitor

$$C_{TDC} = 4 \cdot C_{TAC} \quad (5.2)$$

and a lower recharging current

$$I_{TDC} = 1/32 \cdot I_{TAC} \quad (5.3)$$

Using the relation for charge in a capacitor and constant currents

$$C \cdot U = Q = I \cdot t$$

one gets the gain of this method for the time after the process ( $t_{TDC}$ ) versus the time before ( $t_{TAC}$ ) by assuming the voltage level is equal after connecting both capacitors:

$$\begin{aligned} \frac{I_{TAC} \cdot t_{TAC}}{C_{TAC}} = U_{TAC} &= U_{TDC} = \frac{I_{TDC} \cdot t_{TDC}}{C_{TDC}} \\ \Rightarrow t_{TDC} &= t_{TAC} \cdot \frac{I_{TAC}}{I_{TDC}} \cdot \frac{C_{TDC}}{C_{TAC}} \\ \stackrel{(5.2) \& (5.3)}{\Rightarrow} &= t_{TAC} \cdot 32 \cdot 4 = t_{TAC} \cdot 128 \end{aligned} \quad (5.4)$$