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INTERNATIONAL PHD PROJECTS IN APPLIED NUCLEAR PHYSICS AND INNOVATIVE TECHNOLOGIES

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Data Acquisition System for Straw Tube Detector in Cracow

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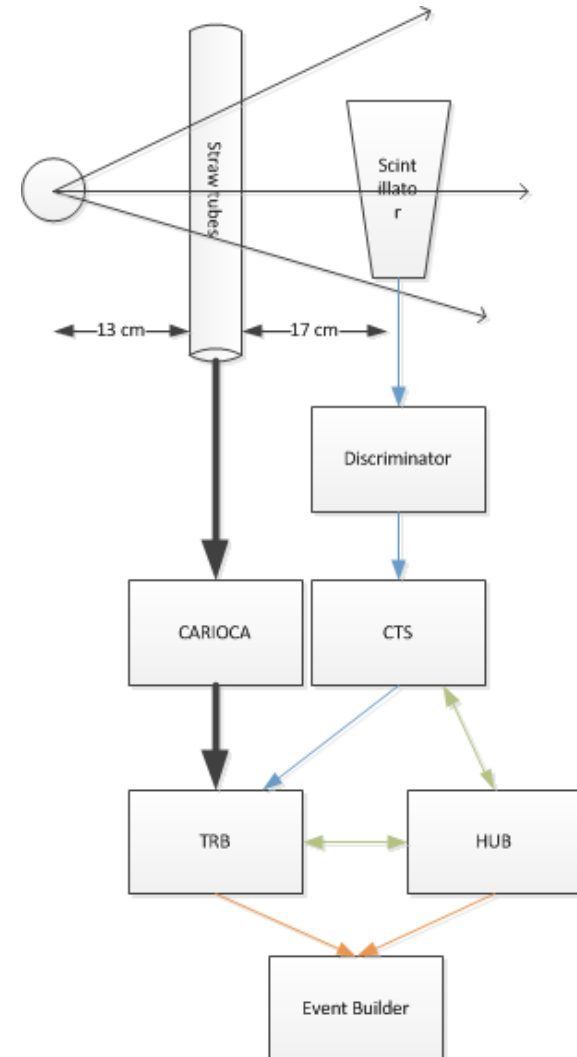
Plan

1. Test setup
2. Hardware
 1. CARIOCA
 2. TRBv2
 3. HUBv2
 4. CTS
3. Measurements
 1. Noise
 2. Channels and timing
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4. Summary



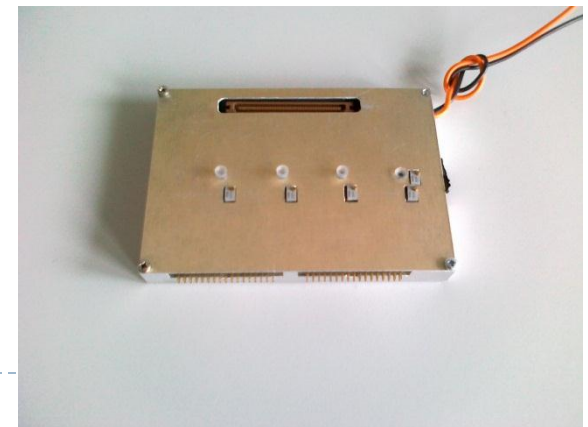
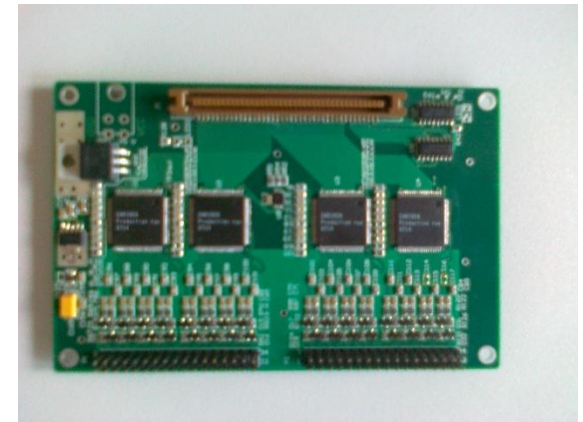
Test Setup

- ▶ Triggering done by scintillator
- ▶ NIM modules as discriminator
- ▶ Trigger control by CTS
- ▶ CARIOCA as Straws Front-End
- ▶ Time measurement by HPTDC on TRB
- ▶ Trigger rate 145kHz
- ▶ Uplink bandwidth 50 MBps
- ▶ Reference time, TrbNet, Gigabit Ethernet
- ▶ Lightweight unpacker



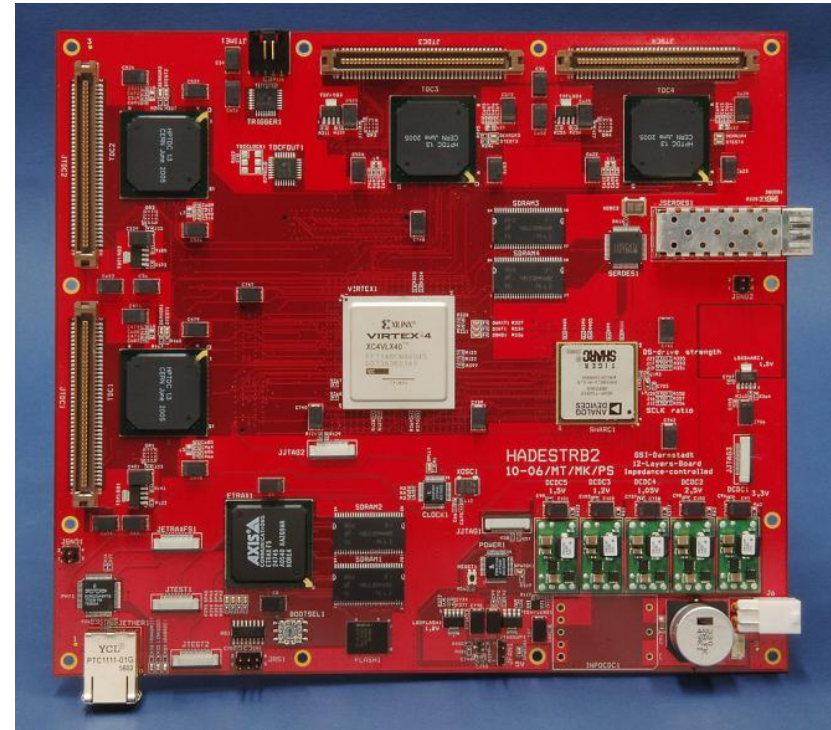
Hardware - CARIOCA

- ▶ CARIOCA
 - ▶ Amplifier, shaper, baseline restorer, discriminator
 - ▶ LVDS outputs
- ▶ CARIOCA Board 1
 - ▶ 4x 8 channel CARIOCA
 - ▶ Manually adjustable thresholds per device
- ▶ CARIOCA Board 2
 - ▶ 4x 8 channel CARIOCA
 - ▶ Remote thresholds adjustment per device
 - ▶ Different input plugs to reduce crosstalk



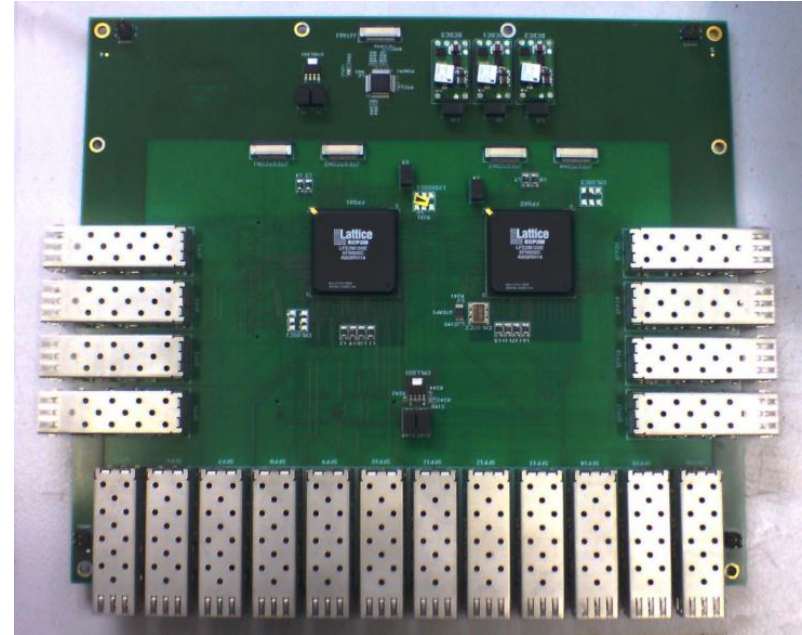
Hardware – TRBv2

- ▶ 4x HPTDC
 - ▶ 32 channels each
 - ▶ Up to 17ps resolution
- ▶ 1x Xilinx Virtex4 FPGA
- ▶ 1x ETRAX
- ▶ 1x 2Gbps Optical link
- ▶ 1x RJ45
- ▶ 1x Addon connector
- ▶ 1x Reference time input



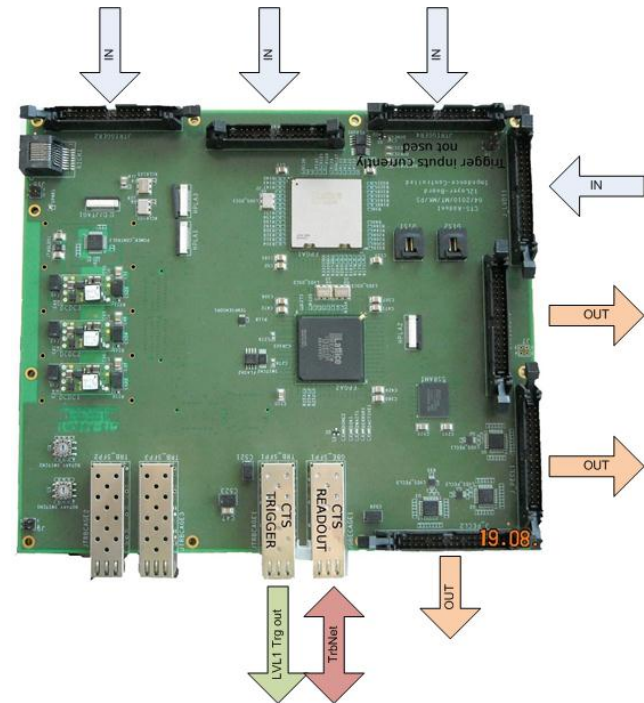
Hardware – HUBv2

- ▶ 2x Lattice ECP2M100 FPGA
- ▶ 20x 2Gbps optical links
 - ▶ Multiprotocol
 - ▶ Current setup:
 - ▶ 1 Gigabit Ethernet
 - ▶ 1 TrbNet – Trigger channel
 - ▶ 1 TrbNet – Slow Control channel
 - ▶ 16 TrbNet - General



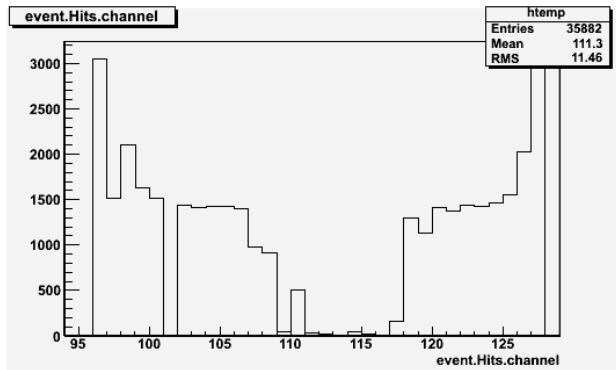
Hardware - CTS

- ▶ 68 x LVDS trigger inputs
- ▶ 51 x LVDS trigger outputs
- ▶ 1 x RJ45 trigger output
- ▶ 1 x TrbNet Trigger output
- ▶ 1 x TrbNet general connection
- ▶ 1x Lattice SCM – trigger logic
- ▶ 1x Lattice ECP2M50 – optical links control

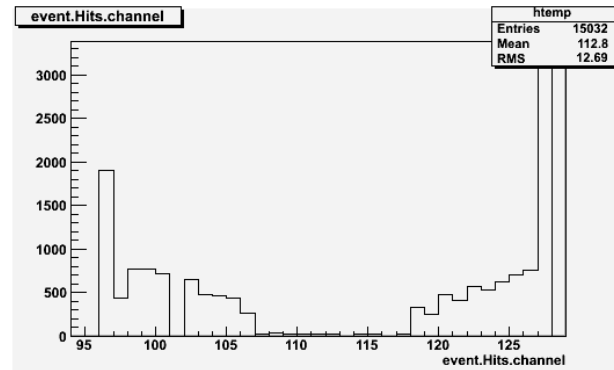


Measurements - noise

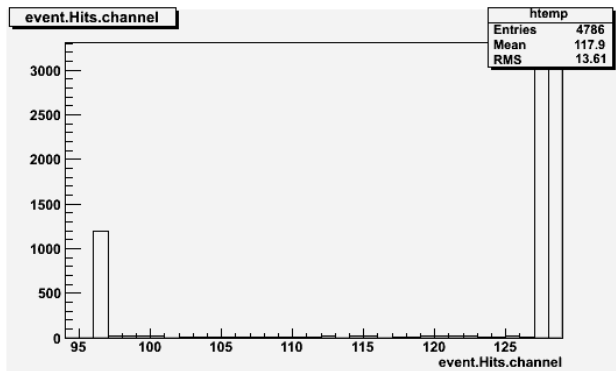
▶ Noise and thresholds adjustment - CARIOCA1



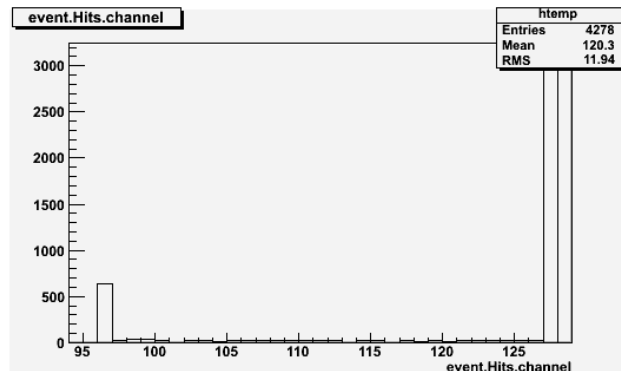
Threshold 1000



Threshold 1100



Threshold 1150

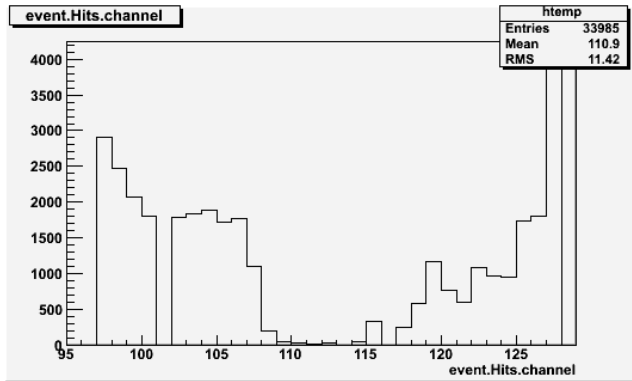


Threshold 1200

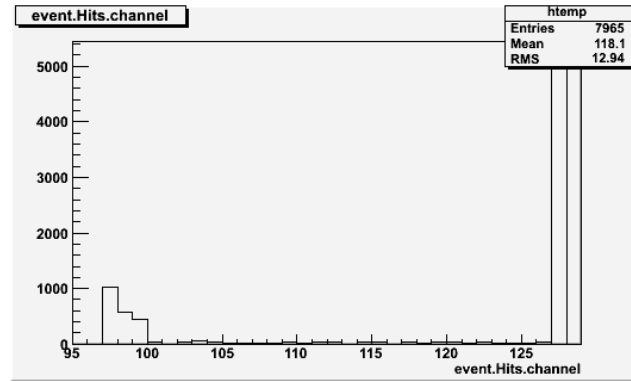
- CARIOCA devices on borders generate more noise
- CARIOCA board has to be shielded
- Long cable between CARIOCA board and TRB has to be shielded
- Common grounding doesn't help

Measurements – noise

▶ Noise and threshold adjustment – CARIOCA 2

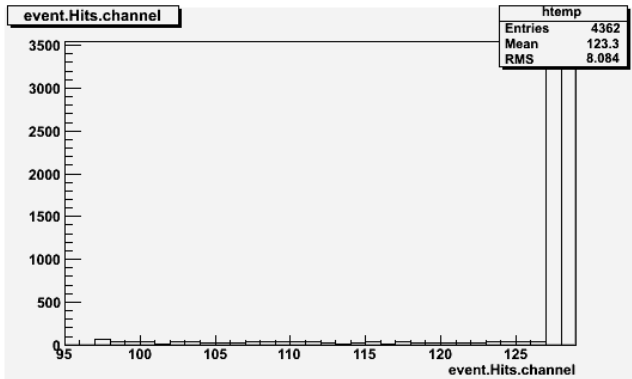


Threshold 900

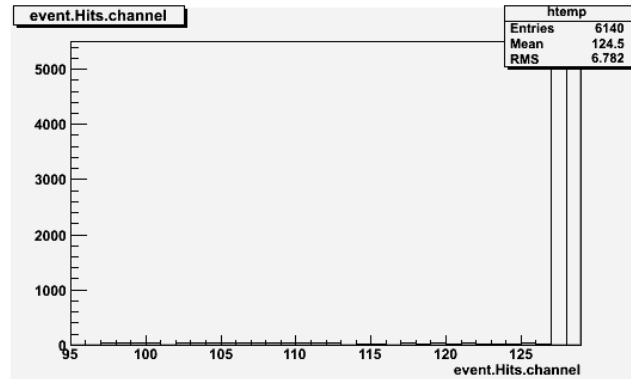


Threshold 1000

- Almost the same behaviour as for CARIOCA1



Threshold 1050

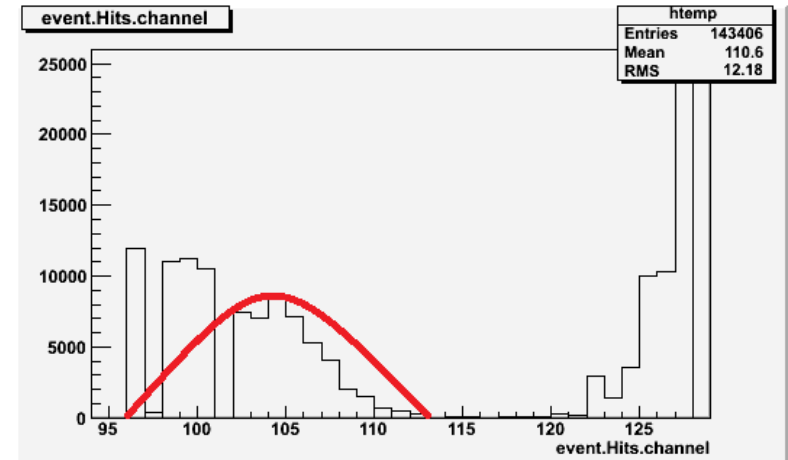


Threshold 1200

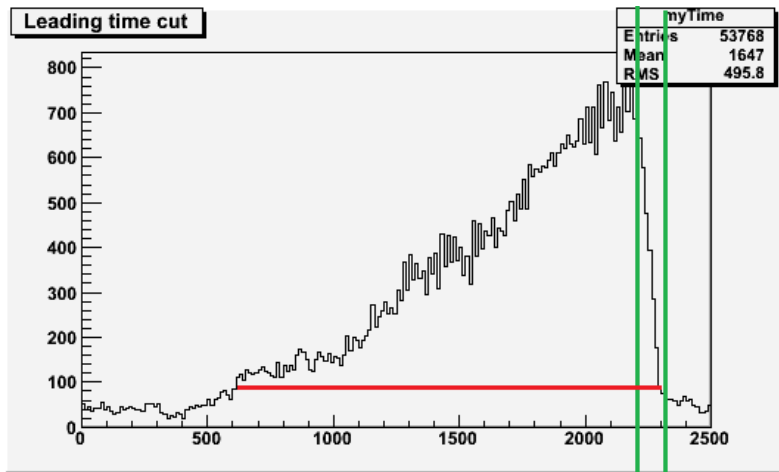


Measurements – channels and timing

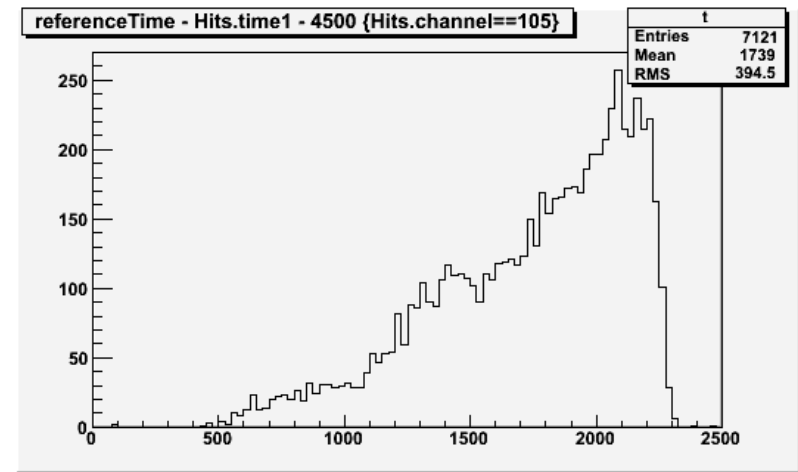
- ▶ Risetime: ~10ns
- ▶ Maximum drift time: 180ns



Hits on channels



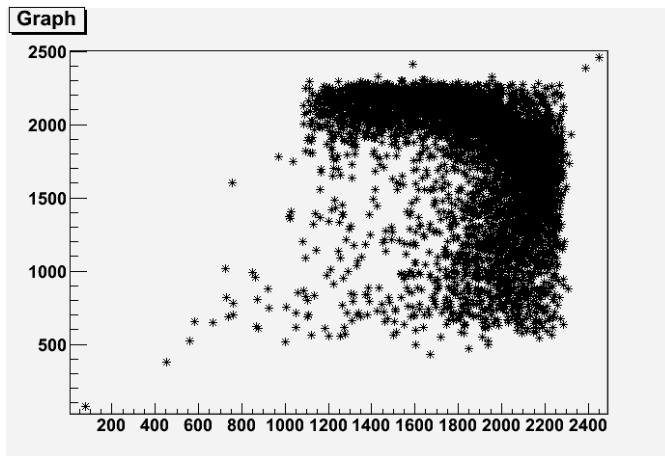
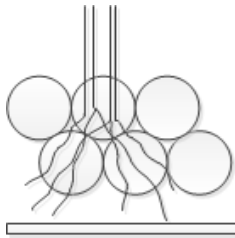
Leading time for all channels



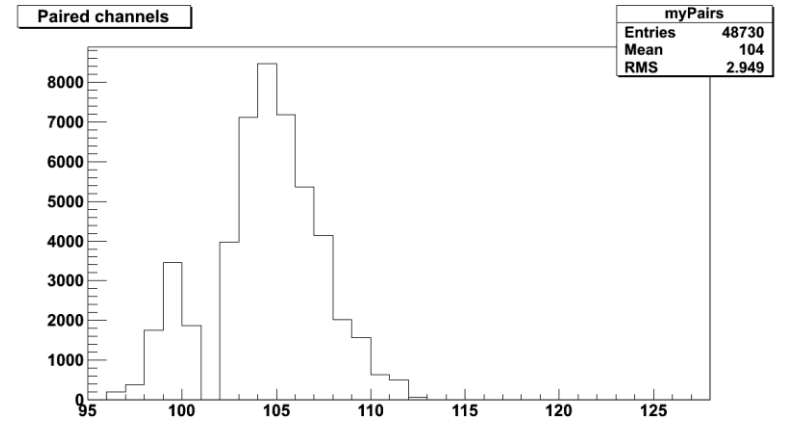
Leading time for channel 105

Measurements - tracks

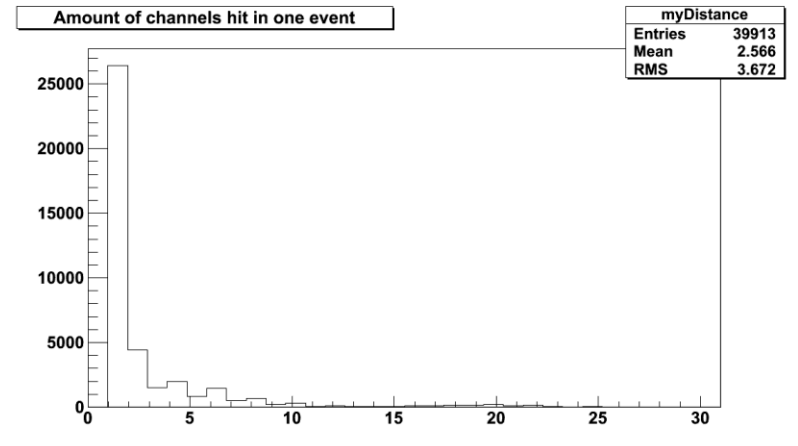
- ▶ Selection of channels with hits on neighbours
- ▶ Low-energetic electrons disperse in gas



T1 and T2 for channel 105



Channels with neighbours hits



Common hits on all channels (distance between channels)

Summary and plans

- ▶ Very sensitive setup – a lot of effort on shielding needed
- ▶ Correct CARIOCA 2 problems
- ▶ Migrate to Marek Idziks' ASIC chip



Backup

