IPMI Contoller

Johannes Lang

II. Physikalisches Institut
JLU Giessen

Agenda

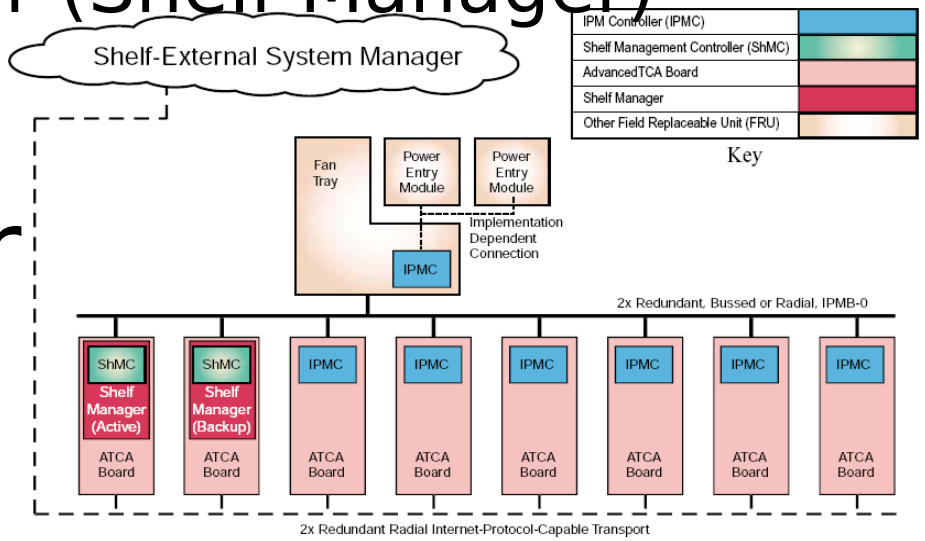
- IPMI & Requirements for Compute Nodes
- Functional Devices
- Design
- Program Flow
- Status / Outlook

General IPMI

Intelligent Platform Management Interface

- manage & monitor the operation and health of each FRU
- provide communication, management and control among the distributed contollers to an overall System Manager (Shelf Manager)

→ IPM Controller

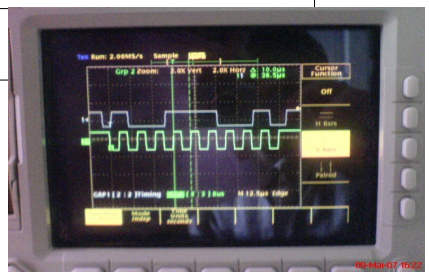


IPMI commands

- Genaral IPMI request format

Byte	Data Field
1	Responder Slave address
2	NetFn / Responder LUN (6bits/2bits)
3	Header Checksum
4	Request Slave Address
5	RequestSequence / Requester LUN
6	Command
7:N	Data Bytes
N+1	DataCheksum

Transmitted via I²C →

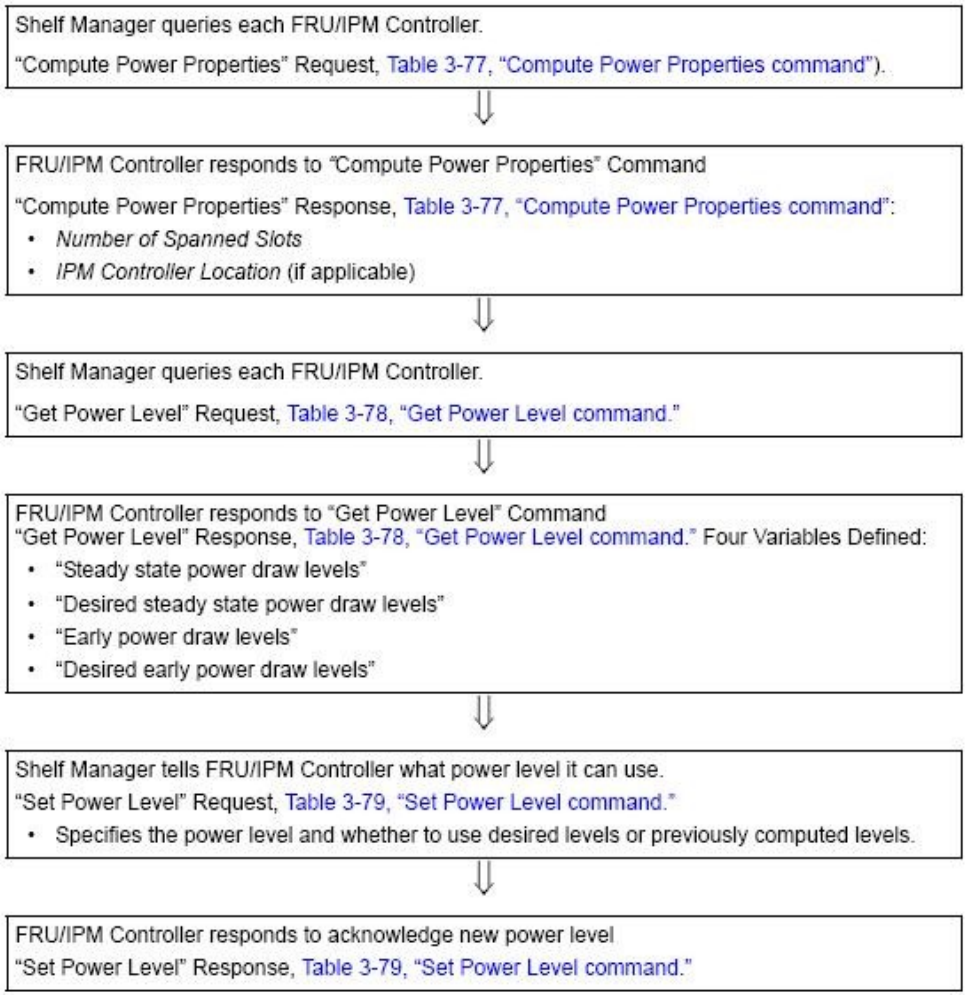


- General IPMI response format

Byte	Data field
1	Requester Slave Address
2	NetFn / Requester LUN (6bits/2bits)
3	Header Checksum
4	Responder Slave Address
5	Request Sequence / Responder LUN
6	Command
7	Completion Code
8:N	Data Bytes
N+1	Data Checksum

Example: Power Negoitiation

Figure 3-16 Power discovery Board/FRU participation



Ask for Power Properties

Power Properties

Ask for Desired Power Level

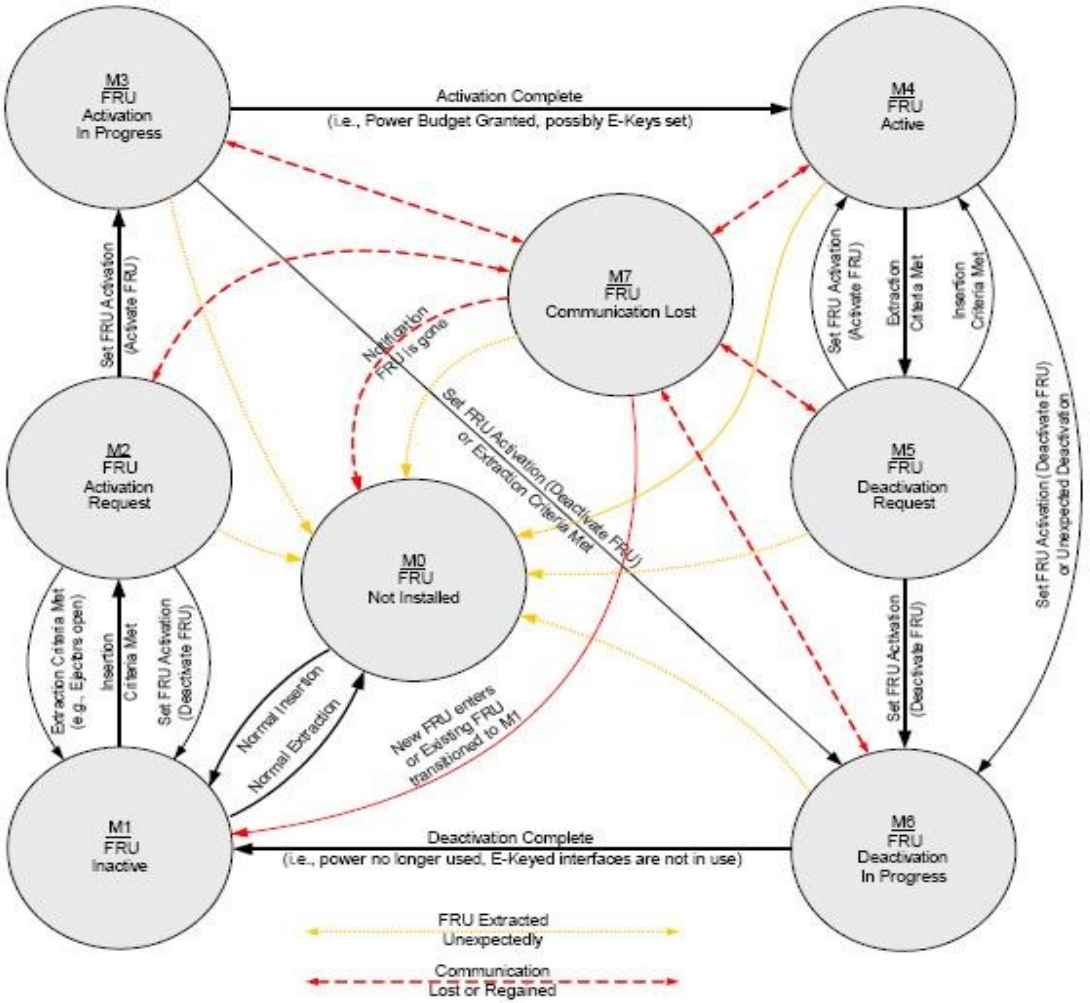
Desired Power Level

Granted Power Level

Acknowledge Power Level

IPMI State Machine

Figure 3-6 FRU state transitions, including unexpected transitions and error conditions



IPMI Requirements for Compute Nodes

- Get the Hardware Address
- Negotiate Power with Shelf Manager
- Set Bitstream Address for booting
- Enable DC/DC for Compute Node
- Monitore Voltages
- Check Configuration of FPGA`s
- Get further FPGA information via Status Bus
- Read Temperature Sensors
- Report to Shelf Manager
- Show status on front panel
- Receive Reset Command via button
- Provide Hot Swap
- Answer requests from Shelf Manager

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Atmel ATmega2560

- AVR 8-Bit Microcontroller with RISC Architecture
- 256KByte Flash
- 1 x TWI (2-wire Serial Interface = I²C)
- External- & Pin Change Interrupt
- 86 Programmable I/O Lines

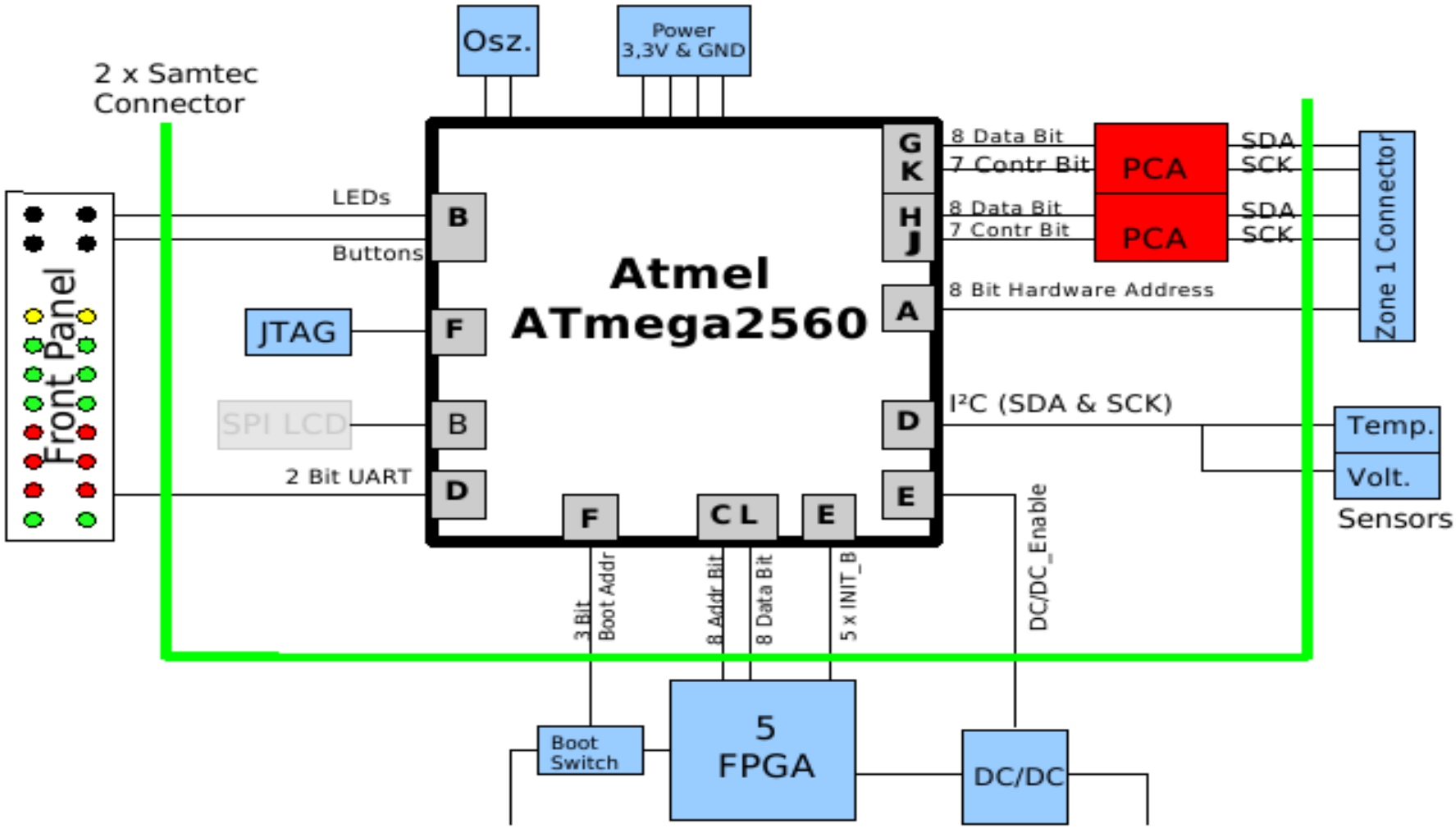
NXP PCA9665

- Parallel to I²C Interface
- 8 Data Bits
- 7 Control Bits
- Internal Oszillator

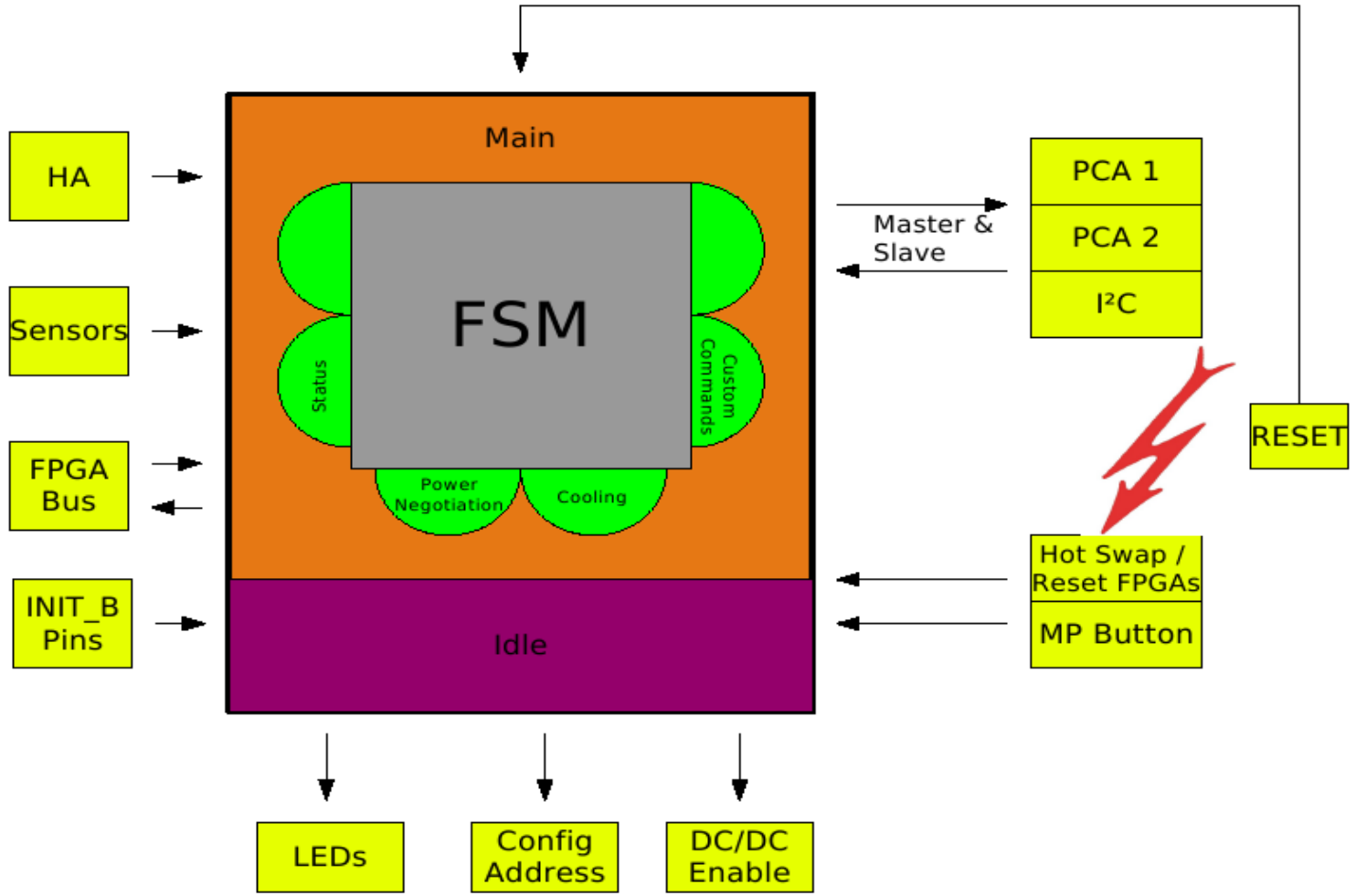
Realization of Signals

- 8 Bit Hardware Address
- 2 x I²C Interface PCA to Shelf Manager
- DC_Enable Signal
- 5 x INIT_B_0 (one to each FPGA)
- I²C Bus for Sensors
  - Temperature Sensor for each FPGA
  - Volage Sensor for every voltage
- 3 Bit Configuration Address boot bitstream selection
- Status Bus to FPGA`s (8bit address + 8 bit data)
- LED`s & buttons on front panel

IPMC Add-on Card

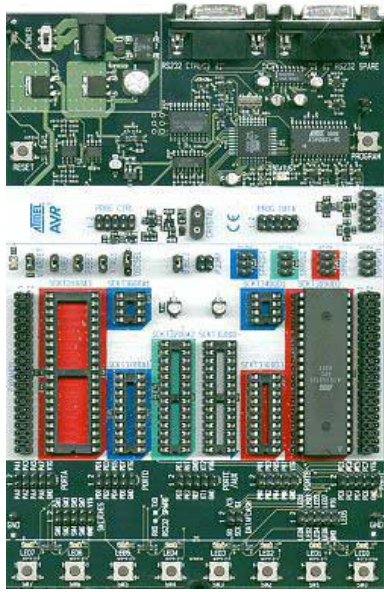


Program Flow



status & outlook

- Testing on STK500
- Programming in C (avr-gcc, avrlibc)
- I²C communication with Shelf Manager on ATCA
- Prompting information via UART
- TODO
  - Implement complete IPMI commands
  - Test PCA9665 from NXP
  - Layout of IPMC



Thanks for your attention!

Connector & Front Panel

Connector 1

Pin	Function
1	GND
2	PICMG_HA0
3	PICMG_HA1
4	GND
5	GND
6	PICMG_HA2
7	PICMG_HA3
8	GND
9	GND
10	PICMG_HA4
11	PICMG_HA5
12	GND
13	GND
14	PICMG_HA6
15	PICMG_HA7
16	GND
17	GND
18	PICMG_SCK_A
19	PICMG_SDA_B
20	GND
21	GND
22	PICMG_SCK_B
23	PICMG_SDA_B
24	GND
25	GND
26	I2C_SDA
27	I2C_SCK
28	GND
29	GND
30	I2C_INT
31	Enable_Power_MC
32	GND
33	GND
34	SYS_RST
35	MP_Button
36	GND
37	GND
38	M48V_ALARM
39	LED_IPMC
40	GND
41	GND
42	LED_TEM
43	LED_ERR/STATUS
44	GND
45	GND
46	RST_uC
47	VCC3V3_IPM
48	GND
49	GND
50	VCC3V3_IPM
51	VCC3V3_IPM
52	GND
53	GND
54	VCC3V3_IPM
55	VCC3V3_IPM
56	GND
57	GND
58	VCC3V3_IPM
59	VCC3V3_IPM
60	GND

Connector 2

Pin	Function
1	GND
2	CONFIG_ADDR_0
3	CONFIG_ADDR_1
4	GND
5	GND
6	CONFIG_ADDR_2
7	FPGA_0_INIT_B
8	GND
9	GND
10	FPGA_1_INIT_B1
11	FPGA_1_INIT_B2
12	GND
13	GND
14	FPGA_1_INIT_B3
15	FPGA_1_INIT_B4
16	GND
17	GND
18	IPMC_BUS0
19	IPMC_BUS1
20	GND
21	GND
22	IPMC_BUS2
23	IPMC_BUS3
24	GND
25	GND
26	IPMC_BUS4
27	IPMC_BUS5
28	GND
29	GND
30	IPMC_BUS6
31	IPMC_BUS7
32	GND
33	GND
34	IPMC_BUS8
35	IPMC_BUS9
36	GND
37	GND
38	IPMC_BUS10
39	IPMC_BUS11
40	GND
41	GND
42	IPMC_BUS12
43	IPMC_BUS13
44	GND
45	GND
46	IPMC_BUS14
47	IPMC_BUS15
48	GND
49	GND
50	FRONT_CON_0
51	FRONT_CON_1
52	GND
53	GND
54	FRONT_CON_2
55	FRONT_CON_3
56	GND
57	GND_IPM_A
58	VCC3V3_IPM_A
59	VCC3V3_IPM_A
60	GND_IPM_A

LVTTL (active high) 48 Signals

QSH-030-01-F-D-A

COMPUE NODE: FRONT PANEL

LEDs

POWER: Connected to Main Input Voltage (48V or 5V)	●	● / ● IPMC: Requesting power (fast) / Hot Swap (slow) / Powered up
POWER: 3,3	●	● POWER: 2,5
POWER: 1,8	●	● POWER: 1,2
POWER: 0,9	●	● POWER: any other
FPGA#0 configured pin	●	● FPGA#0 Status LED
FPGA#1 configured pin	●	● FPGA#1 Status LED
FPGA#2 configured pin	●	● FPGA#2 Status LED
FPGA#3 configured pin	●	● FPGA#3 Status LED
FPGA#4 configured pin	●	● FPGA#4 Status LED
Volt sensor Warning/Error	● / ●	● / ● Temp Warning/Error

BUTTONS

RESET	„Software“ reset of FPGAs / Hot Swap
Reset µC	Reset pin of uC.
MP Button	Multi purpose

Display

LCD Display	eventually display (connected via flat cable)