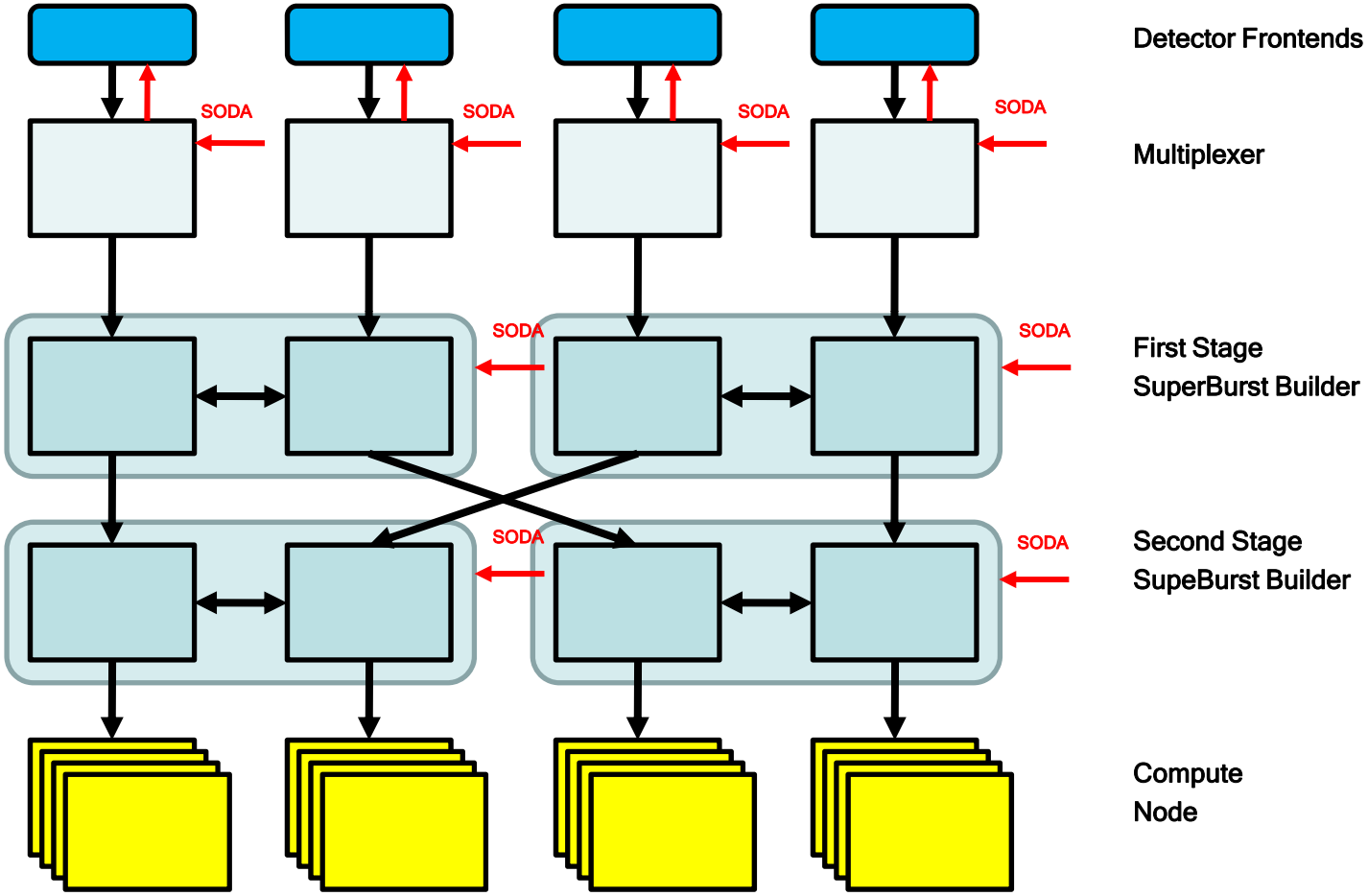
# PANDA Serial Links

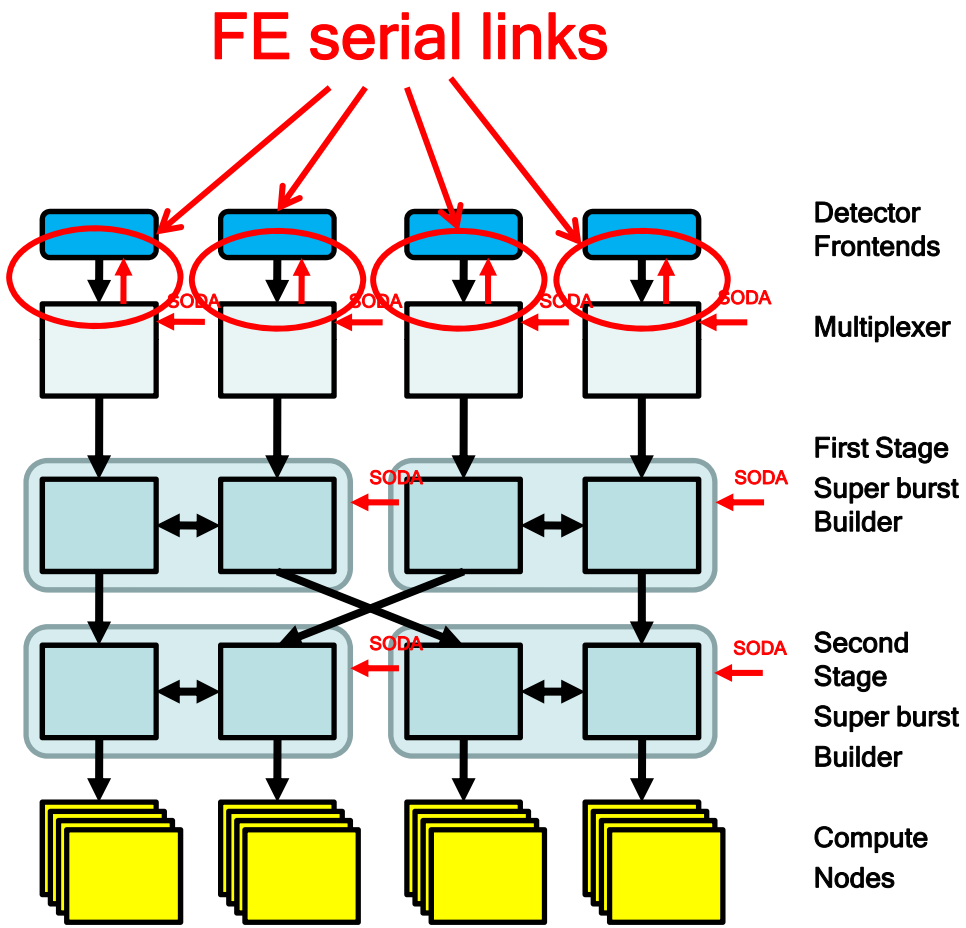
I.Konorov

- Introduction(DAQ, SODA)
- Data concentrator module
- FEE Serial Links
  - GBT
  - FPGA based Serial Links

# PANDA DAQ


Detector Frontends
SODA
SODA
SODA
SODA
Multiplexer
SODA
SODA
First Stage
SuperBurst Builder
SODA
SODA
Second Stage
SupeBurst Builder
Compute
Node

# DAQ Architecture




DAQ :

Beam structure : 2 us burst + 400 ns pause

Super burst : 500 us

Data block corresponds to one burst

Superblock corresponds to 500 us beam

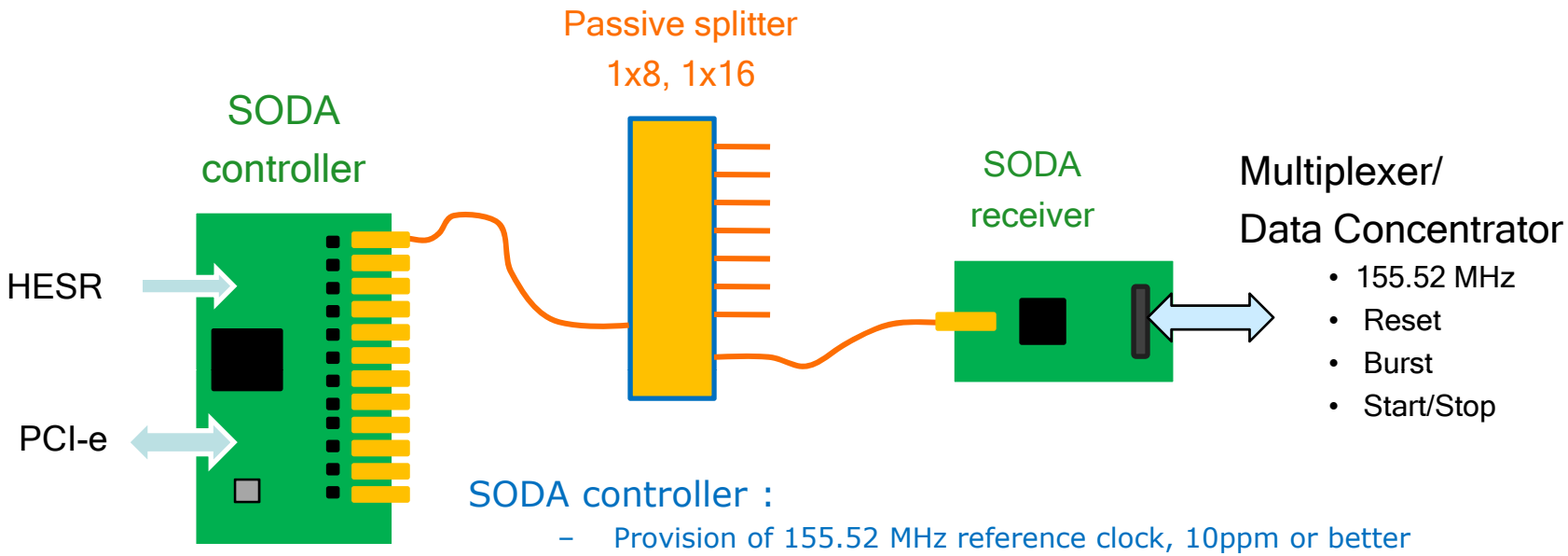
DAQ builds super bursts by Round Robin algorithm

200 GB/s sustained data rate

# RUN and Data taking

- FEEs/Multiplexers always send data unless STOPED
- Data divided to data block burst wise
- One SuperBurst = 256 Bursts or 614.4 µseconds
- Start and Stop take place only at Beginning and End of SuperBurst
- Start and Stop commands independent from Run status
- Run On/Off = Recording ON/OFF

# SODA architecture




SODA controller :

- Provision of 155.52 MHz reference clock, 10ppm or better
- Provision of RESET, Burst, SuperBurst, Start/Stop
- PC interface for configuration and status information
- Lattice FPGA with SERDES

Optical splitter :

- 1x8; 1x16; 1x32

SODA receiver:

- Mounted directly on Data Concentrator/Multiplexer module
- 155.52 MHz
- RESET, SOB, EOB, Start/Stop

# SODA interface

8/10 bit encoding

Command(packet) transmission/handshake

IDLE status

| | | | |
|---|---|---|---|
| K28.7 | K28.7 | K28.7 | K28.7 |

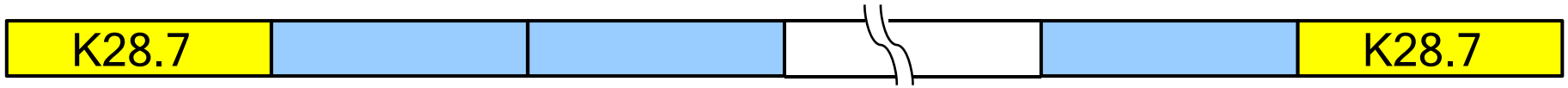
Synchronous command:

RESET, SOB, EOB, SuperBurst, Start, Stop, Trigger, 3 spare bits

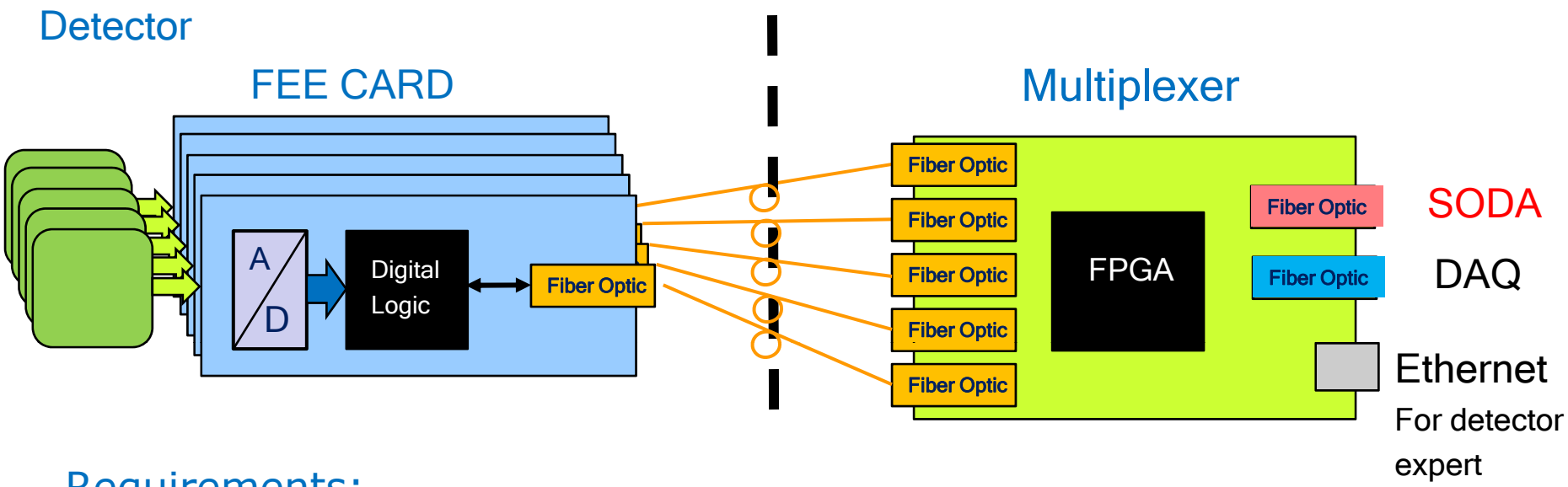
| | | | | |
|---|---|---|---|---|
| K28.7 | 0 | 10 bits | ECC(5b) | K28.7 |

Asynchronous commands

| | | | | |
|---|---|---|---|---|
| K28.7 | 1 | 8 bits | ECC(7b) | K28.7 |



# FEE connection




Requirements:

FEE interface functionality:

- SODA commands
- DATA transmission
- Slow control

Speed: 1.5-4.5Gb/s

Some detectors require radiation tolerant components

Hardware solution: FPGA with SerDes

# Motivation

- Some PANDA detectors and readout circuits will be exposed to high particle flux
  - MVD
  - Planar GEM
  - TPC (?)
  - EMC (?)

- MVD group, lacking manpower, looks for a ready to use solution for high speed optical link

Possible solution:

- GBT – Radiation hard high speed optical link

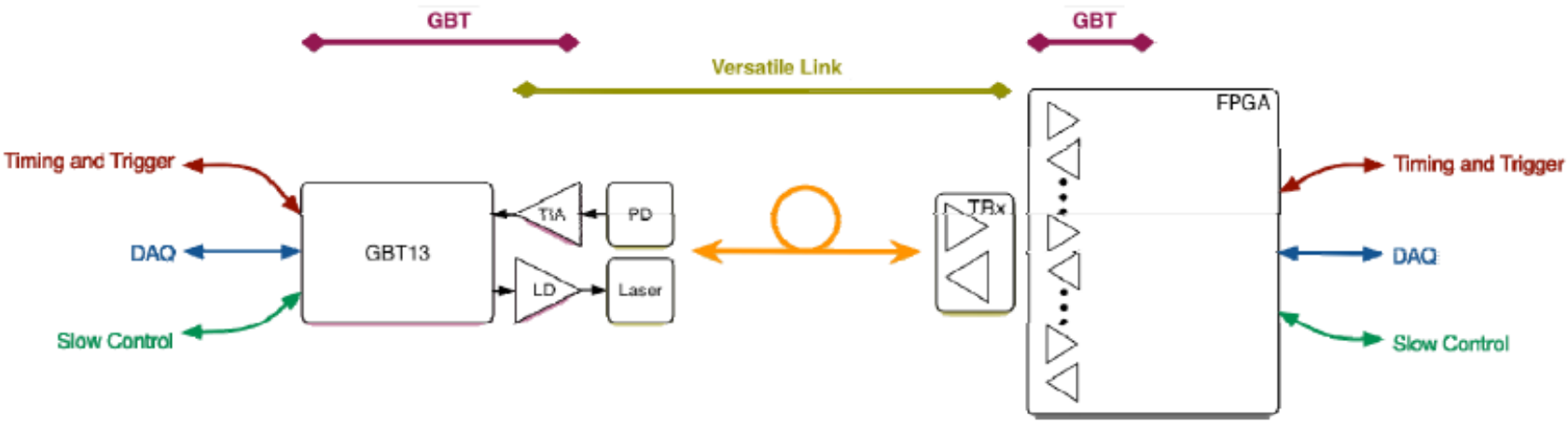
# Radiation Hard Optical Link Architecture

*Defined in the "DG White Paper"*

- *"Work Package 3-1"*
  - Objective:
    - Development of an high speed bidirectional radiation hard optical link
  - Deliverable:
    - Tested and qualified radiation hard optical link
  - Duration:
    - 4 years (2008 – 2011)

***Radiation Hard Optical Link:***

- *Versatile link project:*
  - Opto-electronics
  - Radiation hardness
  - Functionality testing
  - Packaging
- *GBT project:*
  - ASIC design
  - Verification
  - Functionality testing
  - Packaging

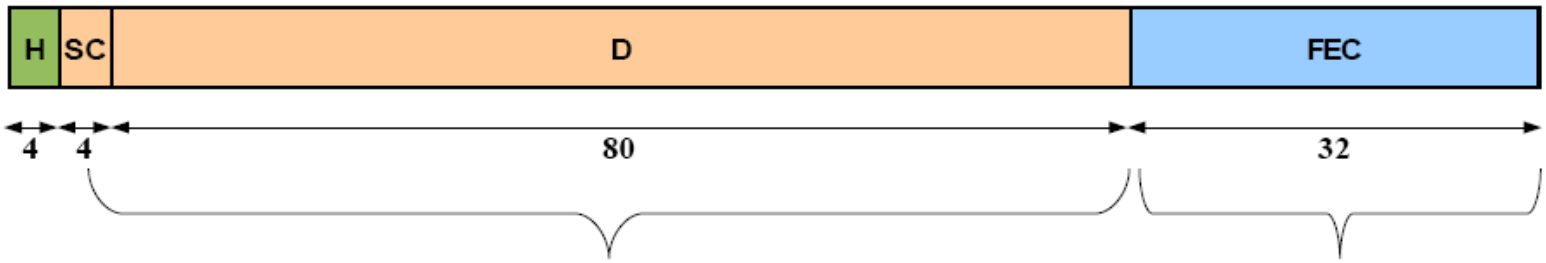



**On-Detector**
Custom Electronics & Packaging
Radiation Hard

**Off-Detector**
Commercial Off-The-Shelf (COTS)
Custom Protocol

# GBT Frame

**SLHC frame: 120 bits @ 40 MHz ≡ 4.8 Gbps**




**User field: 82 bits ≡ 3.28 Gbps**

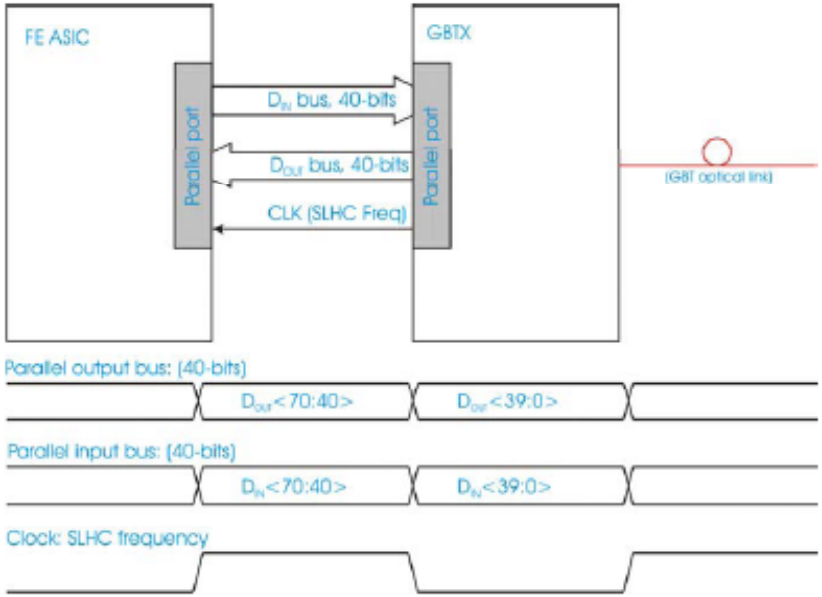
**Reed-Solomon overhead allowing to correct up to 16 consecutive erroneous bits**

H: Header, 4 bits
SC: Slow Control 4 bits
GBT control 2 bits (80 Mb/s)
Slow control 2 bits (80 Mb/s)
D: Data (3.2 Gbps)
FEC: Forward Error Correction (32 bits)

**Line efficiency: 68%**

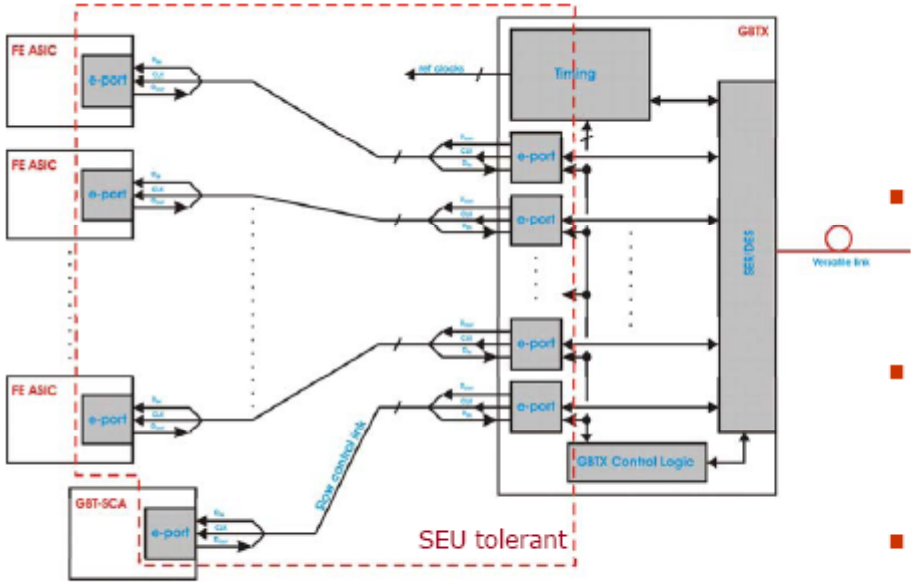
# GBTX-TO-FRONTEND: Parallel Modes

- *P-Bus Mode:*
  - Simple parallel interface
  - 40-bit wide bus
  - Bidirectional
  - Double Data Rate (DDR)
- *B-Bus Mode:*
  - A byte-bus mode is also available
  - Up to five independent buses can be used simultaneously
- *Electrical levels:*
  - SLVS electrical level:
    - 100 Ω termination
    - 400 mV differential
    - 200 mV common mode
    - $I_{LOAD}$ = ± 2 mA




JEDEC standard, JESD8-13
Scalable Low-Voltage Signalling for 400 mV (SLVS-400)
http://www.jedec.org/download/search/JESD8-13.pdf

# GBTX-TO-FRONTEND: E-Link Modes




| Mode | Type | Data Rate | Notes |
|---|---|---|---|
| **OFF** | Power off | - | |
| **B-Bus** | parallel | 80 MB/s | Up to 5 Bytes (DDR) |
| **P-Bus** | parallel | 80 MW/s | One 40-bit word (DDR) |
| **2 ×** | serial | 80 Mb/s | Up to 40 serial links |
| **4 ×** | serial | 160 Mb/s | Up to 20 serial links |
| **8 ×** | serial | 320 Mb/s | Up to 10 serial links |
| **8 ×** | serial-lanes | > 320 Mb/s | |

- *GBT/Frontend interface:*
  - Electrical links (e-link)
  - Serial
  - Bidirectional
  - Up to 40 links
- *Programmable data rate:*
  - Independently in five groups
  - Independently for up/down links
  - 80 Mb/s, 160 Mb/s and 320 Mb/s
- *Lanes:*
  - To achieve > 320 Mb/s
  - Two or more e-links can be grouped forming a "lane"
- *Slow control channel:*
  - 80 Mb/s
- *E-Link:*
  - Three pairs: $D_{OUT}/D_{IN}/CLK$
  - SLVS
- *E-Links will be handled by E-ports:*
  - Electrically
  - "Protocol"
- *Package (preliminary):*
  - BGA: 361 – PINS
  - 16 mm x 16 mm, 0.8 mm pitch

# GBLD

***Main specs:***

- Bit rate 5 Gb/s (min)
- Modulation:
  - current sink
  - Single-ended/differential
- Laser modulation current: 2 to 12 mA
- Laser bias: 2 to 43 mA
- "Equalization"
  - Pre-emphasis/de-emphasis
  - Independently programmable for rising/falling edges
- Supply voltage: 2.5 V
- Die size: 2 mm × 2 mm
- I2C programming interface

***Packaging:***

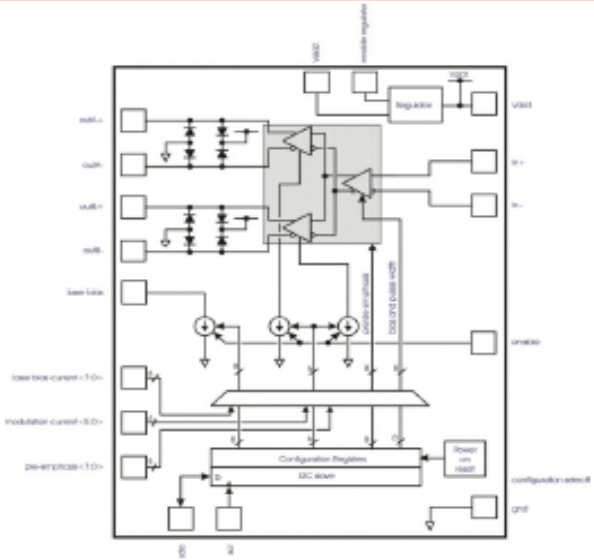
- Part of the versatile link project

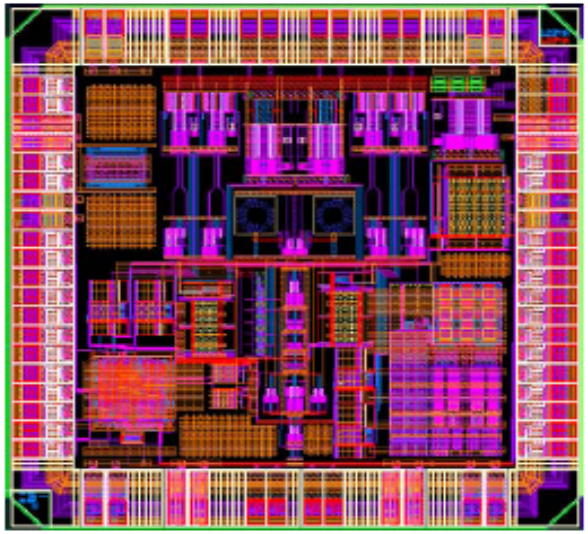
***Engineers :***

- Gianni Mazza – INFN, Italy
- Ping Gui – SMU, USA
- Angelo Rivetti – INFN, Italy
- Ken Wyllie – CERN, Switzerland

***Status:***

- Chip fabricated and tested
- A re-spin was necessary:
  - Chip submitted for fabrication: 16-Feb-2010





# GBTIA

***Main specs:***

- Bit rate 5 Gb/s (min)
- Sensitivity: 20 µA P-P ($10^{-12}$ BER)
- Total jitter: < 40 ps P-P
- Input overload: 1.6 mA (max)
- Dark current: 0 to 1 mA
- Supply voltage: 2.5 V
- Power consumption: 250 mW
- Die size: 0.75 mm × 1.25 mm

***Packaging:***

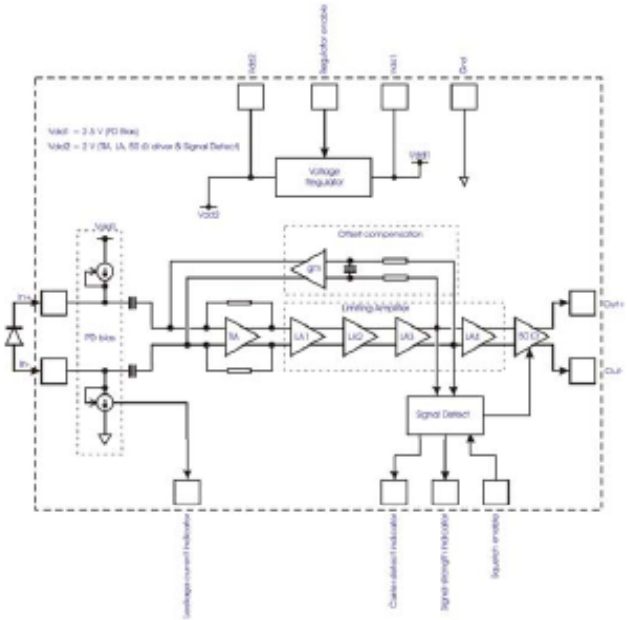
- Part of the versatile link project

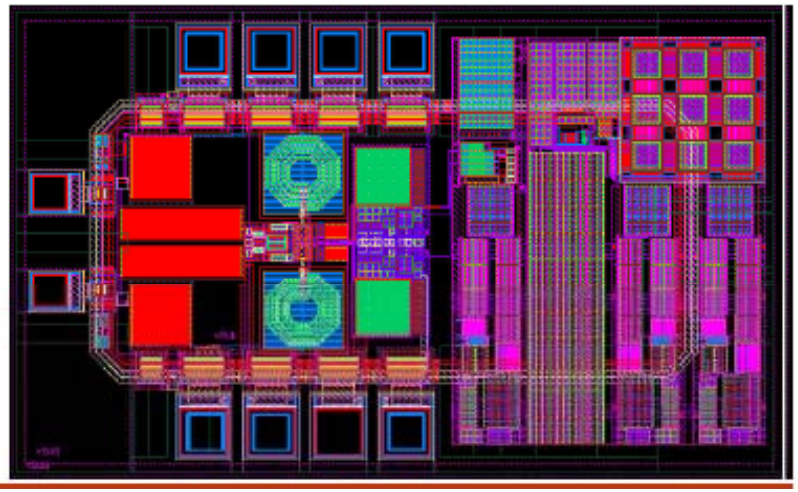
***Engineers :***

- Ping Gui – SMU, USA
- Mohsine Menouni – CPPM, France

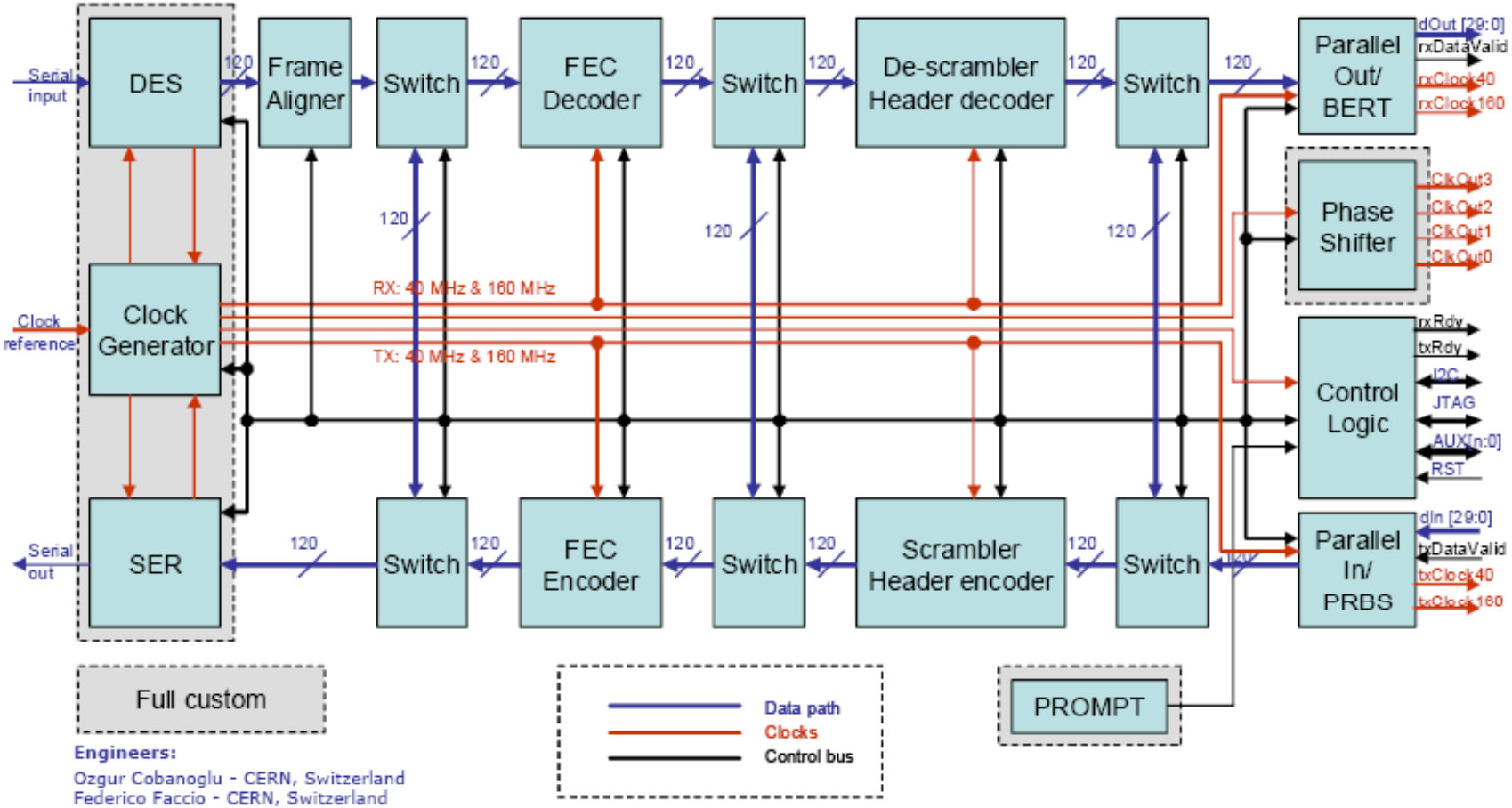
***Status:***

- Chip fabricated and tested
- Chip fully meets specifications!
- Radiation tolerance proven!
- Work has started to encapsulate the GBTIA + PIN-diode in a TO Package
  - (Versatile link project)





# GBT-SERDES

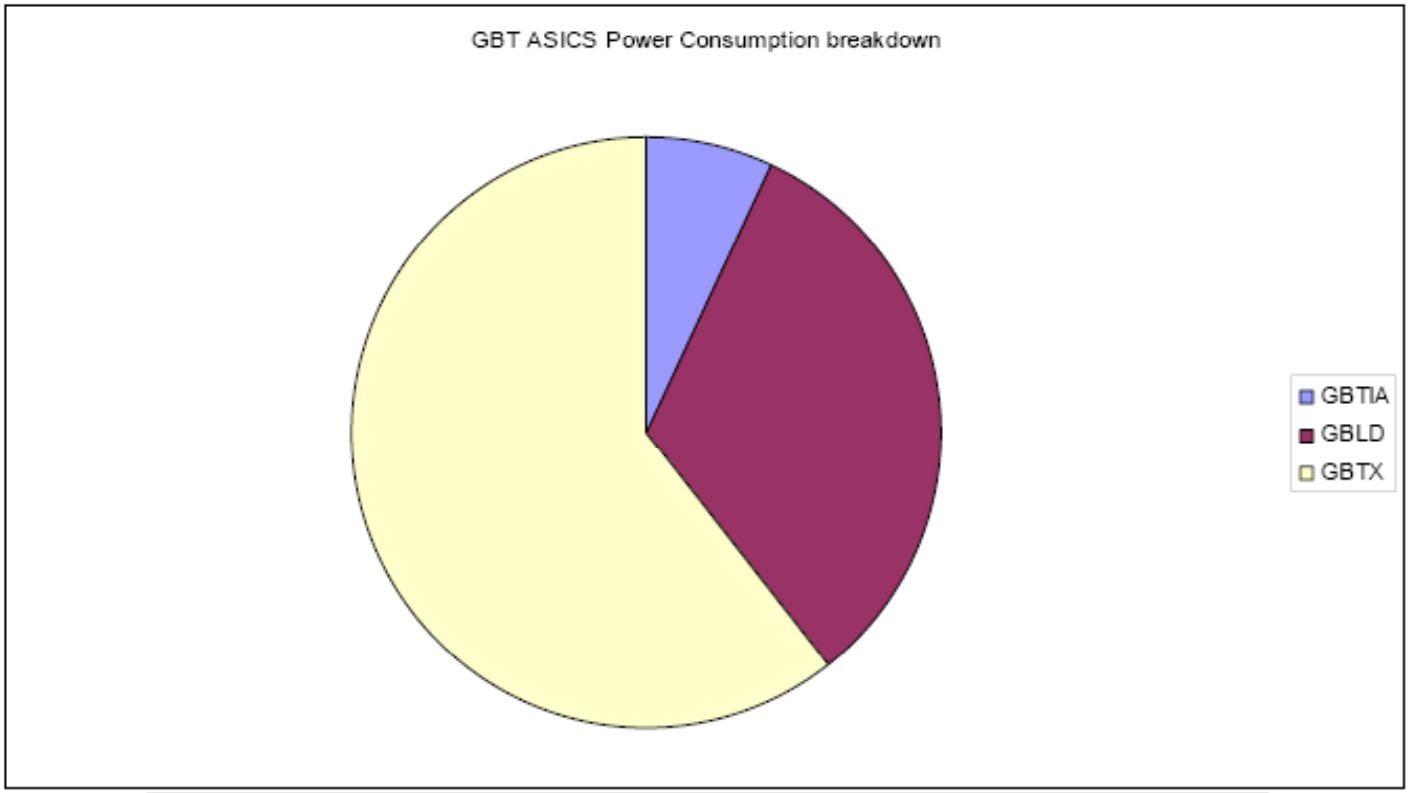



**Engineers:**

Ozgur Cobanoglu - CERN, Switzerland
Federico Faccio - CERN, Switzerland
Rui Francisco – CERN, Switzerland
Ping Gui – SMU, USA
Alessandro Marchioro - CERN, Switzerland
Paulo Moreira - CERN, Switzerland
Christian Paillard - CERN, Switzerland
Ken Wyllie - CERN, Switzerland

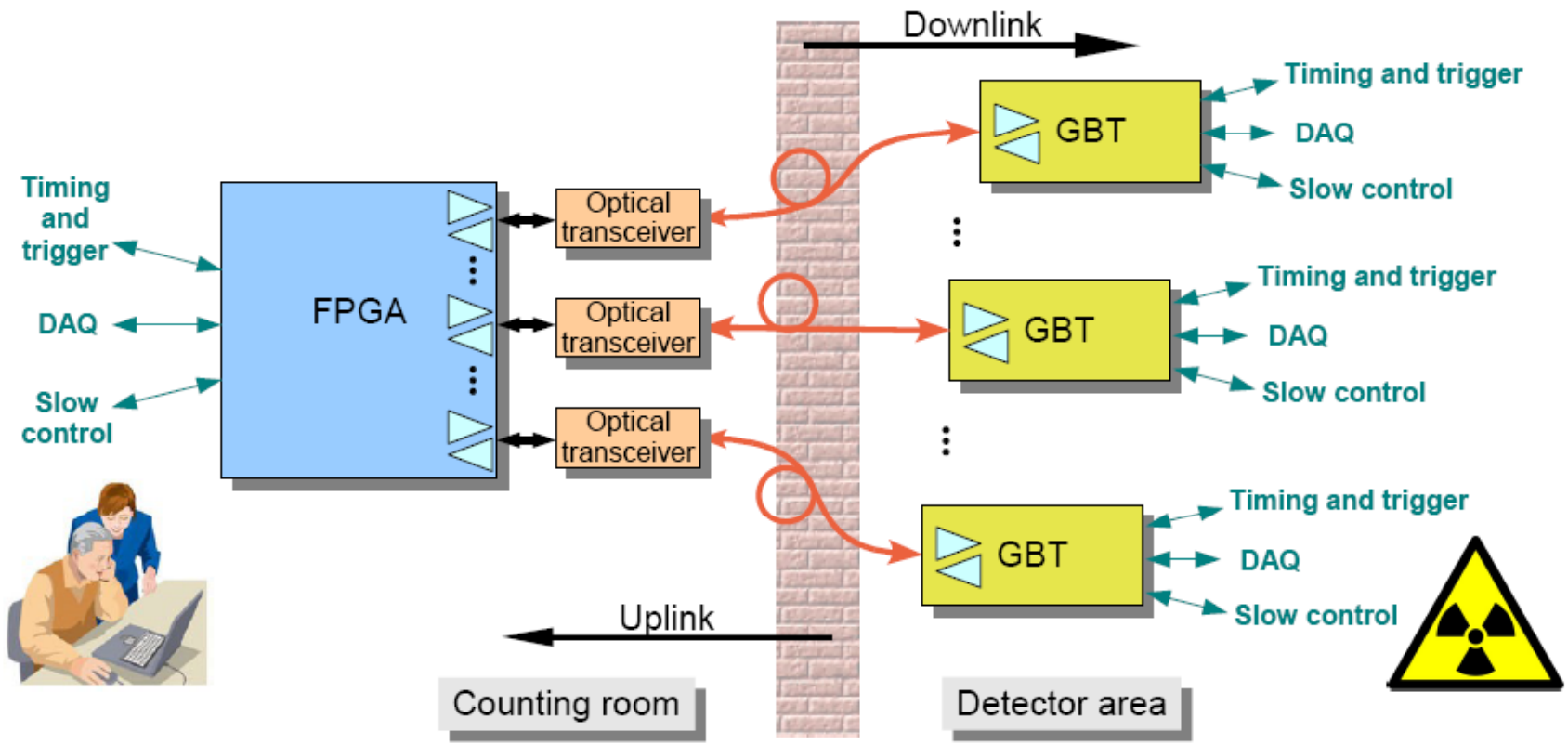
- Submitted for fabrication: 26-Nov-2009
- Currently being packaged.

# GBT Chipset – Power Consumption




| Summary | Power [mW] |
|---|---|
| GBTIA | 123.7 |
| GBLD | 585.9 |
| GBTX | 1092.3 |
| **Total (max)** | 1801.9 |

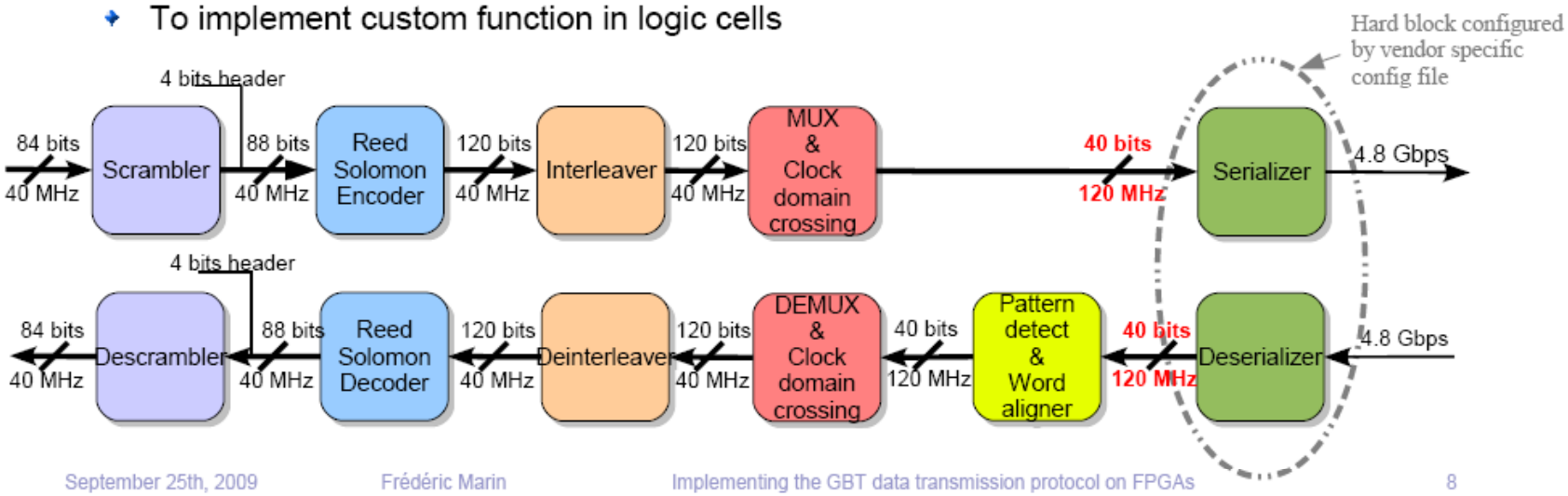
# Typical architecture




GBT protocol needs to be compatible with the FPGAs and vice versa

# GBT in FPGA

- FPGA devices from Altera or Xilinx embed serial transceivers configurable for several standard telecommunication protocols (XAUI, Gigabit Ethernet, PCIe, ...)
- **But:**
  - Transceivers include neither scrambler nor Reed Solomon encoder nor interleaver
  - Their word aligner/comma detection module are not flexible/configurable enough to fit our needs
  - The width of the parallel interface of the ser/des can only take predefine values
- So the way to implement the GBT protocol on FPGA is:
  - To use the transceiver in the most basic way (ser/des function)
  - To implement custom function in logic cells



# Usage of FPGA resources

## Resource usage

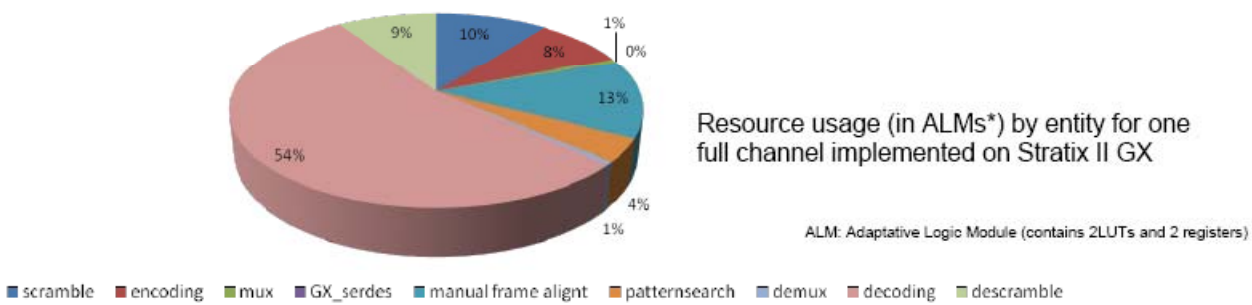
- Implementing several channels leads to an important usage of logic cells resources

| Max usable/available nb of channel | Altera Stratix II GX | Logic cells usage in % |
|---|---|---|
| 8/8 | EP2SGX30D | 92% |
| 12/12 | EP2SGX60D | 78% |
| 16/16 | EP2SGX90E | 69% |
| 20/20 | EP2SGX130G | 59% |
| 24/24 | | |

| Max usable/available nb of channel | Xilinx Virtex 5 | Logic cells usage in % |
|---|---|---|
| 3/8 | XC5VFX30T | 87% |
| | | |
| 10/16 | XC5VFX100T | 93% |
| 13/20 | XC5VFX130T | 94% |
| 20/24 | XC5VFX200T | 96% |

This table gives only ressource usage in terms of logic cells but other ressources are used such as DSP blocks or RAM.
Differences between Altera and Xilinx logic cells usage can be explained by the different policies they adopt in term of ratio between number of logic cells and number of transceivers.

- The Reed Solomon decoder takes most of the resources




Resource usage (in ALMs*) by entity for one full channel implemented on Stratix II GX

ALM: Adaptative Logic Module (contains 2LUTs and 2 registers)

# FPGA implementation of GBT protocol

- GBT functionality implemented and tested
- Problem with fixed propagation time:
  - to be demonstrated

# Project Schedule

- *2008*
  - Design and prototyping of performance critical building blocks:
    - GBTIA, GBLD, Serializer, De-Serializer, Phase Shifter
  - First tests of optoelectronics components
    - SEU tests on PIN receivers
  - Proceed with the link specification meetings
  - General link specification
- *2009*
  - Design/prototype/test of basic serializer/de-serializer (GBT-SERDES) chip
    - GBT-SERDES ("Tape-out" 9th of November)
  - Design/prototype/test of optoelectronics packaging
    - GBTIA + PIN on TO CAN
- *2010*
  - GBLD re-spin
  - GBT-SERDES testing ← !
  - Detailed link specification document
  - Full prototype of optoelectronics packaging
  - Prototype of "complete" GBTX chip ?
- *2011*
  - Extensive test and qualification of full link prototypes
  - System demonstrator (s) with use of full link
  - Schedule of the final production version is strongly dependent on the evolution of the LHC upgrade schedule

# GBT and PANDA

- Compatibility to be verified
  - compatibility with SODA ?
    - GBT frequency 160MHz  and it can also run at 155.52 MHz ☺
    - Only 2 synchronous bits while SODA ☹
    - 38.88 MHz (155.52/4) recovered clock frequency
  - compatibility with FEE ?

- GBT implementation requires significant hardware resources POWER, FPGA

- GBT should be used only for FEE where commercial components can not be used

  -> two types of serial link protocols between FEE and Data Concentrator

  -> GBT based Data Concentrator module

- GBT optical components certainly of interest for PANDA

  TIA, LD, PDiode, Laser

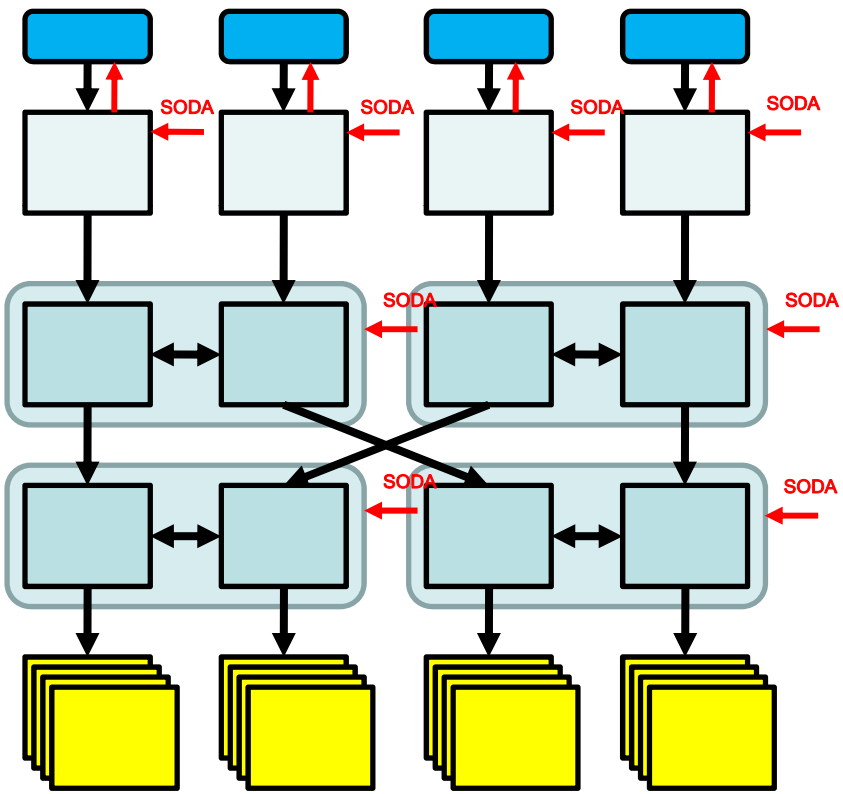
  We have to express our interest in written form

# FPGA based serial link implementation

- 8/10 bit encoding
- Protocol
  - Continuous sequence of fixed frames like GBT
  - Single packets of variable length like SODA

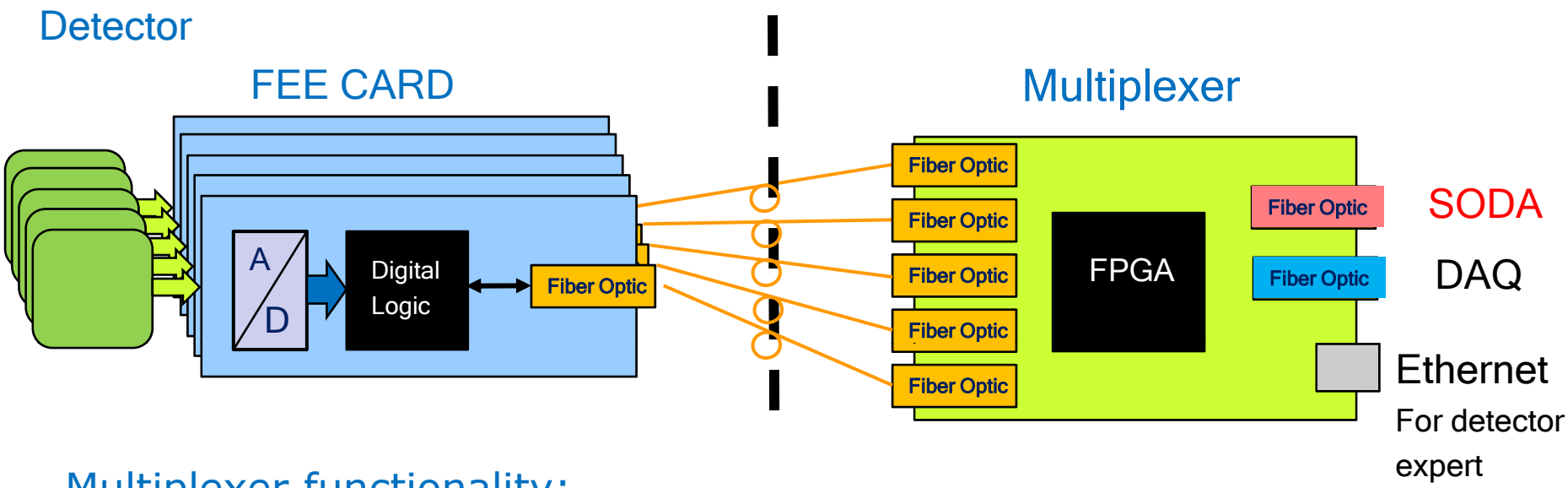
- Continuous frames vs Single packets
  - Frame: advanced error correction functionality ☺
  - Frame: Limited flexibility ☹
  - Packet: flexible ☺
  - Packet: advanced error correction capability to be studied ☹

# Responsibilities




| | |
|---|---|
| Detector Frontends | Detector groups |
| Multiplexer | Detector group s?<br>DAQ group or dedicated group ? |
| First Stage Super burst Builder | DAQ group |
| Second Stage Super burst Builder | DAQ group |
| Compute Nodes | DAQ group |

# Multiplexer




Multiplexer functionality:

- Clusterization (EMC)
- Time ordering (MVD, TPC, STT)
- ….

CN == Multiplexer ?

Request: detector experts should specify requirements for Multiplexer module

# FEE responsible person for every Detector

# SPARE SLIDES

# Synchronous command

**a)**

| | | | |
|---|---|---|---|
| **Packet N** | **K28.7** | **K28.7** | **Packet N+1** |

**b)**

| | | | | |
|---|---|---|---|---|
| **Part 1 of packet N** | **K28.7** | **Synchronous Command** | **K28.7** | **Part 2 of packet N** |

# Communications

- EMC meeting
  - EMC group assigned Myroslav Kravtsyuk as responsible for EMC readout electronics
  - Work Packages for development of EMC readout defined
  - Many packages got responsible institutes

- Other detector groups should define work packages and assign responsible institutes

  - can be discussed in Rauischholzhausen

- MVD group triggered discussion about GBT usage in PANDA

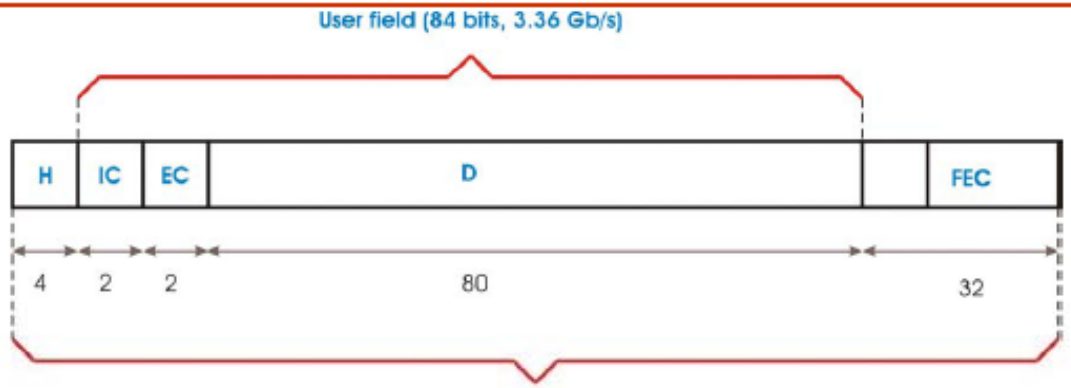
Meeting with CERN Microelectronic group on March 4-th

- FE/TDAQ workshop in Rauischholzhausen April 14-17

Registration for the workshop:

https://indico.gsi.de/conferenceDisplay.py?confId=911

# GBT Link Bandwidth




H: Header, 4 bits
IC: GBT control, 2 bits (80 Mb/s)
EC: Data or Slow control port, 2 bits (80 Mb/s)
D: DATA/TTC/EC - User data, 80 bits (3.2 Gb/s)
FEC: Forward Error Correction, 32 bits

- *Bandwidth:*
  - User: 3.36 Gb/s
  - Line: 4.8 Gb/s
- *Dedicated channels:*
  - Link control: 80 Mb/s
  - Data/Slow control channel: 80 Mb/s
- *DC balance:*
  - Scrambler
  - No bandwidth penalty
- *Forward Error Correction and Frame Synchronization*
  - Efficiency: 73%
  - To be compared with 8B/10B: 80%
    - no error correction capability
- *Link is bidirectional*
- *Link is symmetrical:*
- *Down-link highly flexible:*
  - Can convey unique data to each frontend device that it is serving
  - "Soft" architecture managed at the control room level
  - Other schemes would require dedicated topologies that will be difficult to accommodate on a generic ASIC like the GBTX
- *Line code and frame structure compatible with modern FPGAs*

# The GBT Chipset

- *Radiation tolerant chipset:*
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and Timing Transceiver
  - GBT-SCA: Slow control ASIC
- *Supports:*
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s
- *The target applications are:*
  - Data readout
  - TTC
  - Slow control and monitoring links.
- *Radiation tolerance:*
  - Total dose
  - Single Event Upsets